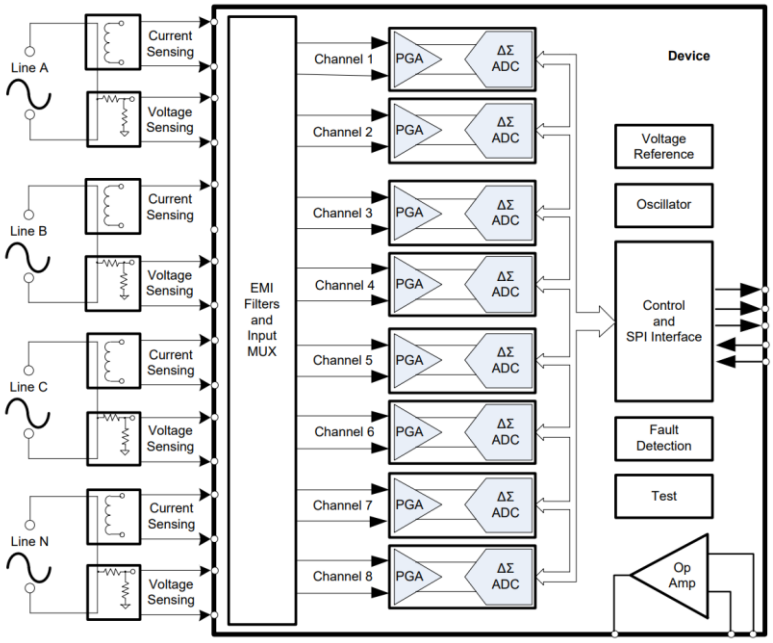
1. Features

- Eight-channel differential analog-to-digital converter (ADC) input
- Excellent performance:
  Dynamic range: 118dB at 1kSPS
  Crosstalk : -110 dB
  (THD): -90 dB at 50 Hz and 60 Hz
- Analog power range options:
  3V to 5V (unipolar)
  ±2.5V (bipolar, DC coupling allowed)
- Digital: 1.8V to 3.6V
- Low power consumption: 2mW per channel
- Data rates: 1, 2, 4, 8, 16, 32, and 64
- Programmable gain: 1, 2, 4, 8, 12, 24
- Fault detection and device testing functions
- SPI™ data interface and four general purpose input/output (GPIO) interfaces.
- Package: TQFP (64)
- Operating temperature range:
  -40℃ to 105℃

2. Applications

- Power supply protection: circuit breaker and relay protection
- Electricity metering: single-phase, multi-phase, and power quality
- Battery testing system
- Test and Measurement
- Synchronous Data Acquisition System



. Function Description

The DADS131E04/08 is a series of multi-channel, synchronous sampling, 24-bit delta - sigma analog-to-digital converters (ADCs) with a built-in programmable gain amplifier (PGA), internal reference, and onboard oscillator. With its wide dynamic range, scalable data transfer rates, and internal fault detection monitor, the DADS131E04/08 is favored for industrial power monitoring and protection, as well as test and measurement applications. True high-impedance inputs allow the DADS131E04/08 to be directly connected to a resistive divider network or voltage transformer to measure line voltage, or connected to a current transformer or Rogowski coil to measure current. Thanks to its high integration and excellent performance, the DADS131E04/08 series enables the creation of scalable industrial power systems with significantly reduced size, power consumption, and overall cost. The DADS131E04/08 features a flexible input multiplexer on each channel, which is independently connected to internally generated signals for test, temperature, and fault detection. Fault detection is performed internally by the device, which uses an integrated comparator with a trigger level controlled by a digital-to-analog converter (DAC). The DADS131E04/08 can operate at data rates up to 64 kSPS.

These complete analog front-end (AFE) solutions are packaged in a TQFP-64 package and rated for industrial use with a temperature range of -40°C to +105°C.

Device Information

Device Model	Packaging	Package size (nominal value)
DADS131E04LFP	TQFP (64)	10.00mm x 10.00mm
DADS131E08LFP	TQFP (64)	10.00mm x 10.00mm

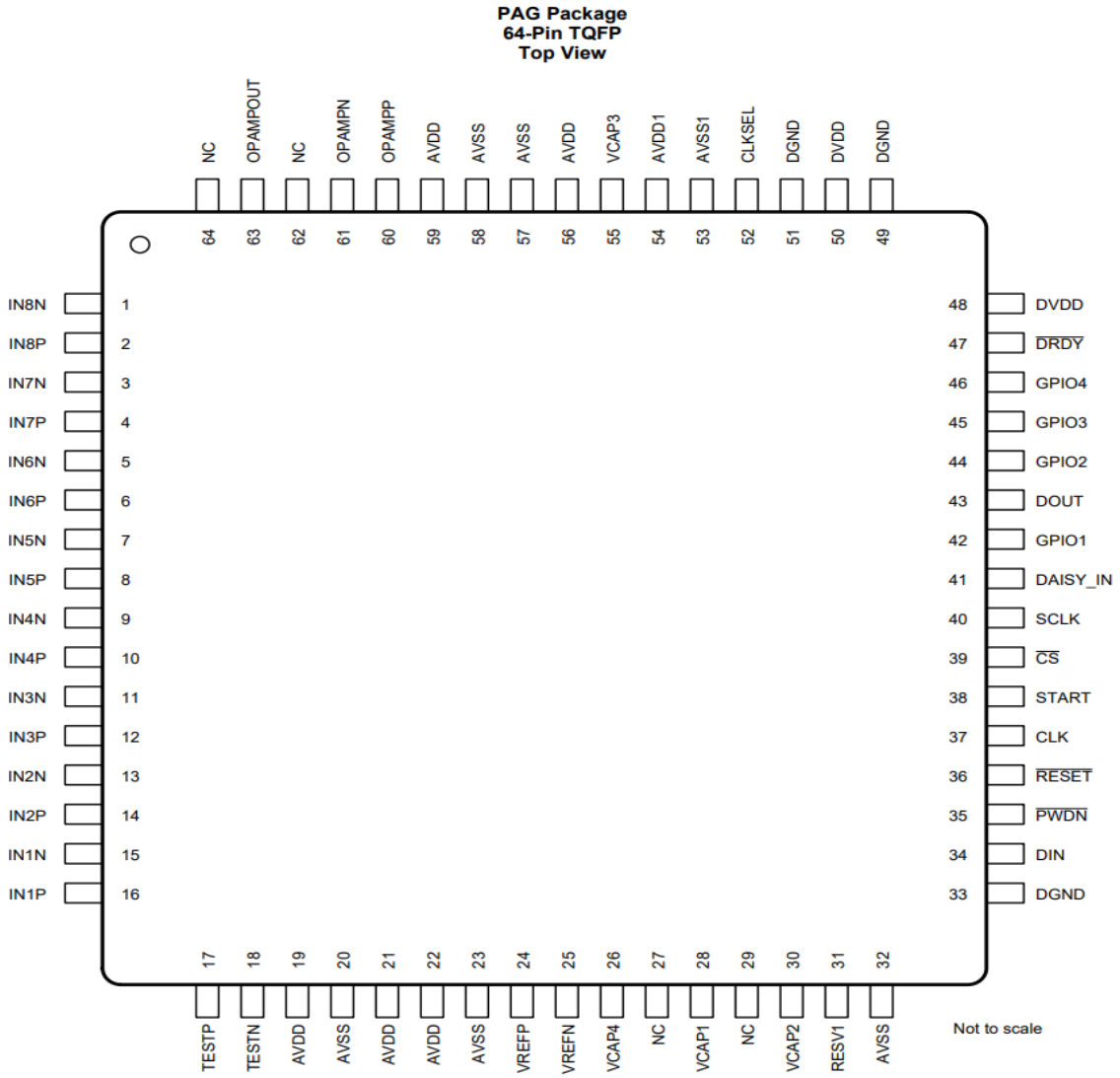
4. Revision Record

Version 2024.5 is the initial version of the datasheet.

5. Device Comparison

Devices	Number of Channels	Packaging	Resolution	Maximum Sampling Rate (kSPS)
DADS131E04	4	TQFP-64	24	64
DADS131E08	8	TQFP-64	24	64

6. Pin Configuration and Functions



Pin Functions

Pin		I/O	Description
Name	No.		
AVDD	19, 21, 22, 56	Supply	Analog power supply. Connect a 1μF capacitor to the AVSS.
AVDD	59	Supply	Charge pump analog power supply. Connect a 1μF capacitor to AVSS, pin 58.
AVDD1	54	Supply	Analog power supply. Connect a 1μF capacitor to AVSS1.
AVSS	20, 23, 32, 57	Supply	Analog ground
AVSS	58	Supply	Charge pump simulation
AVSS1	53	Supply	Analog ground
OPAMPN	61	Analog Input/Output	Op-amp inverting input
OMAMPOUT	63	Analog output	op-amp output
OPAMPP	60	Analog Input	Op-amp non-inverting input
$\overline{CS}$	39	Digital input	Chip select, active low
CLK	37	Digital input	Master clock input
CLKSEL	52	Digital input	Master clock selection
DAISY_IN	41	Digital input	Daisy chain input
DGND	33, 49, 51	Supply	Digital ground
DIN	34	Digital input	Serial data input
DOUT	43	Digital output	Serial digital output
$\overline{DRDY}$	47	Digital output	Data ready, active low
DVDD	48, 50	Supply	Digital power supply. Connect a 1μF capacitor to DGND.
GPIO1	42	Digital Input/Output	General Purpose Input/Output Pin 1 If not in use, please connect a resistor of ≥10kΩ to DGND.
GPIO2	44	Digital Input/Output	General Purpose Input/Output Pin 2 If not in use, please connect a resistor of ≥10kΩ to DGND.
GPIO3	45	Digital Input/Output	General purpose input/output pin 3 If not in use, please connect a resistor of ≥10kΩ to DGND.
GPIO4	46	Digital Input/Output	General purpose input/output pin 4 If not in use, please connect a resistor of ≥10kΩ to DGND.
IN1N	15	Analog Input	Differential Analog Negative Input 1
IN1P	16	Analog Input	Differential Analog Positive Input 1
IN2N	13	Analog Input	Differential Analog Negative Input 2
IN2P	14	Analog Input	Differential Analog Positive Input 2
IN3N	11	Analog Input	Differential Analog Negative Input 3
IN3P	12	Analog Input	Differential Analog Positive Input 3
IN4N	9	Analog Input	Differential Analog Negative Input 4
IN4P	1 0	Analog Input	Differential Analog Positive Input 4
IN5N	7	Analog Input	Differential Analog Negative Input 5 (DADS131E08 only)
IN5P	8	Analog Input	Differential analog positive input 5 (DADS131E08 only)
IN6N	5	Analog Input	Differential Analog Negative Input 6 (DADS131E08 Only)
IN6P	6	Analog Input	Differential analog positive input 6 (DADS131E08 only)
IN7N	3	Analog Input	Differential Analog Negative Input 7 (DADS131E08 only)
IN7P	4	Analog Input	Differential Analog Positive Input 7 (DADS131E08 Only)
IN8N	1	Analog Input	Differential analog negative input 8 (DADS131E08 only)
IN8P	2	Analog Input	Differential analog positive input 8 (DADS131E08 only)
NC	27, 29, 62, 64	---	No connection, keep open
$\overline{RESET}$	36	Digital input	System reset, active low
RESV1	31	Digital input	Reserved, directly connected to DGND
SCLK	40	Digital input	Serial clock input
TESTP	17	Analog Input/Output	Test signal 1
TESTN	16	Analog Input/Output	Test signal 2
START	38	Digital input	Synchronization signal for starting or restarting the conversion
$\overline{PWDN}$	35	Digital input	Power off, low level is active
VCAP1	28	Analog output	Analog bypass capacitor pin; connect a 470pF capacitor to AVSS.
VCAP2	30	Analog output	Analog bypass capacitor pin; connect a 270nF capacitor to AVSS.

Pin		I/O	Description
Name	No.		
VCAP3	55	Analog output	Analog the bypass capacitor pin; connect a 270nF capacitor to the AVSS.
VCAP4	26	Analog output	Analog the bypass capacitor pin; connect a 270nF capacitor to the AVSS.
VREFN	25	Analog Input	Negative analog reference voltage.
VREFP	24	Analog Input/Output	Positive analog reference voltage; connect a 330nF capacitor to VREFN.

7. Specifications

7.1 Absolute Maximum Ratings

		Min	Max	Unit
Voltage (1)	AVDD to AVSS	-0.3	5.5	V
	DVDD to DGND	-0.3	3.9	
	AVSS to DGND	-3	0.2	
	VREFP to AVSS	-0.3	AVDD + 0.3	
	VREFN to AVSS	-0.3	AVDD + 0.3	
	Analog Input	AVSS – 0.3	AVDD + 0.3	
	Digital input	DGND – 0.3	DVDD + 0.3	
Current (1)	Input, continuous, any pin except power supply pins.	-10	10	mA
Temperature (1)	At the junction, T_J		150	℃
	Storage, T_{stg}	-60	150	

(1) Stress exceeding the values listed below under absolute maximum ratings may cause permanent damage to the chip. These listed values are only stress ratings and do not represent the chip's stress under these conditions. It can operate normally under these conditions and under any other conditions beyond the recommended operating conditions. Prolonged operation under absolute maximum rated conditions may affect the reliability of the chip.

(2) The input pins are clamped to the power rails via diodes. If the analog input voltage exceeds AVDD+0.3V or falls below AVSS -0.3V, or if the digital input voltage exceed DVDD+0.3V or lower than DGND -0.3V, the input current will be limited to 10mA or lower.

7.2 ESD Ratings

		Min	Value	Unit
V_{ESD}	Electrostatic discharge	Human Model (HBM), for ANSI/ESDA/JEDEC JS-001 (1)	±1000	V

7.3 Recommended Operating Conditions

			Min	Nom	Max	Unit
Power Supply						
Analog power supply		AVDD to AVSS	2.7	5	5.25	V
Digital power supply		DVDD to DGND	1.8	1.8	3.6	V
Analog to Digital Power Supply		AVDD – DVDD	-2.1		3.6	V
Analog Inputs						
Full-scale differential input voltage		VINxP – VINxN		±VREF/Gain		V
VCM Input Common Mode Range		(VINxP – VINxN) / 2	See section 9.3.3 for details.			
Voltage Reference Input						
Reference voltage	Reference input voltage	VREF = (VREFP – VREFN)		4.5		V
VREFN	Negative input			AVSS		V
VREFP	Positive input			AVSS + 4.5		V
Clock Input						
Clock frequency	External clock input frequency	CLKSEL pin = 0	1.5	2.048	2.25	MHz
Digital Input						
Input voltage			DGND – 0.1		DVDD + 0.1	V
Temperature Range						
T_A	Operating temperature range		-40		85	℃

7.4 Electrical Characteristics

Typical specifications are applicable to T_A = 25 °C. All specifications are applicable under the following conditions: DVDD = 1.8V,

AVDD – AVSS = 5V (1), V_{REF} = 4.5V, external f_{CLK} = 2.048MHz. Data rate = 4KSPS, HR mode, and gain = 1 (unless otherwise specified).

Parameter	Test Conditions	Min	Typ	Max	Unit
Analog Input					
Input capacitor			20		pF
Input bias current	T_A = -40℃ to 105℃, Input = 1.5V		±1.2		nA
DC input impedance		1000			MΩ
PGA Performance					
Gain settings		1, 2, 4, 6, 8, 12, 24			
bandwidth		Please refer to the PGA description.			
ADC Performance					
Resolution	Data rates up to 64kSPS	24			Bit
Data rate	f_{CLK} = 2.048MHz, HR mode	1000		64000	SPS
	f_{CLK} = 2.048MHz, LP mode	250		16000	SPS
DC Channel Performance					
Input reference noise (2)	Gain = 6, 10 seconds of data		5		μVPP
	Gain = 6,256kJ, 0.5 seconds of data.		4	7	μVPP
	Gain setting ≠ 6, data rate ≠ 500SPS	Please refer to the noise measurement section.			
Integral nonlinearity (4)	Full scale, gain = 6, best fit		10		ppm
Offset error			±500		μV
Offset error drift			2		μV/℃
Gain error	Excluding voltage reference error		±0.2	±0.5	% of FS
Gain drift	Excluding voltage reference drift		5		ppm/℃
Gain matching between channels			0.3		% of FS
AC Channel Performance					
CMRR Common Mode Rejection Ratio (3)	f_{CM} = 50Hz , 60Hz	-105	-110		dB
PSRR (Power Supply Rejection Ratio)	f_{PS} = 50Hz , 60Hz		90		dB
Crosstalk	f_{IN} = 50Hz, 60Hz		-126		dB
SNR (Signal-to-Noise Ratio)	f_{IN} = 10Hz input , gain = 6		112		dB
THD Total Harmonic Distortion	10Hz, -0.5dBFs		-98		dB
	100Hz, -0.5dBFs		-100		dB
Operational Amplifier (OPAMP)					
Noise	BW = 150Hz		7		$μV_{RMS}$
Gain-bandwidth product	50kΩ || 10pF load, gain = 1		100		kHz
Slewing rate	50kΩ || 10pF load, gain = 1		0.25		V/μs
Drive strength			50		μA
Total Harmonic Distortion	f_{IN} = 100Hz, gain = 1		-70		dB
Common mode input range		AVSS+0.7		AVDD–0.3	V
Static current			20		μA
Fault Detection					
Comparator threshold accuracy			±30		mV
External Reference					
Input impedance			10		kΩ
Internal Benchmark					
Output voltage	Register bit CONFIG3.VREF_4V = 0, AVDD ≥2.7V		2.4		V
	Register bit CONFIG3.VREF_4V = 1, AVDD ≥4.4V		4		V
V_{REF} accuracy			±2%		
Internal reference drift	TA = 25%		35		ppm/℃
	Commercial grade: 0 ℃ to 70℃		35		ppm

Parameter		Test conditions		Min	Typ	Max	Unit
Startup time							
Power	DADS131E04	AVDD – AVSS = 3V	HR mode (64KSPS)				mW

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consumption			LP mode (250SPS)				mW
		AVDD – AVSS = 5V	HR mode (64KSPS)				mW
			LP mode (250SPS)				mW
	DADS131E08	AVDD – AVSS = 3V	HR mode (64KSPS)				mW
			LP mode (250SPS)				mW
		AVDD – AVSS = 5V	HR mode (64KSPS)		30	33	mW
			LP mode (250SPS)				mW
Power outage		AVDD – AVSS = 3V			10		μW
		AVDD – AVSS = 5V			20		μW
Standby mode		AVDD – AVSS = 3V			2		mW
		AVDD – AVSS = 5V			4		mW
Static channel power		AVDD – AVSS = 3V, PGA + ADC			818		μW
		AVDD – AVSS = 5V, PGA + ADC			1.5		mW

(1) The performance is also applicable to 5V operation. Production testing for the limits is performed at 3V.

(2) Noise data tested over 10-second intervals. The test was not performed in production. The input reference noise was calculated by short-circuiting the input over 10-second intervals.

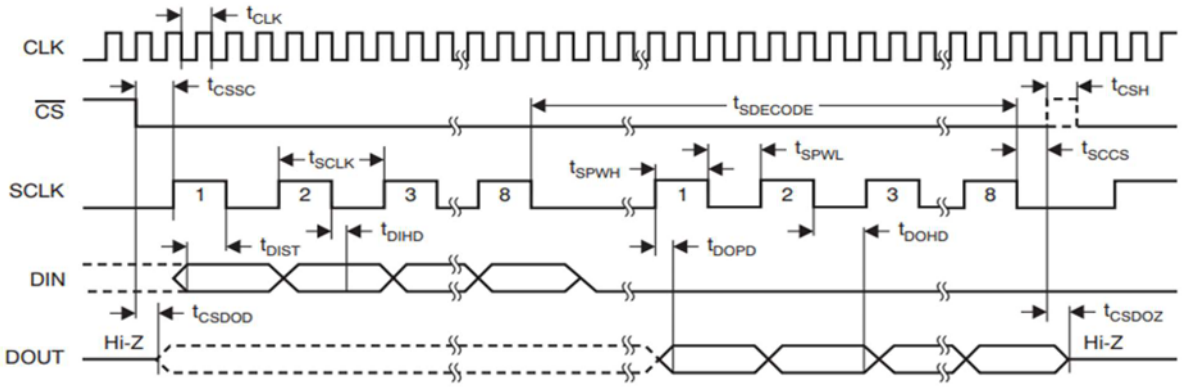
(3) CMRR is measured using a common-mode signal from AVSS + 0.3V to AVDD - 0.3V. The values shown are the maximum values for all eight channels.

7.5 Timing Requirements: SPI Serial Interface

		2.7V ≤ DVDD ≤ 3.6V			1.8V ≤ DVDD ≤ 2.0V			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CLK}	Master clock cycle	414		666	414		666	ns
t_{CSSC}	Delay time, from CS low level to the first SCLK		6			17		ns
t_{SCLK}	SCLK cycle		50			66.6		ns
$t_{SPWH, L}$	Pulse setup time, SCLK pulse duration, high or low level		15			25		ns
t_{DIST}	Setup time, DIN is valid for the falling edge of SCLK.		10			10		ns
t_{DIHD}	Hold time, DIN effective after the falling edge of SCLK		10			11		ns
t_{CSH}	Pulse duration, CS high		2			2		t_{CLK}
t_{SCCS}	The delay time is until the falling edge of SCLK reaches the high level of CS.		4			4		t_{CLK}
$t_{SDECODE}$	Command decoding time		4			4		t_{CLK}
$t_{DISCK2ST}$	Setup time, DAISY_IN is valid only on the rising edge of SCLK.		10			10		ns
$t_{DISCK2HT}$	Hold time: DAISY_IN is valid after the rising edge of SCLK.		10			10		ns

7.6 Switching Characteristics: SPI Serial Interface

Parameter		2.7V ≤ DVDD ≤ 3.6V			1.8V ≤ DVDD ≤ 2.0V			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{DOHD}	Hold time, from the falling edge of SCLK to the invalid DOUT	10			10			ns
t_{DOPD}	Propagation delay time, from the rising edge of SCLK to the valid DOUT			17			32	ns
t_{SDOD}	Propagation delay time, CS low level to DOUT drive	10			20			ns
t_{CSDOZ}	Propagation delay time, CS high to DOUT Hi-z			10			20	ns



Note: SPI is set to CPOL = 0 and CPHA = 1.

Figure 7.1 Serial Interface Timing

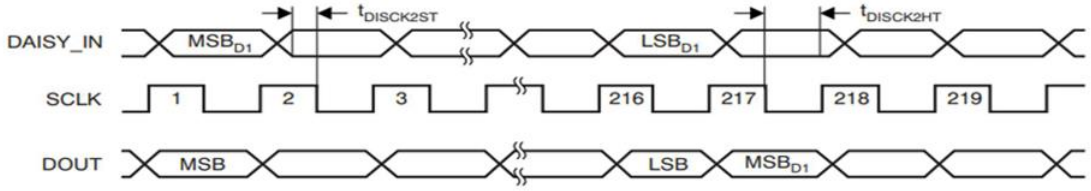


Figure 7.2 Daisy-Chain Interface Timing

8. Parameter Measurement Information

8.1 Noise Measurements

The noise performance of the DADS131E04/08 channels can be optimized by adjusting the data rate and PGA gain. Decreasing the data rate and increasing the PGA gain both result in a decrease in input noise. This is particularly useful for measuring weak bioelectric potential signals.

The table below shows the noise performance of the DADS131E08 measured using a 5V analog power supply and a 4.5V reference voltage. These data represent typical noise performance at TA = +25°C.

The displayed data is the result of averaging readings from multiple chips, measured with the input short-circuited. At least 1000 consecutive readings were used to calculate the value of each reading. RMS (μVRMS) and peak-to-peak (μVPP) noise. For lower data rates, the ratio of the two is approximately 6.6.

Table 8.1 Input reference noise (μVRMS , μVPP) under HR1/2=1 configuration VREF=4.5V

DR bit of CONFIG1 register	Output data rate (SPS)	PGA = 1		PGA = 2		PGA = 4		PGA = 6		PGA = 8		PGA = 12		PGA = 24	
		μV_{RMS}	μV_{PP}	μV_{RMS}	μV_{PP}	μV_{RMS}	μV_{PP}	μV_{RMS}	μV_{PP}	μV_{RMS}	μV_{PP}	μV_{RMS}	μV_{PP}	μV_{RMS}	μV_{PP}
010	16000	21.70	151.89	10.85	75.94	5.60	39.23	3.87	27.10	3.05	21.32	2.27	15.89	1.16	11.64
011	8000	6.93	48.53	3.65	25.52	1.98	13.87	1.31	9.19	1.11	7.80	0.92	6.41	0.80	5.57
100	4000	4.33	30.34	2.28	15.95	1.24	8.66	0.93	6.50	0.79	5.52	0.65	4.53	0.56	3.94
101	2000	3.06	6.13	1.61	11.29	0.88	6.13	0.66	4.60	0.56	3.90	0.46	3.20	0.40	2.79
110	1000	2.17	15.17	1.14	7.98	0.62	4.34	0.46	3.25	0.39	2.76	0.32	2.26	0.28	1.97

9. Detailed Description

9.1 Overview

The DADS131E04/08 is a low-noise, low-power, multi-channel, simultaneous sampling, 24-bit, delta - Σ analog-to-digital converter (ADC) chip that integrates a programmable gain amplifier (PGA) and various EEG-specific functions make them ideal for electrocardiogram (ECG) and electroencephalogram (EEG) applications. By shutting down the power supply to the EEG-specific circuitry, the chip can also be used for high performance, multi-channel data acquisition system.

This series of chips features a highly programmable multiplexer for temperature, power supply, input short circuit, and bias measurements. Furthermore, the multiplexer allows any input electrode to be programmed as a reference driver. PGA gain is selectable from seven settings (1, 2, 4, 6, 8, 12, and 24). The on-chip ADC provides data rates from 250 SPS to 64 kSPS. Chip communication is accomplished using an SPI-compatible interface, which provides four general purpose input/output (GPIO) pins. Multiple chips can be synchronized using the START pin.

An internal reference generates a low-noise 2.4V or 4.5V internal voltage, and an internal oscillator generates a 2.048MHz clock. Internal operational amplifiers can provide common-mode voltages for external measurements. Lead detection can be performed using a current source.

9.2 Functional Block Diagram

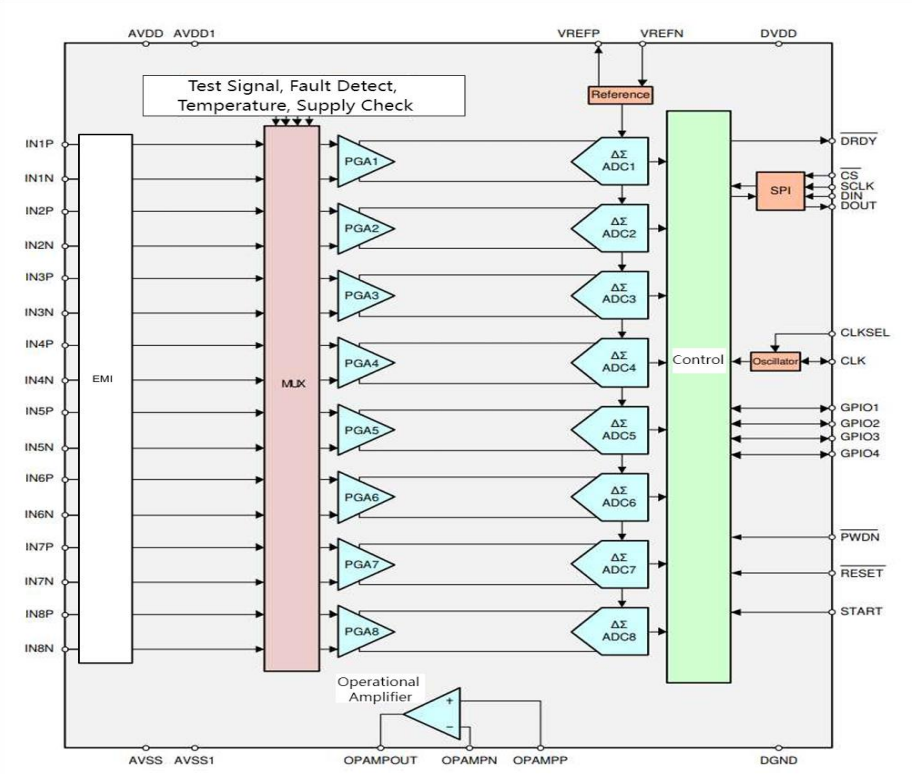


Figure 9.2.1 Overall block diagram of the chip

9.3 Functional Description

This section describes the internal functional information of the DADS131E04/08. Where f_{CLK} represents the CLK pin signal frequency, t_{CLK} represents the CLK pin signal period, f_{DR} represents the output data rate, and t_{DR} represents the output data time period, f_{MOD} represents the frequency at which the modulator samples the input.

9.3.1 Input Multiplexer

Each channel in the DADS131E04/08 has an input multiplexer (Figure 9.3.1) that provides flexible signal switching options through configuration.

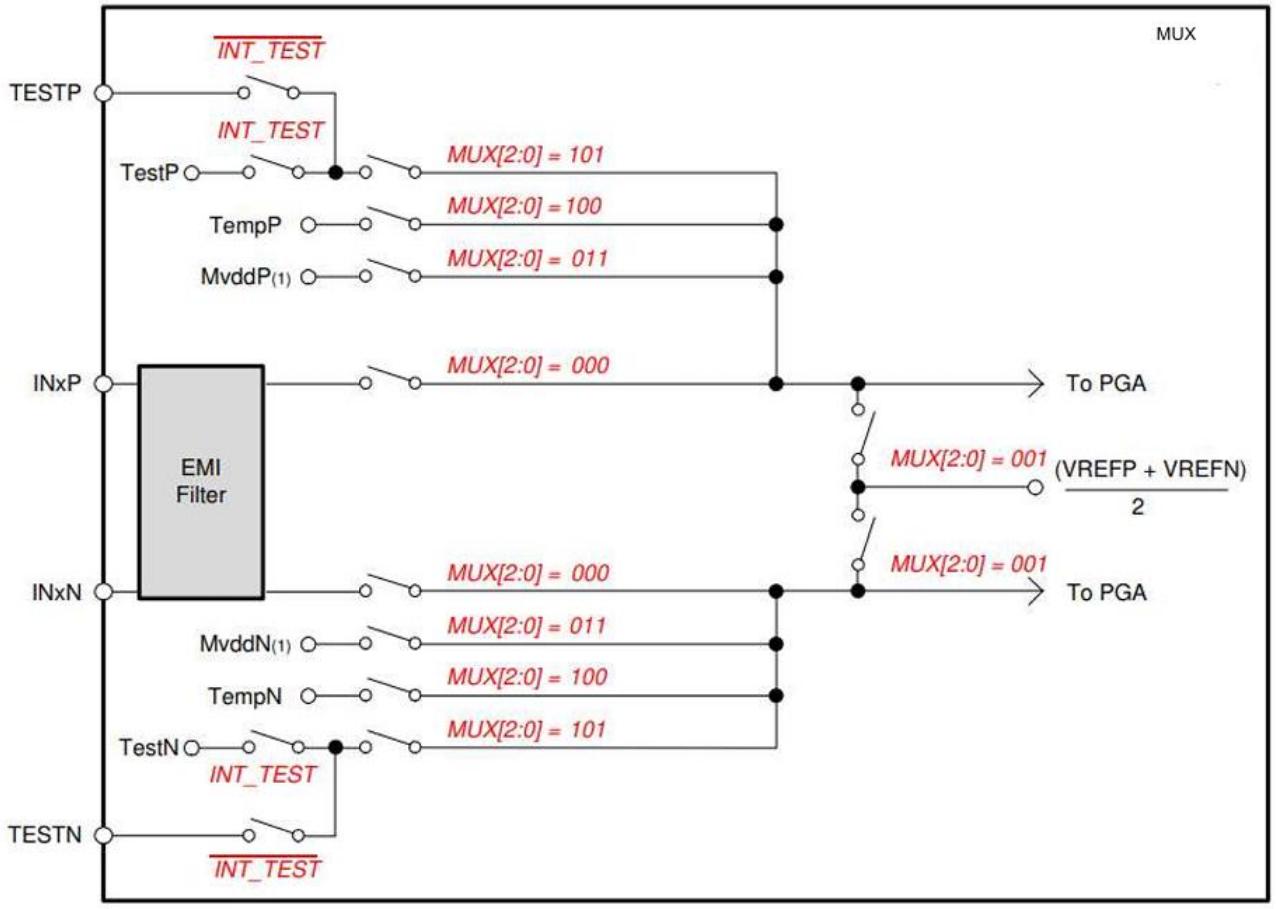


Figure 9.3.1 Multiplexer on the channel

(1) Chip noise measurement

Setting CHnSET[2:0]=001 shorts the P/N terminals of the channels and sets the common-mode voltage of [(VREFP + VREFN)/2] to the input of both channels. This setting can be used to test the inherent noise of the chip.

(2) Test signals (TestP and TestN)

Setting CHnSET[2:0]=101 allows the internally generated test signals to be introduced into the P/N terminals of the channel. For information on the internal test signals, please refer to the CONFIG2 register description.

(3) Temperature sensors (TempP and TempN)

The DADS131E04/08 contains an on-chip temperature sensor. This sensor uses two internal diodes, with the current density of one diode being 16 times that of the other, as shown in Figure 9.3.2. The difference in diode current density generates a voltage difference proportional to the absolute temperature. Due to the low thermal resistance of the package to the printed circuit board (PCB), the internal chip temperature is closely related to the PCB temperature. Please note that the self-heating of DADS131E04/08 will cause the internal temperature reading to be higher than the temperature of the surrounding PCB.

Setting CHnSET[2:0] = 100 can introduce the temperature sensor signal to the P/N terminals of the channel.

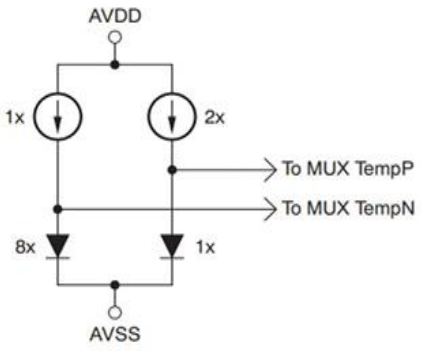


Figure 9.3.2 Temperature sensor measurement in the input

(4) Power measurement

Setting CHnSET[2:0]=011 will set the channel inputs to different power supply voltages of the chip. For channels 1, 2, 5, 6, 7, and 8, (MVDDP – MVDDN) is [0.5 × (AVDD + AVSS)].

For channels 3 and 4, (MVDDP – MVDDN) is DVDD/4.

To avoid PGA saturation when measuring the power supply, set the gain to 1.

9.3.2 Analog Input

The analog input of the chip is connected to a programmable gain amplifier with low noise, low drift and high input impedance through a multiplexer. The DADS131E04/08 analog input is fully differential.

The range of the differential input voltage (VINxP – VINxN) can be from –VREF/gain to VREF/gain. There are two methods to drive the DADS131E04/08 analog input: pseudo-differential or full differential, as shown in Figure 9.3.3.

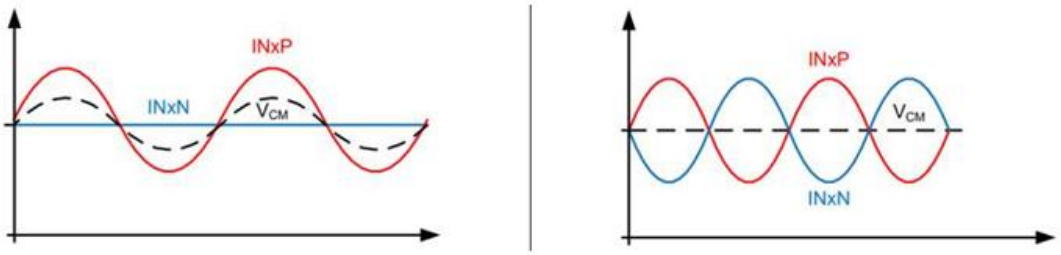


Figure 9.3.3 Pseudo-difference (left) and fully-difference (right) driving methods

Keep the INxN pins at a common voltage, preferably at the intermediate power supply, which is the pseudo-differential input mode. Swing the INxP pins around the common voltage VREF/gain to VREF/gain and keep them within the absolute maximum specification range. When the input is configured in the pseudo-differential mode, the common-mode voltage (VCM) will change with the signal level. It is necessary to ensure that the differential signal at the minimum and maximum points meets the common-mode input specification.

Configure the signals on INxP and INxN as reverse signals centered around the common-mode voltage (VCM), which is the full-differential input method. Both INxP and INxN inputs swing from the common voltage +½ VREF/gain to the common voltage –½ VREF/gain. The differential voltage at the maximum and minimum points is equal to –VREF/gain to VREF/gain, and centered around a fixed common-mode voltage. To achieve the best performance, it is recommended to set the common-mode voltage at the midpoint of the analog power supply, that is, [(AVDD + AVSS)/2].

9.3.3 PGA Settings and Input Range

The low-noise PGA is a differential input and output amplifier, and the gain settings (1, 2, 4, 6, 8, 12, and 24) can be configured by writing to CHnSET. The DADS131E04/08 uses CMOS inputs, so current noise is negligible. Table 9.3.1 shows typical bandwidth values for various gain settings.

Please note that the table shows the bandwidth for small signals. For large signals, performance is limited by the PGA slew rate.

Table 9.3.1 PGA Gain versus Bandwidth

Gain	Nominal bandwidth (kHz) at room temperature
1	662
2	332
4	165
6	110
8	83
12	55
24	27

To maintain the PGA within its linear operating range, the input signal must satisfy the following:

$$AVDD - 0.2\ V - \left(\frac{Gain \times V_{MAX\_DIFF}}{2}\right) > CM > AVSS + 0.2\ V + \left(\frac{Gain \times V_{MAX\_DIFF}}{2}\right)$$

Where VMAX_DIFF = PGA input maximum differential voltage; CM = common-mode range. For example: if AVDD = 5 V, Gain = 12, VMAX_DIFF = 350 mV, then, 2.3 V < CM < 2.7 V. The differential input voltage range (VINxP – VINxN) depends on the analog power supply and reference voltage used in the system as well as the gain, ranging from –VREF / gain to VREF / gain.

9.3.4 Δ – Σ Modulator

Each channel in the DADS131E04/08 has a 24-bit ΔΣ ADC. This converter uses a second-order modulator optimized for low-noise applications. The modulator samples the input signal at a rate of (f_{MOD} = f_{CLK} /2), and the chip noise is shaped until it reaches f_{MOD} /2, as shown in Figure 9.3.4.

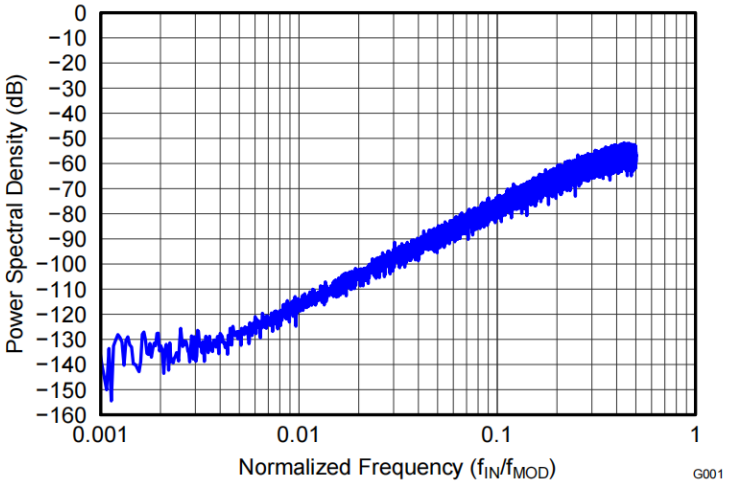


Figure 9.3.4 Modulator noise spectrum

9.3.5 Reference Voltage

The DADS131E04/08 internally generates a reference voltage, typically 4.5V or 2.4V (based on AVSS), controlled by the VREF_4V bit in the CONFIG3 register. When using the internal reference voltage, connect VREFN to AVSS. This disables the internal reference buffer and applies an external reference to VREFP. Figure 9.3.5 shows a typical external reference drive circuit. The internal reference circuit can be powered off by setting the PD_REFBUF bit in the CONFIG3 register. When multiple chips are cascaded, the internal reference of a certain chip can be shared by powering it off. By default, the chip uses the external reference after waking up.

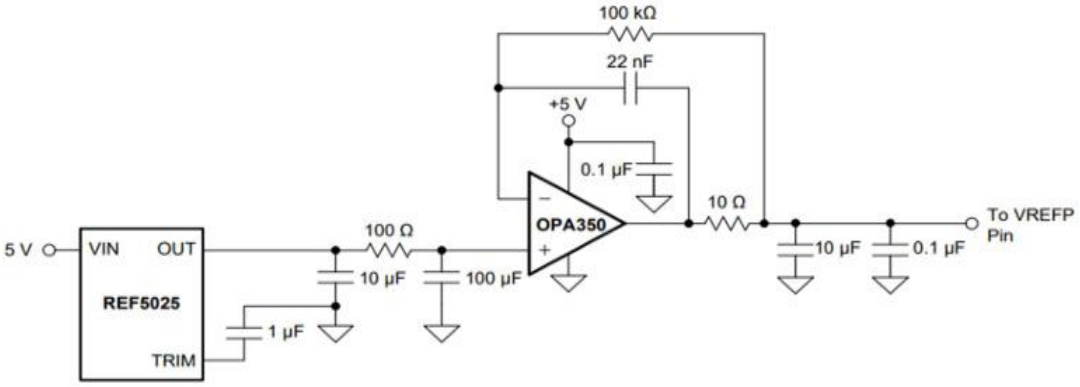


Figure 9.3.5 External Reference Driver

9.3.6 Digital Decimation Filter

The digital filter receives the output of the modulator and extracts the data stream. By adjusting the filtering parameters, a trade-off can be made between resolution and data rate: the more filtering is applied, the higher the resolution can be achieved; the less filtering is applied, the higher the data rate can be achieved. Higher data rates are typically used for detecting the detachment of the AC leads in EEG applications. The digital filter on the channel consists of a third-order sinc filter. The extraction ratio of the sinc filter can be adjusted through the DR bit in the CONFIG1 register. This setting is a global setting that affects all channels, so all channels in the chip operate at the same data rate. This sinc filter is a variable extraction rate third-order low-pass filter. The data is input to the filter in parallel from the modulator at the rate of f_{MOD}. The Z-domain transfer function of the sinc filter (N is the sampling rate) is as follows:

$$|H(z)| = \left| \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3$$

Figure 9.3.6/7 shows the transmission characteristics of the filter, with the horizontal axis representing the normalized frequency and the vertical axis representing the gain (dB).

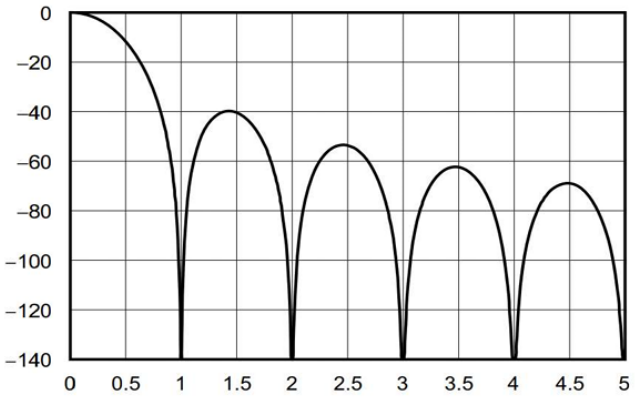


Figure 9.3.6 sinc transmission characteristics (frequency normalized to f_{IN}/f_{DR})

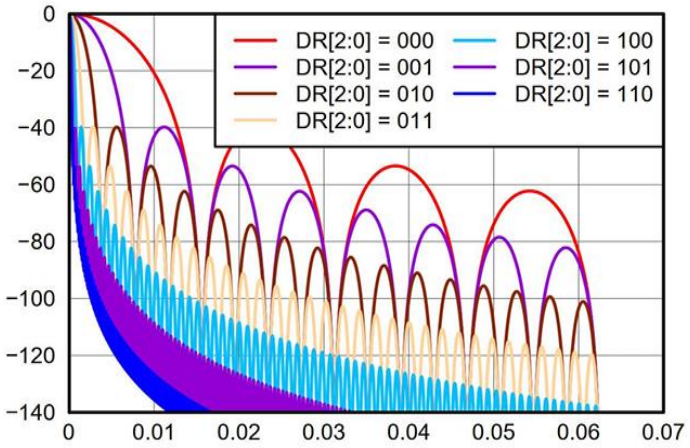


Figure 9.3.7 sinc transmission characteristics (frequency normalized to f_{IN}/f_{DR})

9.3.7 Clock

DADS131E04/08 provides both internal and external clock methods. The internal clock is suitable for low-power, battery-powered systems. The internal oscillator is adjusted at room temperature to ensure accuracy. The clock selection is controlled by the CLKSEL pin and the bits of the CLK_EN register.

The CLKSEL pin selects the internal or external clock. The CLK_EN bit in the CONFIG1 register enables and disables the oscillator clock to be output on the CLK pin. The truth table for these two pins is shown in Table 9.3.2.

Table 9.3.2 CLKSEL Pin and CLK_EN Bit

CLKSEL	CONFIG1.CLK_EN	Clock source	Clock pin status
0	X	external clock	Input: External clock
1	0	Internal oscillator	Three states
1	1	Internal oscillator	Output: Internal oscillator

9.3.8 General-Purpose Digital I/O(GPIO)

The DADS131E04/08 has four general purpose digital I/O (GPIO) pins available in normal operating mode. These GPIO pins can be individ-

ually configured as inputs or outputs via the GPIOC bit register.

The GPIOD bit in the GPIO register controls the pin level. When reading the GPIOD bit, the returned data is the pin's logic level, regardless of whether it is programmed as an input or output. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output level.

9.4 Device Functional Modes

9.4.1 Start(START)

Pull the START pin high for at least 2 tCLK cycles, or send the START command to start the analog-to-digital conversion. When the START pin is low and no START command has been sent, the chip will not generate the DRDY_ signal (the conversion is paused). When controlling the conversion using the START command, keep the START pin at a low level. The DADS131E04/08 has two modes for controlling the conversion: continuous mode and single-shot mode, which is selected by SINGLE_SHOT (the 3rd bit of the CONFIG4 register). In multi-chip configurations, the START pin is used for synchronizing the chips.

The settling time (tSETTLE) is the time required for the output to stabilize completely after the start of the analog-to-digital conversion. When START is raised, DRDY_ is also raised.

The next falling edge of DRDY_ indicates that the data is ready. Figure 9.4.1 shows the timing diagram, and Table 9.4.1 lists the settling times for different data rates. The settling time depends on fCLK and the downsampling rate (controlled by the DR[2:0] bits in the CONFIG1 register). After the initial settling time, DRDY_ drops, indicating that the data conversion is complete and the data rate tDR appears. If no

data is read back on DOUT before the next data is ready, DRDY_ goes high for 4 tCLK and then returns to the low level to indicate that new data is ready. Please note that when START remains at a high level and the input signal undergoes a step change, the filter needs 3×tDR to stabilize at the new value. The stable data is ready at the fourth falling edge of DRDY_.

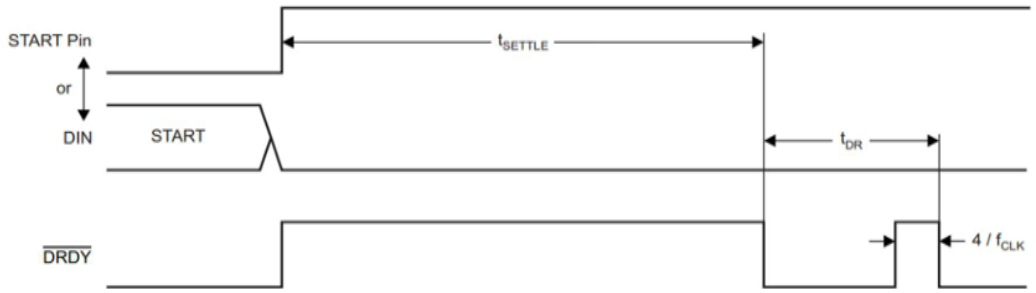


Figure 9.4.1 Settling Time

Table 9.4.1 Setup time for different data rates

DR[2:0]	Normal mode	Unit
000	521	t_{CLK}
001	1033	t_{CLK}
010	2057	t_{CLK}
011	4105	t_{CLK}
100	8201	t_{CLK}
101	16393	t_{CLK}
110	32777	t_{CLK}

9.4.2 Reset (RESET__)

There are two ways to reset the DADS131E04/08: by pulling the RESET_ pin low, or by sending the RESET command. When using the

RESET_ pin, make sure to follow the minimum pulse duration timing specification before pulling the pin back to high level. The RESET command takes effect on the 8th SCLK falling edge of the command. After the reset, it takes 18 t_{CLK} cycles to complete the initialization of the configuration registers to the default state and start the conversion cycle. Please note that when using the WREG command to set the CONFIG1 register to a new value, an internal reset will be automatically sent to the digital filter.

9.4.3 Power outage (PWDN__)

When PWDN_ is pulled down, all on-chip circuits are turned off. To exit the power-down mode, pull the PWDN_ pin high. After exiting the power-down mode, the internal oscillator and reference require time to wake up. During the power-down period, it is recommended to turn off the external clock to save power.

9.4.4 Data Acquisition

(1) Data ready (DRDY_)

DRDY_ is an output signal that transitions from a high level to a low level, indicating that new conversion data is ready. The CS_ signal has no effect on the data ready signal. The behavior of DRDY_ depends on whether the chip is in the RDATAC mode or is reading data on demand using the RDATA command. When reading data using the RDATA command, the read operation can overlap with the next occurrence of DRDY_ without damaging the data. The START pin or the START command places the chip in the normal data capture mode or the pulse data capture mode.

Figure 9.4.2 shows the relationship between DRDY_, DOUT and SCLK during data reading. DOUT is latched on the rising edge of SCLK. DRDY_ is pulled high on the falling edge of SCLK. Please note that whether reading data or sending commands through the DIN pin,

DRDY_ will become high on the first falling edge of SCLK.

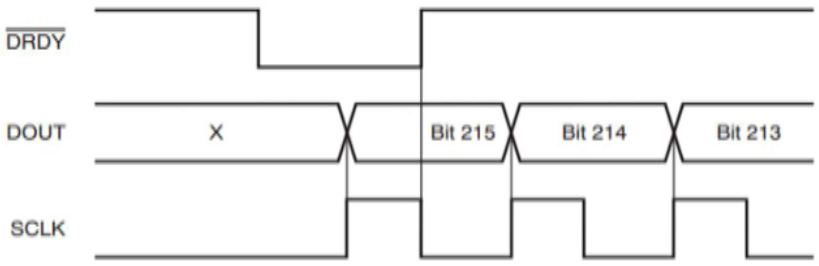


Figure 9.4.2 DRDY_ with data retrieval (CS = 0)

(2) Data reading

Data reading can be accomplished using one of the following two methods:

1. RDATAC: Continuous Read Data command sets the chip to continuous read mode. New data is automatically loaded into the output shift register after each data conversion without sending a command. For more details, see the RDATAC: Continuous Read Data section.

2. RDATA: Read Data command requires sending a command to the chip to load the latest data into the output shift register. For more details, see the RDATA: Read Data section.

Converted data is read by shifting data out on DOUT. The MSB of the data on DOUT is output on the rising edge of the first SCLK. DRDY_ returns high on the falling edge of the first SCLK. DIN should remain low for the entire read operation. The number of bits in the data output depends on the number of channels and the number of bits per channel. For an 8-channel DADS131E04/08, the number of data outputs is [(24 status bits + 24 bits × 8 channels) = 216 bits].

The 24 status bits are formatted as follows: (1100 + LOFF_STATP + LOFF_STATN + bits [4:7] of the GPIO register).

The data format for each channel is MSB-first two's complement. When a channel is closed using a user register setting, the correspond-

ing channel output is set to "0". However, the channel output order remains unchanged.

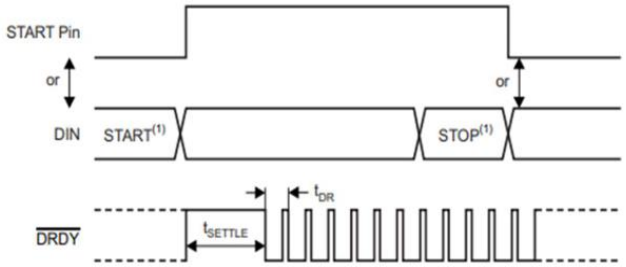
The DADS131E04/08 also provides multiple readback functionality. Data can be read multiple times by simply providing more SCLKs in RDATAC mode, in which case the MSB data byte is repeated after the last byte is read. For multiple readbacks, the DAISY_EN_ bit in the CONFIG1 register must be set to "1".

9.4.5 Continuous Conversion Mode

The conversion begins when the START pin is pulled high or a START command is sent. As shown in 9.4.3, the DRDY_ output goes high at the start of the conversion and low when the data is ready. The conversion will continue indefinitely until the START pin goes low or a STOP command is sent. Pulling the START pin low or issuing a STOP command allows the ongoing conversion to complete.

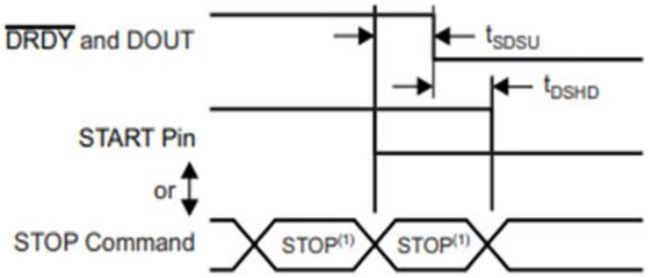
Figure 9.4.4 and Table 9.4.2 illustrate the timing of the START pin or START and STOP commands to the DRDY_ signal during data conversion. t_{SDSU} indicates when to pull the START pin low or when to send a STOP command before the falling edge of DRDY_ to stop further conversion. t_{DSHD} indicates when to pull the START pin low or when to send a STOP command after the falling edge of DRDY_ to complete the current conversion and stop further conversion. To keep the converter running continuously, the START pin can be held high.

When switching from Single-Shot mode to continuous conversion mode, the START signal is pulled low and then high, or a STOP command is sent followed by a START command. This conversion mode is suitable for applications requiring constant continuous conversion.



(1) The START and STOP commands take effect on the 7th falling edge of SCLK.

Figure 9.4.3 Continuous Conversion Mode



(1) The START and STOP commands take effect on the seventh falling edge of SCLK after the command ends.

Figure 9.4.4 Timing from START to DRDY

Table 9.4.2 Timing Characteristics

	Min	Unit
The START pin of t_{SDSU} stops further conversion when it is low or holds for the duration of the STOP command to DRDY	16	t_{CLK}
The time from when the t_{DSHD} START pin is low or a STOP command is given until the current conversion is complete	16	t_{CLK}

9.4.6 Single-Shot Mode

Single-shot mode is enabled by setting the SINGLE_SHOT bit in the CONFIG4 register to "1". In single-shot mode, the DADS131E04/08 performs one conversion when the START pin is pulled high or a START command is sent. As shown in Figure 9.4.5, after the conversion is complete, DRDY_ goes low and stops further conversions. DRDY_ remains low regardless of whether conversion data is read. To start a new conversion, pull the START pin low and then high, or send the START command again. To switch from continuous conversion mode to single-shot mode, pull the START signal low and then high, or send a STOP command followed by a START command.

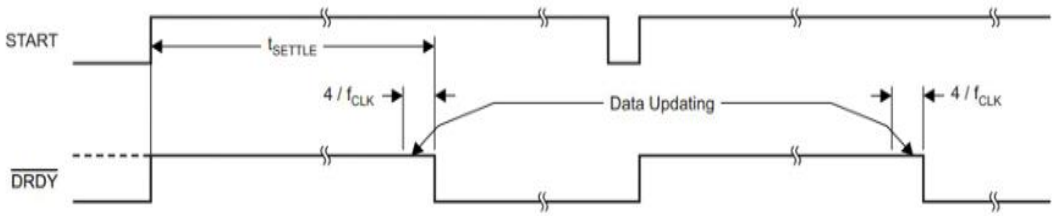


Figure 9.4.5 DRDY_ No data recovery in SINGLE-SHOT mode

This conversion mode is suitable for applications that require non-standard or non-continuous data rates. By issuing the START command or switching the START pin to a high level, the digital filter is reset, effectively reducing the data rate by four times. This mode increases the load on the host processor because the processor must switch the START pin or send the START command to initiate a new conversion cycl

9.5 Programming

9.5.1 Data Format

The chip's 24-bit data is represented in two's complement format. The voltage magnitude (LSB) represented by a least significant bit is calculated using the following equation:

$$1\ LSB = (2 \times V_{REF} / gain) / 2^{24} = +FS / 2^{23}$$

A positive full-scale input produces an output code of 7FFFFFh, and a negative full-scale input produces an output code of 800000h. For signals exceeding the full-scale range, the output is clipped at these codes. The table below summarizes the ideal output codes for different input signals.

Table 9.5.1 Ideal Output Code and Input Signal

Input signal, VIN(INxP – InxN)	Ideal output code
≥FS	7FFFFFh
+FS/ $(2^{23} – 1)$	000001h

0	000000h
- FS/ $(2^{23} - 1)$	FFFFFFh
$\leq FS/(2^{23}/(2^{23} - 1))$	800000h

9.5.2 SPI Interface

The SPI-compatible serial interface consists of four signals: CS_, SCLK, DIN, and DOUT, used to read converted data, read and write registers, and control the operation of the DADS131E04/08.

The data-ready output DRDY_ is used as a status signal to indicate when data is ready. DRDY_ goes low when new data is available.

(1) Chip Select (CS_)

The CS_ pin activates SPI communication. CS_ must be low before data transmission and must remain low for the entire SPI communication cycle. When CS_ is high, the DOUT pin enters a high-impedance state. Therefore, reads and writes to the serial interface are ignored, and the serial interface is reset. The DRDY_ pin operates independently of CS_. Even when CS_ is high, DRDY_ still indicates that a new transition has been completed and is forced high in response to SCLK.

Setting CS_ high will stop SPI communication and reset the serial interface. Data conversion continues, and the DRDY_ signal can be monitored to check if a new conversion result is ready.

The master device monitoring the DRDY_ signal can select the appropriate slave chip by pulling the CS_ pin low. After serial communication is complete, four or more tCLK cycles must be waited before pulling CS_ high.

(2) Serial clock (SCLK)

SCLK provides the clock for serial communication. SCLK is a Schmitt trigger input, but it is recommended to keep SCLK as noise-free as possible to prevent glitches from unintentionally shifting data. Data is shifted into DIN on the falling edge of SCLK and out of DOUT on the rising edge.

When using SCLK shift commands, ensure that all SCLK clocks are sent to the chip. Failure to do so may cause the chip's SPI serial interface to enter an unknown state, requiring CS_ to be pulled high to recover.

For a single chip, the minimum required SCLK speed depends on the number of channels, resolution bit depth, and output data rate. For multiple cascaded chips, the SCLK clock frequency needs to ensure that data from all channels can be read within the data ready interval. Data acquisition can be accomplished by putting the chip into RDATAC mode or by issuing the RDATA command.

(3) Data Input (DIN)

DIN, along with SCLK, is used to send data to the chip. Data on DIN is shifted into the chip on the falling edge of SCLK.

The chip's communication is inherently full-duplex. Even while data is being shifted out, the chip monitors the commands being shifted in. When a command is sent, the data present in the output shift register is shifted out.

Therefore, when shifting out data, ensure that anything sent to the DIN pin is valid. To read data without sending a command to the chip, send a NOP command on DIN.

(4) Data Output (DOUT)

DOUT is used in conjunction with SCLK to read conversion data and register data from the chip. Data is output on the rising edge of SCLK, MSB first. When CS_ is high, DOUT enters a high-impedance state. Figure 9.5.1 illustrates the DADS131E04/08 data output protocol.

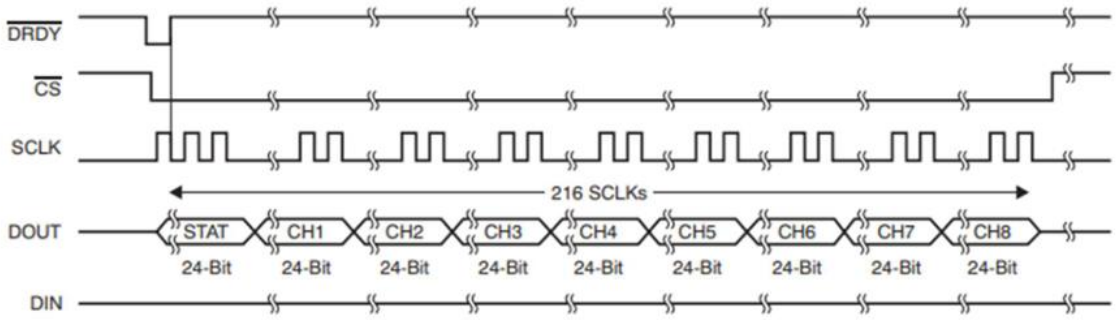


Figure 9.5.1 SP bus data output

9.5.3 SPI Command Definition

The DADS131E04/08 provides flexible configuration control. Table 10 lists the command control and configuration chip operations. Except for register read and write operations, which require data to be added to the second command byte, other commands are independent. CS_ can be pulled high or held low between commands, but must remain low throughout the entire command operation (especially for multi-byte commands). System commands and RDATA commands are decoded by the chip on the seventh falling edge of SCLK. Register read and write commands are decoded on the eighth falling edge of SCLK. When pulling CS_ high after issuing a command, be sure to follow the SPI timing requirements.

Table 10 Command Definitions

Command	Description	First byte	The second byte
System commands			
NOP	No operation	00000000 (00h)	
WAKEUP	Wake up from standby mode	00000010 (02h)	
STANDBY	Enter standby mode	00000100 (04h)	
RESET	Reset/Reset the device	00000110 (06h)	
START	Startup and restart (synchronous) conversion	00001000 (08h)	

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STOP	Stop conversion	00001010 (0Ah)	
OFFSETCAL	Channel offset calibration	00011010 (1Ah)	
Data read commands			
RDATAC	Enable continuous data reading mode. This is the default mode after power-on. (1)	00010000 (10h)	
SDATAC	Stop continuous data reading mode	00010001 (11h)	
RDATA	Data can be read via commands; multiple readbacks are supported.	00010010 (12h)	
Register read commands			
PREG	Read n registers starting from address r rrrr.	001r rrrr (2xh) (2)	000n nnnn (2)
WREG	Write n registers starting from address rrrrr.	010r rrrr (4xh) (2)	000n nnnn (2)

(1) In RDATAC mode, the RREG command is ignored.

(2) n nnnn = the number of registers to read or write – 1. For example, to read or write three registers, set n nnnn = 0 (0010). r rrrr = the starting register address for the read or write command.

(1) Send multi-byte command

The DADS131E04/08 serial interface decodes commands byte-by-byte, requiring 4 t_{CLK} cycles for decoding and execution. Therefore, when sending multi-byte commands (such as RREG or WREG), the end of one byte (or command) must be separated from the end of the next byte (or command) by 4 t_{CLK} cycles.

Assuming a CLK of 2.048 MHz, $t_{SDECODE}$ (4 t_{CLK}) is 1.96 μs. When SCLK is 16 MHz, one byte can be transmitted in 500 ns (0.5 μs). This byte transmission time does not conform to the $t_{SDECODE}$ specification; therefore, a delay must be inserted so that the end of the second byte arrives 1.46 μs later. If SCLK is 4 MHz, one byte is transmitted in 2 μs. Since this transmission time exceeds the $t_{SDECODE}$ specification, the processor can send subsequent bytes without delay.

(2) WAKEUP: Exit standby mode

The WAKEUP command exits low-power standby mode. This command has no SCLK rate limit and can be sent at any time. Any subsequent commands must be sent after a 4 t $_{CLK}$ cycle delay.

(3) STANDBY: Enter standby mode

The STANDBY command enters low-power standby mode. All parts of the circuit, except the reference section, are powered off. This command has no SCLK rate limit and can be issued at any time. Once the chip is in standby mode, do not send any commands other than the wake-up command.

(4) RESET: Resets the register to its default value

The RESET command resets the digital filter cycle and returns all register settings to their default values. This command has no SCLK rate limit and can be issued at any time. Executing the RESET command requires 18 t_{CLK} cycles; avoid sending any commands during this period.

(5) START: Start the conversion

The START command initiates data conversion. The START pin must be pulled low to control the conversion via command. This command is invalid if conversion is in progress. The STOP command stops conversion.

If a START command is immediately followed by a STOP command, there must be a 4 t_{CLK} cycle delay between them. When sending a START command to the chip, keep the START pin low until a STOP command is issued. This command has no SCLK rate limit and can be issued at any time.

(6) STOP: Stop the conversion

The STOP command stops the conversion. Pull the START pin low to control the conversion via command. When the STOP command is sent, the ongoing conversion completes and stops further conversion. If the conversion has already stopped, this command has no effect. This command has no SCLK rate limit and can be issued at any time.

(7) RDATAC: Continuous data reading

The RDATAC command initiates the conversion data output on each DRDY_ pulse without issuing a subsequent read command. This mode places the conversion data in the output register, which can be directly shifted out. Continuous read mode is the chip's default mode, activated by power-on.

RDATAC mode is canceled by the stop read command. If the chip is in RDATAC mode, an SDATAC command must be issued before any other commands can be sent to the chip. This command has no SCLK rate limit; however, subsequent data read SCLK or SDATAC command should wait at least 4 tCLK cycles before completion (see the Send Multibyte Commands section).

The RDATAC timing is shown in Figure 9.5.2. There is a 4 tCLK cycle forbidden region around the DRDY_ pulse where this command cannot be issued. To read data from the chip after issuing an RDATAC command, ensure the START pin is high or issue a START command.

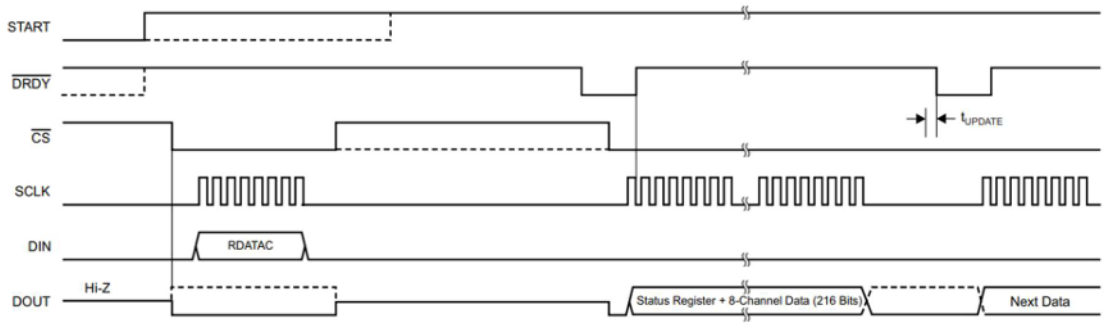

Figure 9.5.2 Usage of the RDATAC command

(8) SDATAC: Stop reading data continuously

The SDATAC command cancels continuous data reading mode. This command has no SCLK rate limit, but the next command must wait for 4 t_{CLK} cycles to complete.

(9) RDATA: Read data

When not in continuous read mode, the RDATA command loads the latest data into the output shift register. This command is issued after DRDY_ goes low to read the conversion result. This command has no SCLK rate limit; subsequent commands or data reads do not require a wait time on the SCLK. To read data from the chip after issuing the RDATA command, ensure the START pin is high or issue the START command. When using the RDATA command to read data, the read operation can overlap with the next DRDY_ without corrupting the data.

Figure 9.5.3 illustrates the usage of the RDATA command.

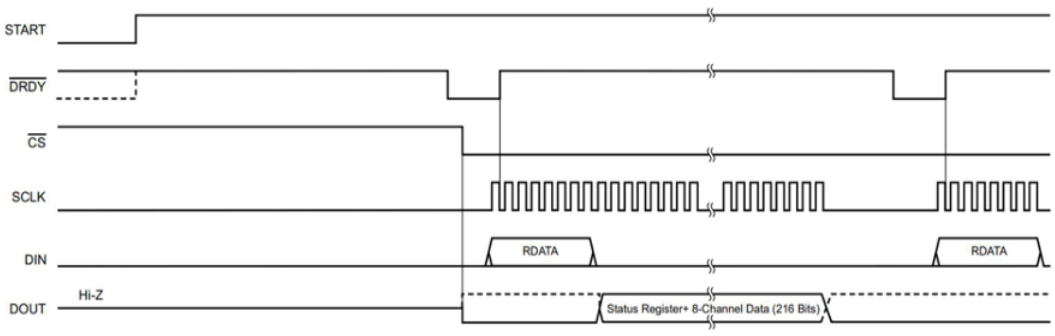

Figure 9.5.3 Usage of the RDATA command

(10) RREG: Read data from register

This command reads register data. The register read command is a two-byte command followed by the register data output. The first byte contains the command and the register address. The second command byte specifies the number of registers to read – 1.

First command byte: 001r rrrr, where r rrrr is the starting register address.

Second command byte: 000n nnnn, where n nnnn is the number of registers to read – 1.

The MSB of the first register is output on the 17th rising edge of SCLK, as shown in Figure 9.5.4. When the chip is in continuous read mode, the SDATAC command must be issued before the RREG command can be issued. The RREG command can be issued at any time. However, because this command is a multi-byte command, the issuance of SCLK must satisfy the tSDECODE timing, thus there is an SCLK rate limit. Note that CS_ must be low throughout the entire command.

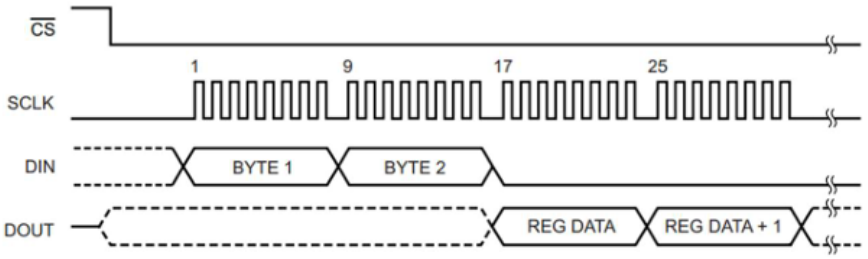

Figure 9.5.4 Example of the RREG command:

Read two registers starting from register 00h (ID register): BYTE1 = 0010 0000, BYTE2 = 00000001.

(11) WREG: Data written to register

This command writes data to a register. The register write command is a two-byte command followed by the register data input. The first byte contains the command and the register address.

The second command byte specifies the number of registers to write to -1.

First command byte: 010r rrrr, where r rrrr is the starting register address.

Second command byte: 000n nnnn, where n nnnn is the number of registers to write to -1.

Following the command bytes is the register data (MSB priority format), as shown in Figure 9.5.5. The WREG command can be issued at any time; however, because it is a multi-byte command, the issuance of SCLK must satisfy the tSDECODE timing, thus there is an SCLK rate limit. Note that CS_ must be low throughout the entire command.

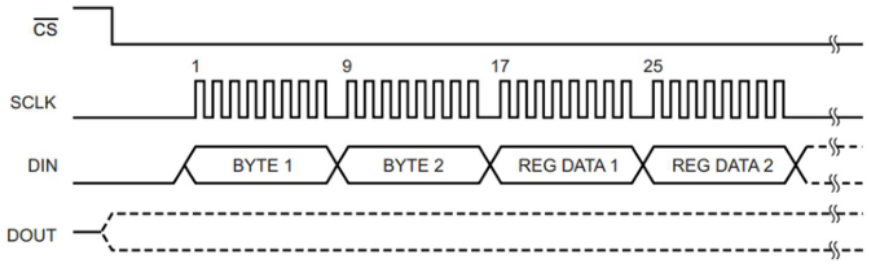

Figure 9.5.5 Example of the WREG command:

Write two registers starting from 00h (ID register): BYTE 1 = 0100 0000, BYTE2 = 0000 0001.

9.6 Register Definition

Table 9.6.1 describes the various DADS131E04/08 registers.

Table 9.6.1 Register Allocation

Address	Register	Default settings	Register bits							
			7	6	5	4	3	2	1	0
Read-only ID register										
00h	ID	xxh	REV_ID[2:0]			1	DEV_ID[1:0]		NU_CH[1:0]	
Global settings										
01h	CONFIG1	06h	HR1	DAISY_EN_	CLK_EN	HR2	0	DR[2:0]		
02h	CONFIG2	40h	0	1	0	INT_TEST	0	TEST_AMP0	TEST_FREQ[1:0]	
03h	CONFIG3	40h	PD_REFBUF_	1	VREF_4V	0	OPAMP_REF	PDB_OPAMP	0	0
04h	FAULT	00h	COMP_TH[2:0]			0	00		00	
Channel settings										
05h	CH1SET	61h	PD1	GAIN1[2:0]			0	MUX1[2:0]		
06h	CH2SET	61h	PD2	GAIN2[2:0]			0	MUX2[2:0]		
07h	CH3SET	61h	PD3	GAIN3[2:0]			0	MUX3[2:0]		
08h	CH4SET	61h	PD4	GAIN4[2:0]			0	MUX4[2:0]		
09h	CH5SET	61h	PD5	GAIN5[2:0]			0	MUX5[2:0]		
0Ah	CH6SET	61h	PD6	GAIN6[2:0]			0	MUX6[2:0]		
0Bh	CH7SET	61h	PD7	GAIN7[2:0]			0	MUX7[2:0]		
0Ch	CH8SET	61h	PD8	GAIN8[2:0]			0	MUX8[2:0]		
Fault detection status register (read-only)										
12h	FAULT_STATP	00	IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT
13h	FAULT_STATN	00	IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT
GPIO settings										
14h	GPIO	0F	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

9.6.1 ID Control Register (Address = 00h) (Reset = xxh)

Table 9.6.1 ID Control Register

7	6	5	4	3	2	1	0
REV_ID[2:0]			1	DEV_ID[1:0]		NU_CH[1:0]	
R-xh			R-1h	R-3h		R-xh	

Note: R/W = Read/Write; R = Read-only; -n = Reset value

Table 9.6.2 Description of ID Control Register Fields

Bit	Fields	Type	Reset	Description
7:5	REV_ID[2:0]	R	xh	**Reserved.** These bits indicate the chip version and are subject to change without notice.
4	Reserved	R	1h	**Reserved.** Always read back to 1.
3:2	DEV_ID[1:0]	R	0h	**Chip identifier. These bits indicate the chip type.** 00 : DADS131E0X
1:0	NU_CH[1:0]	R	xh	**Number of channels. These bits indicate the number of channels.** 00 : 4-channel DADS131E04 10 : 8-channel DADS131E08

9.6.2 CONFIG1: Configuration Register 1 (Address = 01h) (Reset = 06h)

This register configures the DAISY_EN_ bit, clock, and data rate.

Table 9.6.3 CONFIG1: Configuration Register 1

7	6	5	4	3	2	1	0
HR1	DAISY_EN_	CLK_EN	HR2	0	DR[2:0]		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-6h		

Note: R/W = Read/Write; R = Read-only; -n = Reset value

Table 9.6.4 Description of Fields in Configuration Register 1

Bit	Fields	Type	Reset	Description
7	HR1	R/W	0h	**High sampling rate or low power mode 1** This bit determines whether the chip operates in low-power mode or high-sampling-rate mode. 0 = Low Power LP Mode 1 = High Sampling Rate (HR) Mode
6	DAISY_EN_	R/W	0h	**Daisy chain or multiple readback mode** 0 : Daisy Chain Mode 1: Multiple readback mode
5	CLK_EN	R/W	0h	**Clock connection** (1) When the CLKSEL pin is 1, this bit determines whether the internal oscillator signal is connected to the CLK pin. 0: Oscillator clock output disabled 1: Oscillator clock output enabled
4	HR2	R/W	0h	**High sampling rate or low power mode 2** This bit determines whether the chip operates in low-power mode or high-sampling-rate mode. 0 = Low Power LP Mode 1 = High Sampling Rate (HR) Mode
3	Reserve	R/W	0h	**Reserve**
2:0	DR[2:0]	R/W	6h	**Output data rate** HR1/2 and DR determine the chip's output data rate. For HR1=1 and HR2=1, $f_{MOD} = f_{CLK}/2$; for HR1/2=1 and HR2/1=0, $f_{MOD} = f_{CLK}/4$; for HR1=0 and HR2=0, $f_{MOD} = f_{CLK}/8$. DR determines f_{MOD} . The frequency division is based on the data sampling rate as follows: 000: $f_{MOD}/16$ (up to 64kSPS)

				001:f_{MOD}/32 010:f_{MOD}/64 011:f_{MOD}/128 100:f_{MOD}/256 101:f_{MOD}/512 110:f_{MOD}/1024 (minimum 250 SPS) 111: Reserved (not used)

(1) It consumes additional power when driving external chips.

9.6.3 CONFIG2: Configuration Register 2 (Address = 02h) (Reset = 40h)

This register is primarily configured to generate test signals.

Table 9.6.5 CONFIG2: Configuration Register 2

7	6	5	4	3	2	1	0
0	1	0	INT_TEST	0	TEST_AMP	TEST_FREQ[1:0]	
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Note: R/W = Read/Write; R = Read-only; -n = Reset value

Table 9.6.6 Description of Fields in Configuration Register 2

Bit	Fields	Type	Reset	Description
7:6	Reserve	R/W	1h	**Reserve**
5	Reserve	R/W	0h	**Reserve**
4	INT_TEST	R/W	0h	**Test source.** This bit determines the source of the test signal. 0: Oscillator clock output disabled 1: Oscillator clock output enabled
3	reserve	R/W	0h	**Reserve** Always write 0h
2	TEST_AMP	R/W	0h	**Test signal amplitude** 0 : 1 x (VREFP – VREFN) / 2400 1: 2 x (VREFP – VREFN) / 2400
1:0	TEST_FREQ[1:0]	R/W	0h	**Output data rate** 00: In f_{CLK} / 2^{21} pulse 01: In f_{CLK} /2^{20} pulses 10: Not used 11: DC

(1) It consumes additional power when driving external chips.

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9.6.4 CONFIG3 : Configuration Register 3 (Address = 03h) (Reset = 40h)

This register is primarily used to configure internal or external references and BIAS operations.

Table 9.6.7 CONFIG3: Configuration Register 3

7	6	5	4	3	2	1	0
PD_REFBUF_	1	VREF_4V	0	OPAMP_REF	PDB_OMAMP	0	0
R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Note: R/W = Read/Write; R = Read-only; -n = Reset value

Table 9.6.8 Description of Fields in Configuration Register 3

Bit	Fields	Type	Reset	Description
7	PD_REFBUF_	R/W	0h	**The reference buffer is de-energized.** 0 : Power-off internal reference buffer 1: Enable internal reference buffer
6	Reserve	R/W	1h	**Reserve**
5	VREF_4V	R/W	0h	**Reference voltage.** This bit determines the internal reference voltage VREFP. 0: VREFP is set to 2.4V 1: VREFP is set to 4V (only for use with a 5V analog power supply)
4	reserve	R/W	0h	**Reserve**
3	OPAMP_REF	R/W	0h	**op-amp reference source** This bit determines the source of the op-amp's reference signal. 0 : External feed of reference signal 1: The reference signal is generated internally by (AVDD+AVSS)/2.
2	PDB_OPAMP	R/W	0h	**op-amp power supply** 0 : Op-amp is powered off 1: Op-amp enable
1	Reserve	R/W	0h	**Reserve**
0	Reserve	R	0h	**Reserve**

9.6.5 FAULT: Fault Detection Control Register (Address = 04h) (Reset = 00h)

This register is configured for fault detection operations.

Table 9.6.9 LOFF: Lead Detection Control Register

7	6	5	4	3	2	1	0
COMP_TH2[2:0]			0	0		0	
R/W-0h			R/W-0h	R/W-0h		R/W-0h	

Note: R/W = Read/Write; R = Read-only; -n = Reset value

Table 9.6.10 Description of Lead Detection Control Register Fields

Bit	Fields	Type	Reset	Description
7:5	COMP_TH2[2:0]	R/W	0h	**Error detection comparator threshold** comparator positive terminal 000: 95% 001: 92.5% 010: 90% 011: 87.5% 100: 85% 101: 80% 110: 75% 111: 70% comparator negative terminal 000: 5% 001: 7.5%
4:0	Reserve	R/W	0 h	**Reserve**

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9.6.6 CHnSET: Channel Setup (n = 1 to 8) (Address = 05h to 0Ch) (Reset = 61h)

This register configures the channel's power mode, PGA gain, and multiplexer settings.

Table 9.6.11 CHnSET: Channel Setting Register

7	6	5	4	3	2	1	0
PDn	GAINn[2:0]			0	MUXn[2:0]		
R/W-0h	R/W-6h			R/W-0h	R/W-0h		

Note: R/W = Read/Write; R = Read-only; -n = Reset value

Table 9.6.12 Description of Lead Detection Control Register Fields

Bit	Fields	Type	Reset	Description
7	PDn	R/W	0h	**Power outage.** This bit determines the power-off mode of the corresponding channel. 0: Normal operation. 1: Power outage in the channel. When closing a channel, it is recommended to set the CHnSET register MUXn[2:0] = 001 to close the channel. Set the input to short circuit.
6:4	GAINn[2:0]	R/W	6h	**PGA gain.** These bits determine the PGA gain setting. 000: 1 001: 2 010: 4 011: 6 100: 8 101: 12 110: 24 111: Do not use
3	Reserve	R/W	0h	**Reserve**
2:0	MUXn[2:0]	R/W	1h	**Channel input.** These bits determine the channel input selection.

				000: Normal electrode input 001: Input short circuit (used for offset or noise measurement) 010: Reserved 011: MVDD for power supply measurement 100: Temperature sensor 101: Test signal 110: Reserved 111: Reserved

9.6.7 FAULT_STATP: Positive Fault Status Register (Address = 12h) (Reset = 00h)

This register stores the fault status of the positive terminal of each channel.

Table 9.6.13 FAULT_STATP: Positive Terminal Fault Status Register (Read-only)

7	6	5	4	3	2	1	0
IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Note: R/W = Read/Write; R = Read-only; -n = Reset value

Table 9.6.14 Description of Fields in the Positive Terminal Fault Status Register

Bit	Fields	Type	Reset	Description
7: 0	IN[8:1]P_FAULT	R	0h	**Channel [8:1] Positive input fault status** 0: Input did not exceed voltage threshold. 1: Input voltage exceeds threshold

9.6.8 FAULT_STATN: Negative terminal fault status register (address = 13h) (reset = 00h)

This register stores the fault status of the negative terminal of each channel.

Table 9.6.15 FAULT_STATN: Negative Fault Status Register (Read-only)

7	6	5	4	3	2	1	0
IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Note: R/W = Read/Write; R = Read-only; -n = Reset value

Table 9.6.16 Description of Fields in the Negative Terminal Fault Status Register

Bit	Fields	Type	Reset	Description
7:0	IN[8:1]N_FAULT	R	0h	**Channel [8:1] Positive input fault status** 0: Input did not exceed voltage threshold 1: Input voltage exceeds threshold

9.6.9 GPIO: General Purpose I/O Registers (Address = 14h) (Reset = 0Fh)

This register controls the behavior of the GPIO pins.

Table 9.6.17 GPIO: General Purpose I/O Registers

7	6	5	4	3	2	1	0
GPIOD[4:1]				GPIOC[4:1]			
R/W-0h				R/W-Fh			

Note: R/W = Read/Write; R = Read-only; -n = Reset value

Table 9.6.18 Description of General-Purpose I/O Register Fields

Bit	Fields	Type	Reset	Description
7:4	GPIOD[4:1]	R/W	0h	**GPIO data** These bits are used to read and write data to the GPIO port. When reading the register, the returned data corresponds to the state of the external GPIO pin, regardless of whether it is programmed as an input or output. As an output, writing to GPIOD sets the output value. As an input, writing to GPIOD has no effect.
3:0	GPIOC[4:1]	R/W	Fh	**GPIO control (corresponding to GPIOD)** These bits determine whether the corresponding GPIOD pin is an input or an output. 0: Output 1: Input

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10. Application Matters

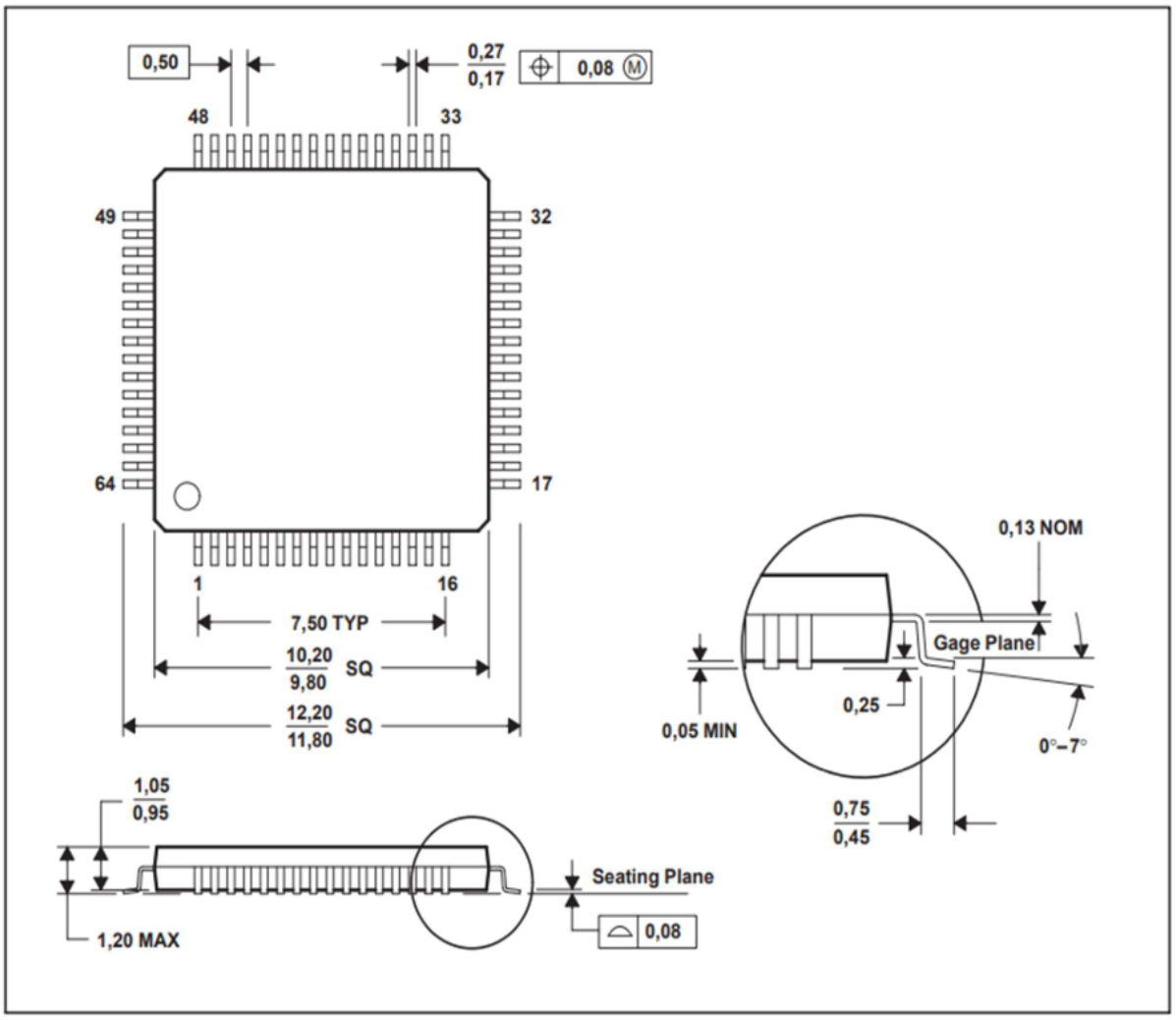
10.1 Precautions for electrostatic discharge

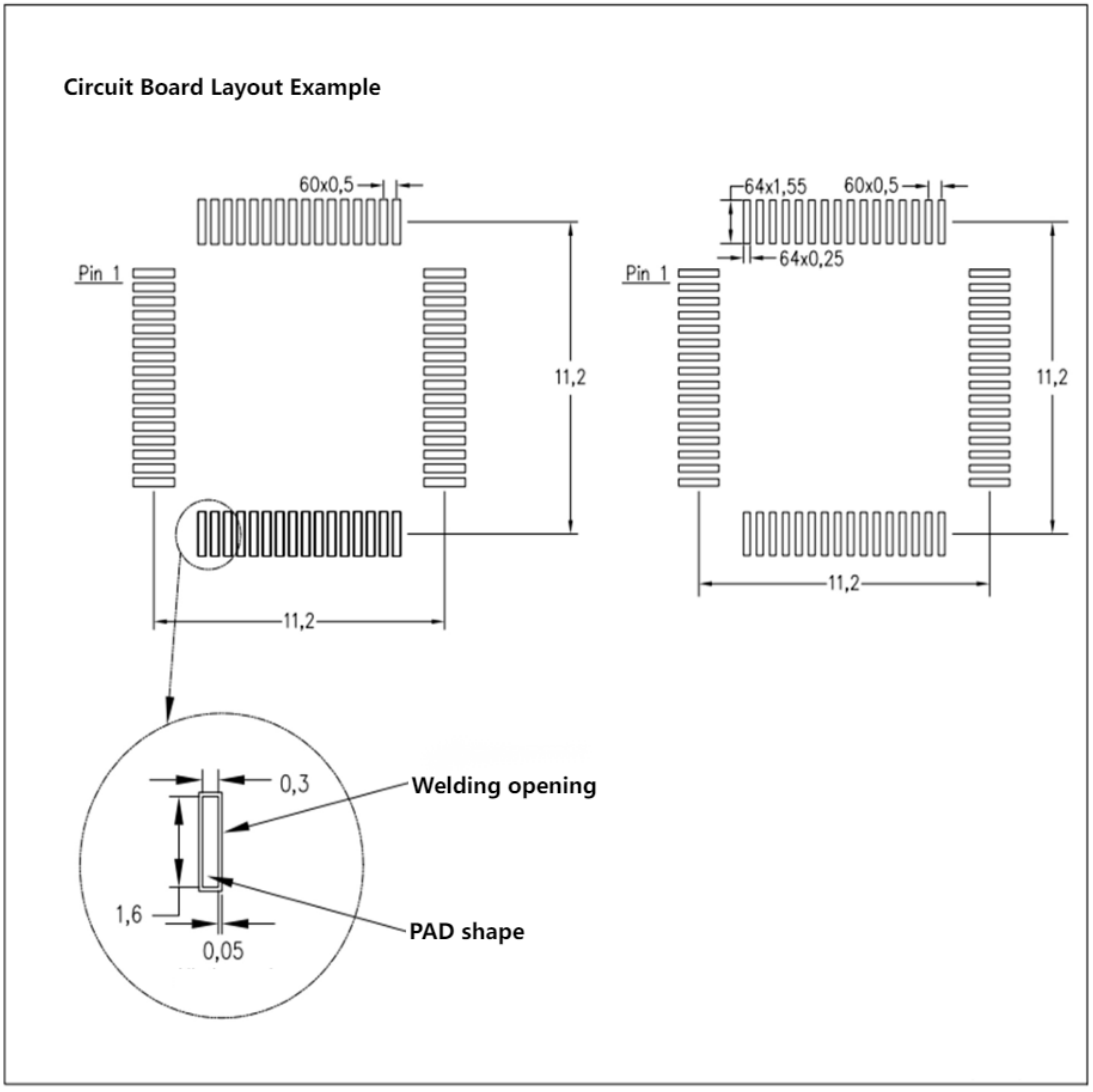
This chip may be damaged by ESD. Appropriate precautions are recommended when handling all chips. Failure to follow proper handling and installation procedures may result in damage.

ESD damage can range from minor performance degradation to complete chip failure. Delicate chips may be more susceptible to damage because even very small parameter variations can cause the chip to fail to meet its published specifications.

10.2 Detailed Package Dimensions

TQFP Package





Note: A. All linear dimensions are in millimeters.

10.3 Chip Ordering Information List

Product Model	Temperature range	Packaging	Packaging	RoHS

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DADS131E04LFP	– 40°C to +105°C	64-LQFP	960/tray	Y
DADS131E08LFP	– 40°C to +105°C	64-LQFP	960/tray	Y