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## Features

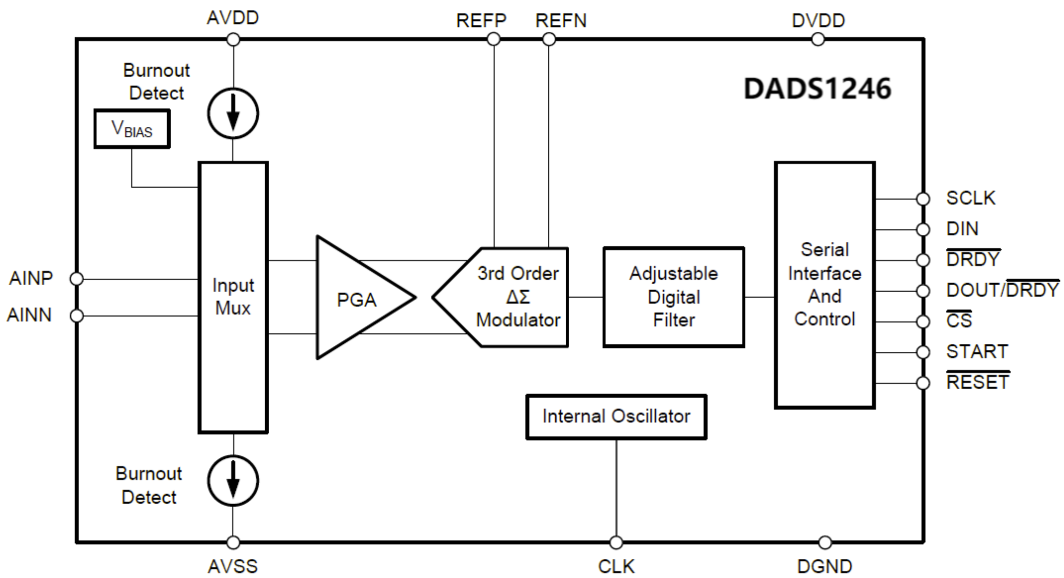
- Programmable data rate: up to 2kSPS
- Single-cycle setup for all data rates
- Harmonic suppression at 20SPS
- Analog multiplexer with 2 independently selectable inputs
- Low-noise programmable gain amplifier: $48nV_{RMS}$ when PGA=128
- Integrated low-drift 2.048V reference voltage: 10ppm/ °C
- Sensor failure detection
- 1 general purpose input/output interfaces
- Built-in temperature sensor
- Self-calibration and system calibration
- SPI interface compatible
- Analog power supply: unipolar (2.7V) to 5.25V) and bipolar (±2.5V) operating voltage
- Digital power supply: 2.7V to 5.25V

The DADS1246 is a precision 24-bit analog-to-digital converter (ADC) that includes many integrated features to reduce system cost and component count for sensor measurement applications. This chip features a low-noise programmable gain amplifier (PGA), a single-cycle digital filter, a high-precision Delta-Sigma (ΔΣ) A/D converter, and an internal oscillator.

The DADS1246's input analog multiplexer supports one differential input. Furthermore, this multiplexer integrates sensor failure detection. The programmable gain amplifier (PGA) provides selectable gain up to 128x. These features provide a complete front-end solution for temperature sensor measurement applications. Digital filters enable single-cycle setup to support fast channel cycling when using the input multiplexer and provide data rates up to 2 kSPS. For data rates of 20 SPS or lower, the filters suppress harmonics from 50 Hz and 60 Hz power frequency interference

## Applications

- Temperature sensor measurement:
  Resistance temperature detectors (RTDs), thermocouples and thermistors
- Pressure measurement
- Flow meter
- Factory automation and process control



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## Absolute Maximum Ratings

Unless otherwise stated, operate within the room temperature range [(1)] .

| | | Min | Max | Unit |
|---|---|---|---|---|
| Source voltage | AVDD to AVSS | -0.3 | 5.5 | V |
| | AVSS to DGND | -2.8 | 0.3 | |
| | DVDD to DGND | -0.3 | 5.5 | |
| Power-on sequence | Recommended power-on sequence for AVDD and DVDD | See Figure 6 | | |
| Analog input voltage | AINx, REFPx, REFNx, VREFOUT, VREFCOM, IEXC1, IEXC2 | AVSS-0.3 | AVDD+0.3 | V |
| Digital input voltage | SCLK, DIN, DOUT/DRDY, DRDY, CS, START, RESET, CLK | DGND-0.3 | DVDD+0.3 | V |
| Input current | Continuous, any pin except power supply pins | -10 | 10 | mA |
| | Instantaneously, any pin except the power supply pin | -100 | 100 | |
| Temperature | Junction temperature, TJ | | 150 | ℃ |
| | Storage, Tstg | -60 | 150 | |

(1) The stress values listed below, exceeding the absolute maximum ratings, may cause permanent damage to the device. These are only operating conditions at the stress ratings; functional operation of the device at the ratings and any other operation beyond the recommended operating conditions are not described here. Prolonged operation at the absolute maximum ratings will affect the reliability of the device.


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## Electrical Characteristics

Minimum and maximum specification values apply to a temperature range of TA = -40 °C to +125°C. Typical specification values were determined at TA = 25°C. All specification values are at AVDD = 5V, DVDD = 3.3V, AVSS = 0V, external VREF = 2.048V, and $f_{CLK}$ = 4.096 MHz (unless otherwise noted).

| Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Analog Input** | | | | | |
| Differential input current | | | 100 | | pA |
| Absolute input current | | | See Table 4 | | |
| **PGA** | | | | | |
| PGA gain settings | | | 1, 2, 4, 8, 16, 32, 64, 128 | | V/V |
| **System performance** | | | | | |
| resolution | | 24 | | | Bits |
| DR data transfer rate | | 5, 10, 20, 40, 80, 160, 320, 640, 1000, 2000 | | | SPS |
| ADC conversion time | | | Single cycle | | |
| INL Integral Nonlinearity | Single-ended input, gain = 1, VCM = 2.5 V | 0.004% | | 0.06% | FS |
| $V_{IO}$ input offset voltage | After calibration (1) | -10 | | 10 | uV |
| Offset Drift | Differential input 10mV, endpoint fitting, gain PGA=1, VCM=2.5 V | | See Figure 5 | | |
| Gain error | TA = 25°C, before all gain calibrations. DR = 40 SPS, 80 SPS, or 160 SPS | -0.05% | 0.01% | 0.05% | |
| Gain drift | | | 1 | | ppm/°C |
| Noise | | | See Tables 1 and 2 | | |
| CMRR common mode rejection ratio | Gain under DC conditions = 1 | 100 | 101 | | dB |
| | Gain under DC conditions = 32 | 97 | 98 | | |
| PSRR Power Supply Rejection Ratio | Gain = 32, Bitrate = 80 SPS under DC conditions for AVDD/DVDD | 112 | 138 | | dB |
| **Voltage reference input** | | | | | |
| Reference input current | | | 30 | | nA |
| Reference drift (2) | $T_A$ = 25°C to 105°C | | 4 | 15 | ppm/°C |
| | $T_A$ = –40 °C to 105 °C | | 6 | 20 | ppm/°C |
| Output current (3) | | -10 | | 10 | mA |
| Load regulation | | | 50 | | µV/mA |
| Startup time | | | See Table 7 | | |
| **Internal oscillator** | | | | | |
| Internal oscillator frequency | | 3.89 | 4.096 | 4.3 | MHz |
| **Failure Current Source** | | | | | |
| Failure current source setting | | | 0.5, 2, 10 | | µA |

1. Noise level misalignment calibration
2. Specified by a combination of design and final production testing
3. Do not exceed the load of the internal reference voltage source

## Electrical Characteristics (continued)

Minimum and maximum specification values apply to a temperature range of TA = -40 °C to +105°C. Typical specification values were determined at TA = 25°C. All specification values are at AVDD = 5V, DVDD = 3.3V, AVSS = 0V, external VREF = 2.048V, and $f_{CLK}$=4.096MHz (unless otherwise noted).

| Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Bias voltage** | | | | | |
| Bias voltage | | | (AVDD + AVSS) / 2 | | V |
| Bias voltage output impedance | | | 400 | | Ω |
| **Temperature sensor** | | | | | |
| Output voltage | TA = 25°C | | 112 | | mV |
| Temperature coefficient | | | 353 | | uV/℃ |
| **General Purpose Input/Output (GPIO)** | | | | | |
| $V_{IL}$ low-level input voltage | | AVSS | | 0.3×AVDD | V |
| $V_{IH}$ high-level input voltage | | 0.7×AVDD | | AVDD | V |
| $V_{OL}$ low- level output voltage | $I_{OL}$ = 1 mA | | | 0.2×AVDD | V |
| $V_{OH}$ high-level output voltage | $I_{OH}$ = 1 mA | 0.8×AVDD | | | V |
| **Digital input/output (excluding GPIO)** | | | | | |
| $V_{IL}$ low- level input voltage | | DGND | | 0.3×DVDD | V |
| $V_{IH}$ high-level input voltage | | 0.7×DVDD | | DVDD | V |
| $V_{OL}$ low- level output voltage | $I_{OL}$ = 1 mA | DGND | | 0.2×DVDD | V |
| $V_{OH}$ high-level output voltage | $I_{OH}$ = 1 mA | 0.8×DVDD | | | V |
| Input leakage | DGND < VIN < DVDD | –10 | | 10 | μA |
| **Power supply** | | | | | |
| $I_{AVDD}$ simulates the power supply current | Power saving mode | | 0.1 | | μA |
| | Normal conversion mode, AVDD = 3.3 V, PGA = 1. DR = 20 SPS, External Reference | | 33.1 | | μA |
| | Normal conversion mode, AVDD = 3.3 V, PGA = 128. DR = 20 SPS, External Reference | | 158.6 | | μA |
| $I_{DVDD}$ digital power supply current | Power saving mode | | 0.2 | | μA |
| | Normal mode, DVDD = 3.3 V, PGA = 1, DR = 20 SPS, internal oscillator | | 143.5 | | μA |
| | Normal mode, DVDD = 3.3 V, PGA = 128, DR = 20 SPS, internal oscillator. | | 143.5 | | μA |
| Power consumption | AVDD = DVDD = 3.3 V, PGA = 1. DR = 20 SPS, internal oscillator, external reference | | 0.58 | | mW |
| | AVDD = DVDD = 3.3 V, PGA=128, DR = 20 SPS, internal oscillator, external reference | | 0.99 | | mW |



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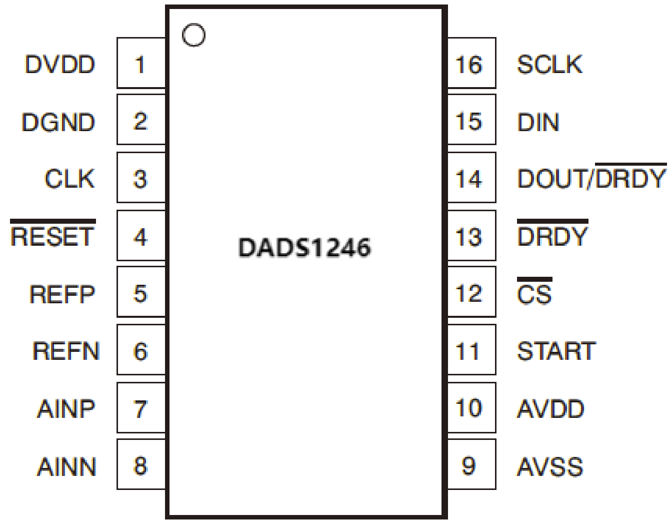
**TSSOP16 Package Pin Definition**




## Pin Function Table

| Pin name | PIN No. | Function | Description |
|---|---|---|---|
| AINP | 7 | Input/Output | Analog input positive |
| AINN | 8 | Input/Output | Analog input negative |
| AVDD | 10 | Power supply | Positive analog power supply |
| AVSS | 9 | Power supply | Negative analog power supply |
| CLK | 3 | Input | External clock source pin. If this pin is not used, it is connected to DGND |
| $\overline{CS}$ | 12 | Input | Chip select; active low |
| DGND | 2 | Ground | Digital ground |
| DIN | 15 | Input | Serial data input |
| DOUT/$\overline{DRDY}$ | 14 | Output | Serial data output in conjunction with data ready; active low. |
| $\overline{DRDY}$ | 13 | Output | Data ready, active low |
| DVDD | 1 | Power supply | A 0.1uF capacitor is connected between the positive digital power supply and DGND |
| REFN | 6 | Input | A negative external reference voltage input is used to connect a capacitor ranging from 1uF to 47uF to REFP |
| REFP | 5 | Input | Positive external reference voltage input |
| $\overline{RESET}$ | 4 | Input | Reset ( active low ) |
| SCLK | 16 | Input | Serial clock input |
| START | 11 | Input | Start conversion |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## Switching Characteristics

Operating ambient temperature TA = -40 °C to 105 °C and DVDD = 2.7V to 5.5V (unless otherwise noted; see Figures 1 and 2).

| Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| The propagation delay time of $t_{DOPD}$, from the rising edge of SCLK to the valid new DOUT | DVDD ≤ 3.6V | | | 50 | ns |
| | DVDD>3.6V | | | 180 | |
| $t_{DOHD}$ DOUT Hold Time | | 0 | | | ns |
| The propagation delay time of $t_{CSDO}$, from the rising edge of CS to the high-impedance state of DOUT | | | | 10 | ns |
| $t_{PWH}$ pulse duration, DRDY high level | | 3 | | | $t_{CLK}$ |

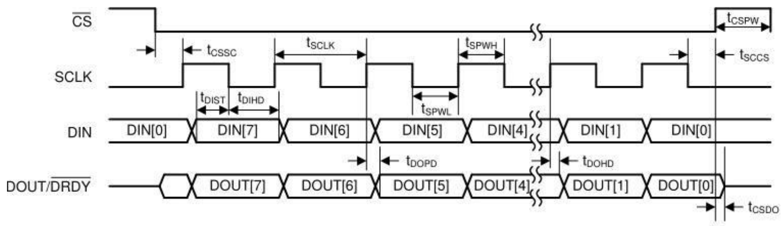
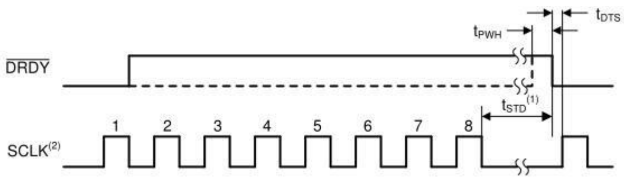



Figure 1. Serial interface timing, DRDY mode bit = 0




(1) This timing diagram only applies when the CS pin is low. When CS is high, SCLK does not need to be low during tSTD.

(2) During partial retrieval of output data, SCLK can only be sent in multiples of eight.

Figure 2. Timing of the serial interface that allows loading conversion results

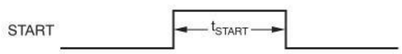



Figure 3. Minimum start pulse duration

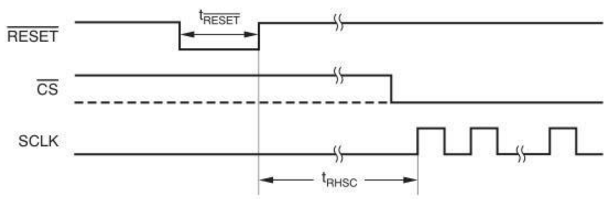



Figure 4. Reset pulse duration and serial interface after reset



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## Noise performance

Optimize ADC noise performance by adjusting the data rate and PGA settings. Typically, the lowest input noise is achieved using the highest gain that matches the input signal range. Do not set the gain too high to prevent the ADC output from going out of range. Noise also depends on the output data rate; as the data rate decreases, the ADC bandwidth decreases accordingly. A reduction in total bandwidth results in a reduction in overall noise. Tables 1 and 2 summarize the device's noise performance. These data represent typical noise performance at TA=25°C. The data shown are the result of averaging readings from multiple chips, and the input signal needs to be shorted during measurement. At least 128 consecutive readings are required to calculate each root mean square noise (RMS) and peak (PP) noise.

Table 1 lists the input noise in units of μVRMS and μV. Table 2 presents the corresponding data for ENOB (effective number of bits), where the ENOB of RMS noise is defined by Equation 1:

$$ENOB=\ln((2\cdot V_{REF}/Gain)/V_{NRMS})/\ln(2) \quad \text{(Equation 1)}$$

Among them $V_{NRMS}$ = The equivalent RMS noise voltage of the input is used to calculate the peak-to-peak noise ENOB in the same way.

Table 1. Noise, in $\mu V_{RMS}$ and ($\mu V_{PP}$)

Conditions: AVDD=DVDD=3.3V, AVSS=0V, Internal reference voltage=2.048V, C3=4.7 μV

| Data transfer rate (SPS) | Gain (PGA Enabled) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
| 5 | 5.80 (38.33) | 7.32 (48.33) | 20.16 (133.05) | 31.81 (209.96) | 8.69 (57.37) | 12.68 (83.74) | 23.26 (153.56) | 41.20 (271.97) |
| 10 | 8.13 (53.71) | 11.98 (79.10) | 21.38 (141.11) | 43.61 (287.84) | 11.98 (79.10) | 13.50 (89.11) | 33.62 (221.92) | 56.59 (373.53) |
| 20 | 8.65 (57.12) | 16.97 (112.06) | 32.36 (213.62) | 58.88 (388.67) | 14.75 (97.41) | 19.38 (127.93) | 41.06 (270.99) | 73.61 (485.84) |
| 40 | 18.05 (119.14) | 16.64 (109.86) | 34.62 (22.85) | 45.98 (299.56) | 21.12 (139.40) | 24.71 (163.08) | 33.66 (222.16) | 78.75 (519.77) |
| 80 | 20.67 (136.47) | 22.97 (151.61) | 36.32 (239.74) | 77.75 (513.18) | 24.82 (163.81) | 33.51 (221.19) | 53.60 (353.76) | 97.98 (646.72) |
| 160 | 22.63 (149.41) | 30.51 (201.41) | 52.00 (343.26) | 100.54 (663.57) | 35.65 (235.35) | 48.68 (321.28) | 60.07 (396.48) | 160.46 (1059.08) |
| 320 | 23.26 (153.56) | 26.52 (175.04) | 33.95 (224.12) | 57.66 (380.61) | 19.86 (131.10) | 30.07 (198.48) | 59.40 (392.09) | 104.13 (687.25) |
| 640 | 31.10 (205.32) | 31.92 (210.69) | 60.66 (400.39) | 92.58 (611.08) | 27.66 (182.61) | 40.32 (266.11) | 82.26 (542.96) | 126.47 (834.71) |
| 1000 | 28.66 (189.20) | 34.51 (1227.78) | 41.42 (273.43) | 87.03 (574.46) | 28.22 (186.27) | 36.28 (239.50) | 93.06 (614.25) | 185.73 (1225.83) |
| 2000 | 24.56 (162.10) | 39.98 (263.91) | 53.96 (356.20) | 83.71 (552.49) | 31.10 (205.32) | 49.16 (324.46) | 80.19 (529.29) | 124.14 (819.33) |

Table 2. ENOB (Peak-to-Peak Noise) derived from root mean square (RMS) noise.
Conditions: AVDD=DVDD=3.3V, AVSS=0V, Internal reference voltage=2.048V

| **Data transfer rate (SPS)** | **Gain (PGA Enabled)** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **1** | **2** | **4** | **8** | **16** | **32** | **64** | **128** |
| 5 | 19.4 | 19.1 | 17.6 | 16.9 | 18.8 | 18.3 | 17.4 | 16.6 |
| 10 | 18.9 | 18.3 | 17.5 | 16.5 | 18.3 | 18.2 | 16.8 | 16.1 |
| 20 | 18.8 | 17.8 | 16.9 | 16.0 | 18.0 | 17.6 | 16.6 | 15.7 |
| 40 | 17.8 | 17.9 | 16.8 | 16.4 | 17.5 | 17.3 | 16.8 | 15.6 |
| 80 | 17.6 | 17.4 | 16.7 | 15.6 | 17.3 | 16.8 | 16.2 | 15.3 |
| 160 | 17.4 | 17.0 | 16.2 | 15.3 | 16.8 | 16.3 | 16.0 | 14.6 |
| 320 | 17.4 | 17.2 | 16.8 | 16.1 | 17.6 | 17.0 | 16.0 | 15.2 |
| 640 | 17.0 | 16.9 | 16.0 | 15.4 | 17.1 | 16.6 | 15.6 | 14.9 |
| 1000 | 17.1 | 16.8 | 16.5 | 15.5 | 17.1 | 16.7 | 15.4 | 14.4 |
| 2000 | 17.3 | 16.6 | 16.2 | 15.5 | 17.0 | 16.3 | 15.6 | 15.0 |


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## Offset Drift

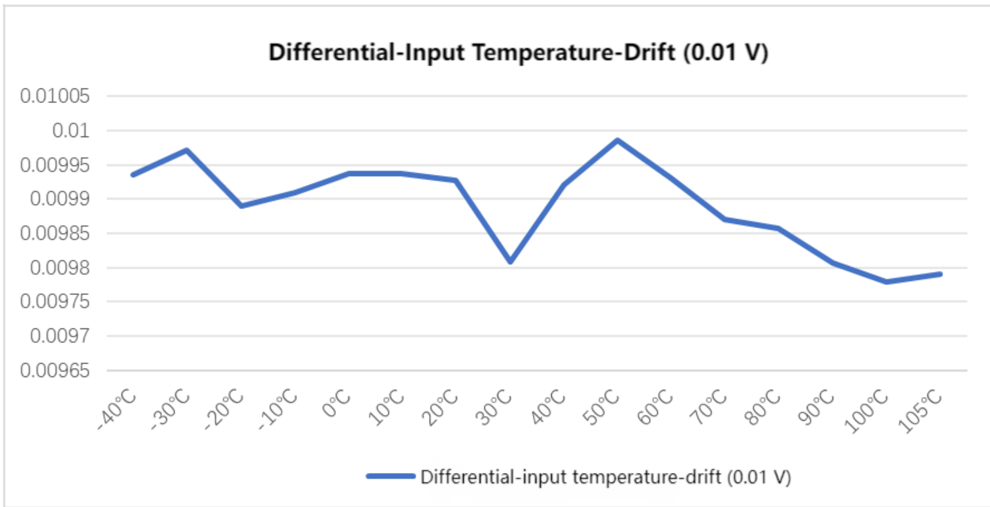



Figure 5. Temperature drift curve of offset drift

## Recommended Power-On Timing Diagram for DVDD and AVDD

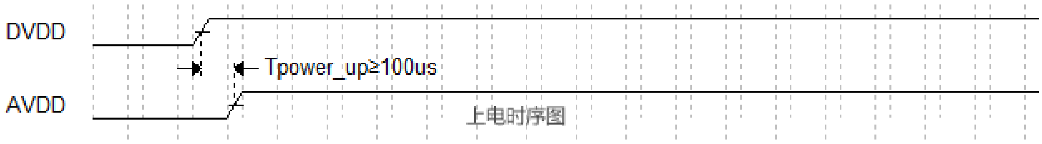
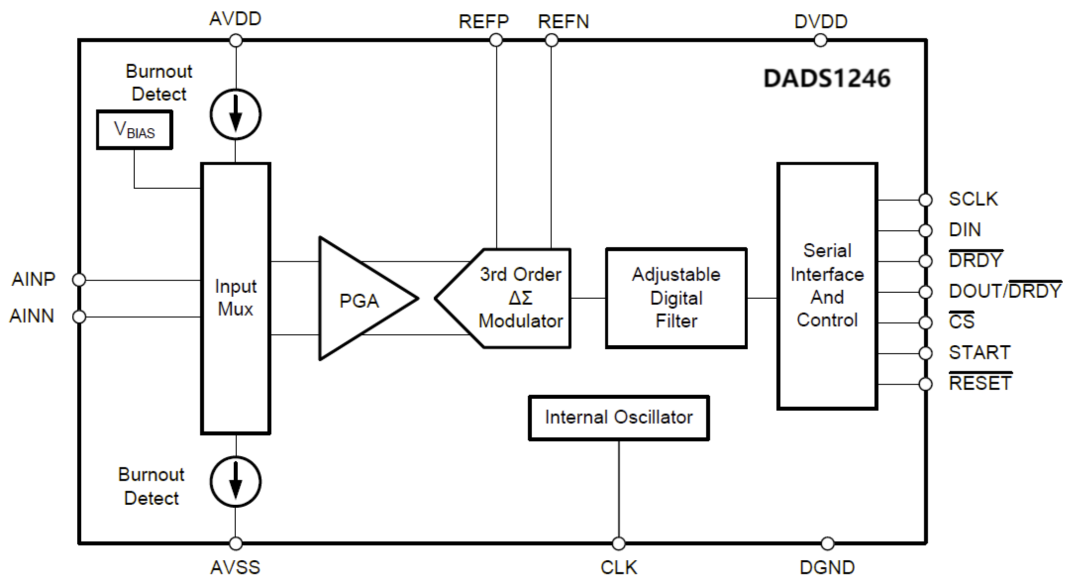



Figure 6. Power -on timing diagram

## Overview

The DADS1246 devices are highly integrated 24-bit data converters. These devices include a low-noise, high-input-impedance programmable gain amplifier (PGA), a delta-sigma (ΔΣ) type ADC with a single-cycle setup digital filter, an internal oscillator, and an SPI-compatible serial interface. The DADS1246 also includes a flexible input multiplexer with system monitoring capabilities and general-purpose I/O settings, an extremely low-drift reference voltage source, and two matched current sources for sensor excitation.

Figure 7: Functional Block Diagram





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## Function Description

### ADC Input Multiplexer

The ADC measures the input signal via the on-chip PGA. All analog inputs are connected to the internal AINP or AINN analog inputs via an analog multiplexer. Figure 8 shows a block diagram of the analog input multiplexer.

The input multiplexer connects to eight analog inputs. The MUX0 register allows selection of any analog input pin as a positive or negative input. The multiplexer also allows selection of on-chip excitation current and bias voltage for specific channels. The input multiplexer allows selection of ambient temperature (internal temperature sensor), AVDD, DVDD, and external reference voltage for measurement. See the system monitor for more information.

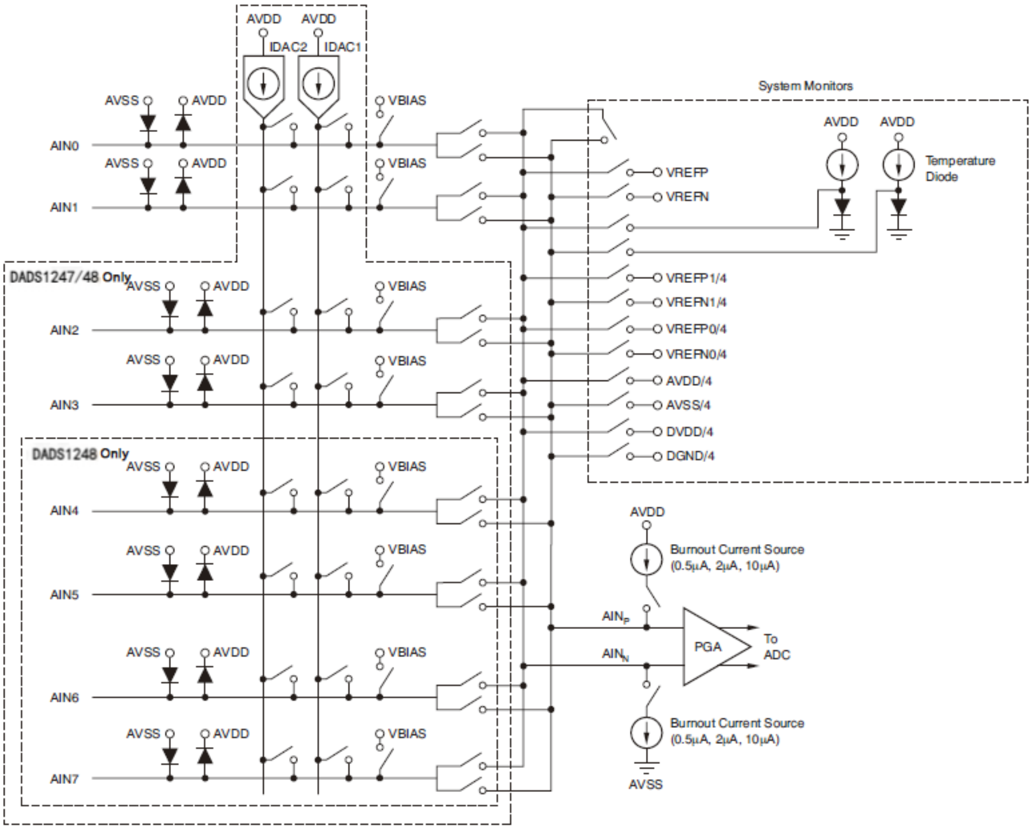


Figure 8. Simplified diagram of input multiplexer

ESD diodes protect the ADC input. To prevent these diodes from conducting, ensure that the voltage on the analog input pin is no more than 100mV lower than AVSS and no more than 100mV higher than AVDD, as shown in Equation 2. The same applies if the input is configured as GPIOs.

$$AVSS - 100mV < V_{(AINX)} < AVDD + 100mV \quad \text{(Equation 2)}$$

## Low-Noise Programmable Gain Amplifier

The DADS1247 features a low-drift, low-noise, high-input-impedance programmable gain amplifier (PGA). Register SYS0 allows setting the PGA gain to 1, 2, 4, 8, 16, 32, 64, or 128. Figure 9 shows a simplified diagram of the PGA.

The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistive feedback network used to set the PGA gain. The PGA input is equipped with an electromagnetic interference (EMI) filter, as shown in Figure 7. Note that, as with any PGA, ensure the input voltage remains within the specified common-mode input range. The common-mode voltage is calculated using Equation 3.

(AVSS+0.1V+(VINMAX × Gain)/2) ≤ VCM ≤ (AVSS-0.1V-(VINMAX×Gain)/2) (Equation 3)

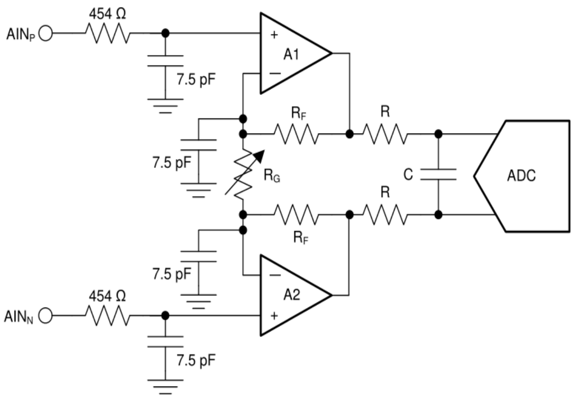


Figure 9. Simplified diagram of PGA

The gain of the device is changed using a variable resistor RG. The differential full-scale input voltage range (FSR) of the PGA is determined by the gain setting and the reference voltage used, as shown in Equation 4.

$FSR=\pm V_{REF}/Gain$ (Equation 4)

Table 3 shows the full-scale input range when using the internal 2.048 reference voltage source.

Table 3. PGA Full scale range

| PGA GAIN SETTING | FSR |
|---|---|
| 1 | ±2.048V |
| 2 | ±1.024V |
| 4 | ±0.512V |
| 8 | ±0.256V |
| 16 | ± 0.128V |
| 32 | ±0.064V |
| 64 | ±0.032V |
| 128 | ±0.016V |

## PGA Common-Mode Voltage Requirements

To maintain the PGA's linear operating range, the input signal must meet certain requirements discussed in this section. The output swings of the two amplifiers (A1 and A2) in Figure 10 cannot be closer to the power supply (AVSS and AVDD) than 100mV. If the outputs OUTP and OUTN are driven within the 100mV range of the power supply rails, the amplifier will saturate and become nonlinear. To prevent this nonlinear operating condition, the output voltage must satisfy Equation 5.

$AVSS+0.1V \le V_{(OUTN)}, V_{(OUTP)} \le AVDD-0.1$ (Equation 5)

It is beneficial to transform the requirements of the above equations into requirements referred to the PGA inputs (AINP and AINN) because the PGA outputs cannot be directly accessed. The PGA employs a symmetrical design; therefore, it can be assumed that the common-mode voltage at the PGA output is the same as the common-mode voltage of the input signal, as shown in Figure 10.

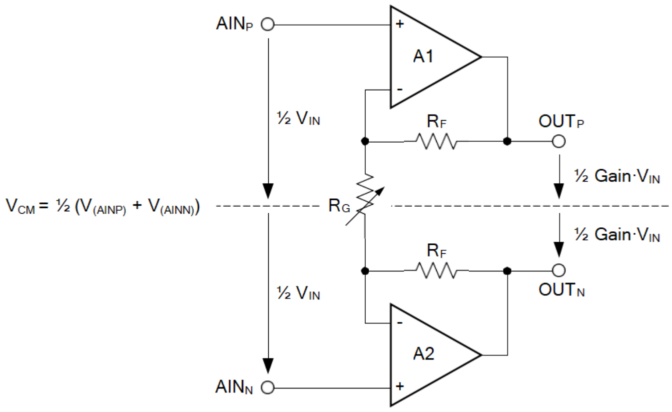


Figure 10. PGA Common Mode Voltage

Common-mode voltage is obtained by the Equation 6.

$VCM = ½(V_{(AINP)} + V_{(AINN)}) = ½(V_{(OUTP)} + V_{(OUTN)})$ (Equation 6)

The voltages at the PGA input terminals (AINP and AINN) can be expressed by Equations 7 and 8.

$V_{(AINP)} = V_{CM} + ½ V_{IN}$ (Equation 7)

$V_{(AINN)} = V_{CM} - ½ V_{IN}$ (Equation 8)

Output voltage (V( OUTP ) and V( OUTN )) can be obtained through the Equations 9 and 10.

$V_{(OUTP)} = V_{CM} + ½ Gain \cdot V_{IN}$ (Equation 9)

$V_{(OUTN)} = V_{CM} - ½ Gain \cdot V_{IN}$ (Equation 10)

Now, the output voltages of amplifiers A1 and A2 (as per Equation 5) can be converted into the requirements for the input common-mode voltage range through Equations 9 and 10, as shown in Equations 11 and 12.

$$V_{CM(MIN)} \geq AVSS + 0.1V + ½ Gain \cdot V_{IN(MAX)}$$
(Equation 11)

$$V_{CM(MAX)} \leq AVDD - 0.1V - ½ Gain \cdot V_{IN(MAX)}$$
(Equation 12)

To calculate the minimum and maximum common-mode voltage limits, the maximum differential input voltage ( $V_{IN(MAX)}$ ) that occurs in the application must be used. $V_{IN(MAX)}$ can be less than the maximum possible full-scale value.

## PGA Common Mode Voltage Calculation Example

The following paragraphs explain how to apply Equations 11 and 12 to the hypothetical application. In this example, with AVDD = 3.3V, AVSS = 0V, gain = 16, and an external reference voltage VREF = 2.5V, the maximum possible differential input voltage VIN = (V(AINP) − V(AINN)) can be applied. This voltage is then limited to the full-scale range of FSR = 2.5V/16 = 0.156V. Therefore, Equations 11 and 12 yield an allowable VCM range of 1.35V ≤ VCM ≤ 1.95V.

For example, if in such an application the sensor signal connected to the input does not utilize the full-scale range but is limited to VIN(MAX) = 0.1V, this reduced input signal amplitude will broaden the VCM limit to 0.9V ≤ VCM ≤ 2.4V. In the case of fully differential sensor signals, the inputs (AINP, AINN) can swing up to 50mV around the common-mode voltage (V(AINP) + V(AINN))/2, which must be kept between 0.9V and 2.4V. The output of a symmetrical Wheatstone bridge is an example of a fully differential signal. Figure 11 shows the case where the common-mode voltage of the input signal is at its minimum limit. In this case, V(OUTN) is exactly 0.1V. Any further reduction in the common-mode voltage (VCM) or an increase in the differential input voltage (VIN) will drive V(OUTN) below 0.1V and saturate amplifier A2.

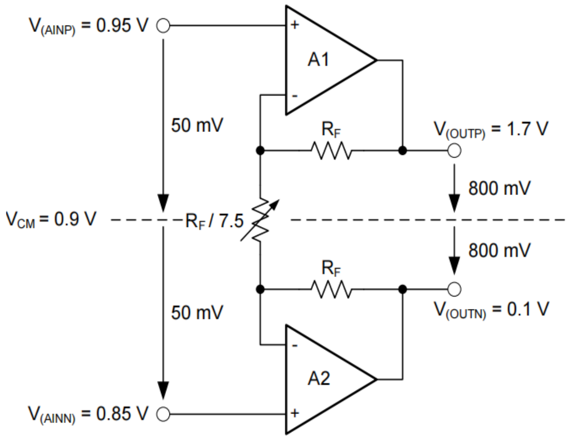


Figure 11. VCM Example at the minimum limit

In contrast, RTD signals are pseudo-differential in nature, with the negative input maintained at a constant voltage beyond 0V, and only the voltage at the positive input changing. When measuring pseudo-differential signals, in this example, the negative input must be biased within a voltage range of 0.85V to 2.35V, and the positive input swing can reach up to VIN(MAX) = 100mV above the negative input. In this case, the voltage at the positive input changes along with the common-mode voltage. That is, when the input signal swings between 0V ≤ VIN ≤ VIN (maximum value), the common-mode voltage swings between V(AINN) ≤ VCM ≤ V(AINN) + ½ VIN (maximum value). Meeting the common-mode voltage requirement of the maximum input voltage VIN(MAX) ensures that the requirement is met across the entire signal range.

Figures 12 and 13 show examples of fully differential and pseudo-differential signals, respectively.

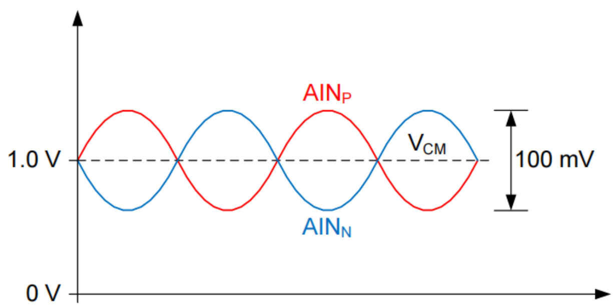


Figure 12. Fully differential input signal



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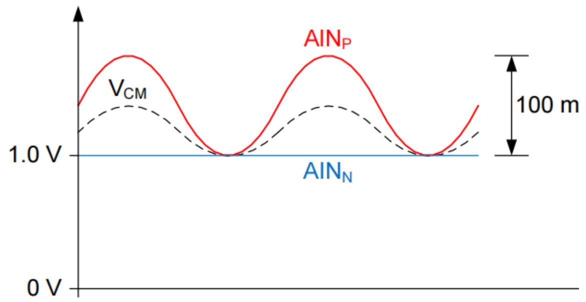



Figure 13. pseudo-differential input signal

Notice: When using a unipolar power supply, the input range does not extend to ground. Equations 11 and 12 show the common-mode voltage requirements.

$$VCM_{(MIN)} \geq AVSS + 0.1V + ½\ Gain \cdot VIN_{(MAX)}$$

$$VCM_{(MAX)} \leq AVDD - 0.1V - ½\ Gain \cdot VIN_{(MAX)}$$

## Analog input impedance

The device input is buffered by a high-input-impedance PGA before reaching the Δ - Σ modulator. For most applications, the input current is small and negligible. However, due to the chopping function of the PGA, the input impedance can be described as a small absolute input current. The absolute input current of the selected channel is approximately proportional to the clock speed of the selected modulator. Table 4 shows typical values for these currents at different voltage coefficients and the corresponding input impedances at different data rates.

Table 4. Typical values of analog input current at data rates (1)

| Condition | Absolute input current | Effective input impedance |
|---|---|---|
| DR=5SPS, 10SPS, 20SPS | ±(0.5nA+0. 1nA/V) | 5000 MΩ |
| DR=40SPS, 80SPS 160SPS | ±(2nA+0.5nA/V) | 1200 MΩ |
| DR=320SPS, 640SPS 1kSPS | ±(4nA+1nA/V) | 600 MΩ |
| DR=2kSPS | ±(8nA+2nA/V) | 300 MΩ |

(1) Input current when VCM=2.5V, TA=25°C AVDD =5V, AVSS =0 V

## Clock source

This device can use either an internal oscillator or an external clock. Connect the CLK pin to DGND before powering on or resetting to activate the internal oscillator. Connecting an external clock to the CLK pin disables the internal oscillator at any time, and the device then operates on the external clock. Once the device has switched to an external clock, it cannot switch back to the internal oscillator unless the device is powered on or reset.

## Modulator

The DADS1246 device uses a third-order Δ - Σ modulator. The modulator converts the analog input voltage into a pulse code modulation (PDM) data stream. To save power, the modulator clock operates in the range of 32kHz to 512kHz, supporting different data rates, as shown in Table 5.

Table 5. Modulator clock frequency at different data rates

| Data rate (SPS) | Modulator rate ($f_{MOD}$) (1) (kHz) | $f_{CLK}/f_{MOD}$ |
|---|---|---|
| 5, 10,20 | 32 | 128 |
| 40, 80, 160 | 128 | 32 |
| 320,640, 1000 | 256 | 16 |
| 2000 | 512 | 8 |

(1) Use an internal oscillator or an external oscillator 4.096 MHz clock.

## Digital Filters

This ADC uses a linear-phase finite-impulse-response (FIR) digital filter, which can be adjusted for different output data rates. The digital filter is always built up within a single cycle.

Table 6 shows the precise data rate when using an external clock of 4.096MHz. The figure also shows the signal -3dB bandwidth and 50Hz and 60Hz attenuation. For good 50Hz or 60Hz rejection performance, use a data rate of 20SPS or lower. The data rate and digital filter frequency response are proportional to changes in the system clock frequency. Changes in the internal oscillator frequency, as described in the electrical characteristics section, also affect the data rate and digital filter frequency response.

Table 6. Digital Filter Specifications (1)

| Nominal Data rate | Actual Data rate | -3dB Bandwidth | attenuation | | | |
|---|---|---|---|---|---|---|
| | | | $f_{IN}$ = 50Hz ± 0.3Hz | $f_{IN}$ = 60Hz ± 0.3Hz | $f_{IN}$ = 50Hz ± 1Hz | $f_{IN}$ = 60Hz ± 1Hz |
| 5SPS | 5.018SPS | 2.26Hz | – 106dB | -74 dB | – 81dB | -69dB |
| 10SPS | 10.037SPS | 4.76Hz | – 106dB | -74 dB | – 80dB | -69dB |
| 20SPS | 20.075SPS | 14.8Hz | – 71dB | -74 dB | -66 dB | -68dB |
| 40SPS | 40.15SPS | 9.03Hz | — | — | — | — |
| 80SPS | 80.301SPS | 19.8Hz | — | — | — | — |
| 160SPS | 160.6SPS | 118Hz | — | — | — | — |
| 320SPS | 321.608SPS | 154Hz | — | — | — | — |
| 640SPS | 643.21SPS | 495Hz | — | — | — | — |
| 1000SPS | 1000SPS | 732Hz | — | — | — | — |
| 2000SPS | 2000SPS | 1465Hz | — | — | — | — |

(1) The values displayed when $f_{CLK}$=4.096 MHz.

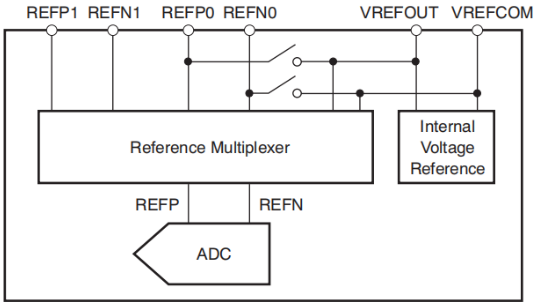
## Reference voltage input

The reference voltage for this device is the differential voltage between REFP and REFN, given by Equation 13:

$$V_{REF} = V_{(REFP)} - V_{(REFN)} \quad \text{(Equation 13)}$$

There is a multiplexer for selecting the reference input, as shown in Figure 14. The reference input uses a buffer to increase the input impedance.

Figure 14. Reference Input Multiplexer




The reference input circuit has an ESD diode to protect the input. To prevent the diode from conducting, ensure that the voltage on the reference input pin is not lower than AVSS - 100mV and does not exceed AVDD + 100mV, as shown in Equation 14.

$$AVSS - 100mV < (V_{(REFP)} \text{ or } V_{(REFN)}) < AVDD + 100mV \quad \text{(Equation 14)}$$

## Sensor Detection

To aid in the detection of potential sensor malfunctions, the device provides selectable current sources (0.5uA, 2uA, or 10uA) as burn-off current sources. When enabled, one current source supplies current to the selected positive analog input (AINP), while the other current source draws current from the selected negative analog input (AINN).

If the sensor is open-circuited, these burn-out current sources will pull the positive input to AVDD and the negative input to AVSS, resulting in a full-scale reading. A full-scale reading may also indicate sensor overload or a missing reference voltage. A reading close to zero may indicate a sensor short circuit. The absolute value of the burn-out current source typically varies by 10%, and the internal multiplexer adds a small series resistance. Therefore, distinguishing between a short-circuit sensor condition and a normal reading can be difficult, especially when using an RC filter at the input. In other words, even if the sensor is short-circuited, the voltage drop across the external filter resistor and the remaining resistance of the multiplexer will cause the output reading to be greater than zero.

When a fusible current source is enabled, the ADC readings of the functional sensor may be corrupted. It is recommended to disable fusible current sources when performing precision measurements and to enable them only to test for sensor failure conditions.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## Bias Voltage Generation

An optional bias voltage is provided for unbiased thermocouples. The bias voltage is (AVDD+AVSS)/2 and can be applied to any analog input channel via the internal input multiplexer. Table 7 lists the bias voltage turn-on time for different sensor capacitances.

Selecting internal bias voltage generators on multiple channels can cause internal short circuits within those channels. Therefore, it is important to limit the current flowing through the device. We recommend that under no circumstances should a current exceeding 5mA be allowed through this path.

Table 7. Bias voltage settling time

| Sensor Capacitor | Establishment Time |
|---|---|
| 0.1uF | 220us |
| 1uF | 2.2ms |
| 10uF | 22ms |
| 200uF | 450ms |

## Ambient Temperature Monitor

On-chip diodes provide temperature sensing capability. When the temperature monitoring function is selected, the anodes of the two diodes are connected to the ADC. Typically, at TA=25°C, the diode voltage difference is 118mV, and the temperature coefficient is 405 uv/°C.

## Device Functional Mode

**Power-on –** When the DVDD is powered on, the internal power-on reset module generates a pulse to reset all digital circuits. All digital circuits remain in the reset state for $2^{16}$ system clock cycles to allow the analog circuits and internal digital power to be established. SPI communication will only occur after the internal reset is released.

**Reset –** When the RESET pin goes low, the device immediately resets. All registers are restored to their default values. The device remains in reset mode as long as the RESET pin remains low. When the RESET pin goes high, the ADC exits reset mode and can convert data. After the RESET pin goes high, the digital filters and registers remain in a reset state for 0.6ms when the system clock frequency is 4.096MHz and $f_{CLK}$=4.096MHz. Therefore, valid SPI communication can only be restored 0.6ms after the RESET pin goes high; see Figure 4. When the RESET pin goes low, the clock selection is reset to the internal oscillator.

A reset can also be performed via the serial interface using the reset command, which functions the same as using the RESET pin. For information on using the RESET command, see RESET (0000 011X).

### Power Saving Mode

Power consumption is minimized by placing the device in power-saving mode. There are three ways to put the device into power-saving mode: using the SLEEP command, pulling the START pin low, and entering power-saving mode after each transition when the START/SYNC command controls the mode transition and the CM value in the SYS0 register is 0.

In power-down mode, the state of the internal reference voltage depends on the setting of the VREFCON bit in the MUX1 register; see register mapping for details.

### Start Pin Control

The START pin provides precise control over the conversion. Pulsing the START pin high initiates the conversion, as shown in Figure 15 and Table 8. When the DRDY mode bit in the IDAC0 register is 1, the DRDY pin goes low, and the DOUT/DRDY pin indicates the conversion is complete. After conversion, the device automatically shuts down. The conversion result can be retrieved during power-down; however, START must be pulled high before communicating with the configuration register. The device remains off until the START pin returns high to begin a new conversion. When the START pin returns high, the decimation filter remains reset for 32 modulator clock cycles to allow the analog circuitry to set up.

Keep A high level on the START pin will configure the device for continuous switching, as shown in the figure 16.

Figure 15.Single-transition timing using the Start pin

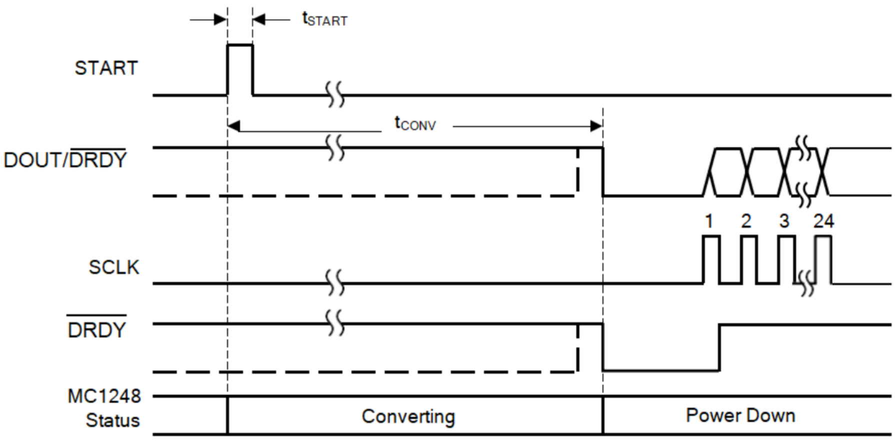
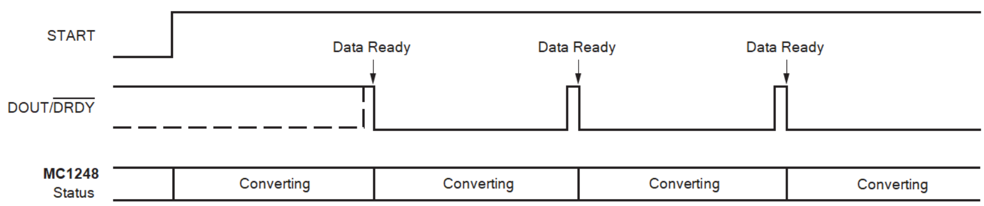



Table 8. Initial pin transition time of Figure 15

| Symbol | Description | Data rate (SPS) | Value | Unit |
|---|---|---|---|---|
| $t_{CONV}$ | Time from the START rising edge to DRDY and DOUT/DRDY going low | 5 | 200.295 | ms |
| | | 10 | 100.644 | ms |
| | | 20 | 50.825 | ms |
| | | 40 | 25.169 | ms |
| | | 80 | 12.716 | ms |
| | | 160 | 6.489 | ms |
| | | 320 | 3.247 | ms |
| | | 640 | 1.692 | ms |
| | | 1000 | 1.138 | ms |
| | | 2000 | 0.575 | ms |

Figure 16. Start Conversion when pin is high



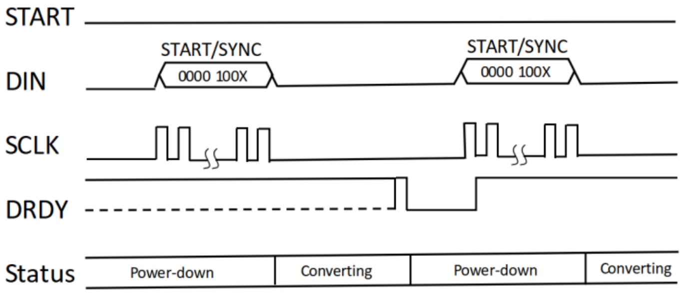

Note : SCLK remains low in this example

When the START pin is held high, the ADC continuously converts the selected input channel. This configuration continues until the START pin is pulled low. The START pin can also be used to perform synchronous measurements in multi-channel applications by applying a pulse . For multiple devices, if each device receives a pulse on the START pin simultaneously , all devices will begin conversion when the START pin rises. If all devices are operating at the same data rate, all devices will complete conversion simultaneously

## Command and Control

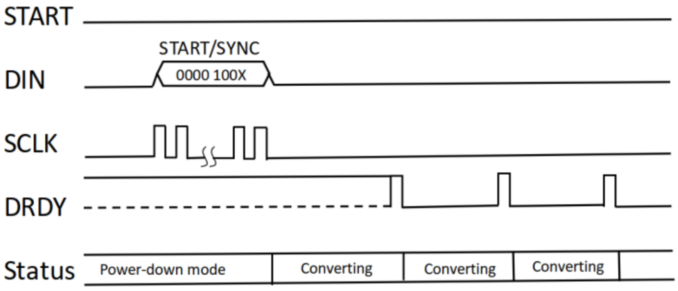
When the START pin is low, the ADC conversion can be controlled by sending a START/SYNC command to the device. When the device receives the START/SYNC command, it determines which conversion mode to enter based on the state of the CM bit in the SYS0 register. In single conversion mode, as shown in Figure 17, the device completes one conversion each time it receives a start/sync command, and then enters power-saving mode. In continuous conversion mode, the device performs conversions continuously. After a conversion is completed, the device puts the result into the output buffer and immediately starts another conversion. To start continuous conversion mode, the CM bit must be set to 1, followed by the start/sync command, as detailed in Figure 18.

To exit the start / synchronization command control switching mode, simply send a stop command to the device once, as shown in the figure. As shown in Figure 19.




Note : CM=0, Single conversion

Figure 17. Use START / SYNC Single conversion timing of the command




Note : CM=1, Continuous conversion

Figure 18. Use START / SYNC Timing of continuous conversion of command

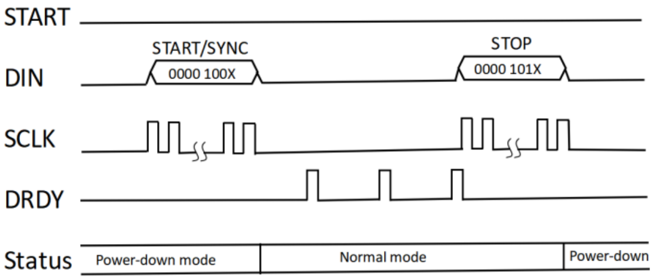



Figure 19. Exit START / SYNC Command Control Mode

Conversions can also be initiated via SPI commands. Similar to using the START pin, the SLEEP command can be used to put the device into power-saving mode. Functionally, this is similar to pulling the START pin low or using the START/SYNC command to control entry into single-conversion mode. To initiate a conversion, the WAKEUP command wakes the ADC and starts the conversion, similar to returning the START pin high or sending the START/SYNC command again. Note that sleep and wake-up commands can only be used to control conversions when the device is in continuous conversion mode. Do not use the START pin and commands simultaneously to control conversions. Furthermore, sending the SYNC or START/SYNC command immediately initiates a new ADC conversion. The digital filter then resets, and the new conversion begins without completing the previous one. This is useful for synchronizing conversions of multiple devices or maintaining periodic timing across multiple channels. Similarly, writing to the first four registers (MUX0, VBIAS, MUX1, or SYS0 addresses 00h to 04h) automatically resets the digital filter. A change in any of these registers will cause a corresponding setting change in the device, but will also restart the conversion, just like the SYNC command.

## Channel Multiplexing Setup Time

This device is a true single-cycle setup ΔΣ converter. Once the input signal has been set up to its final value, the first batch of usable data after the conversion begins is fully set up and available for use. The setup time is approximately equal to the reciprocal of the data rate. The exact time depends on the specific data rate and the operation that initiates the conversion; specific values are shown in Table 9.

## Channel Loop and Overload Recovery

When cycling between channels, pay attention to the device configuration to ensure setup within one cycle. For settings that cycle between multiplexer channels without changing the PGA and data rate settings, changing the MUX 0 register is sufficient. However, when changing the PGA and data rate settings, ensure that no overload occurs during transmission. When configuration register data is transmitted to the device, the new setting takes effect at the end of each transmitted register byte. Therefore, a brief overload may occur during configuration data transmission after the MUX 0 byte has completed and before the SYS 0 byte has completed. This temporary overload can cause intermittent incorrect readings. To ensure no overload occurs, it may be

necessary to split the communication into two separate communications so that the SYS 0 register is changed before changing the MUX 0 register . In overload conditions, ensure that a single cycle proceeds to the next cycle. Because the device uses a chopper-stabilized PGA, changing the data rate in overload conditions can cause chopper instability. This instability results in slow setup time. To prevent this slow setup, always change the PGA or multiplexer settings to a non-overload state before changing the data rate.

## Single Loop Setting

The DADS1246 is capable of single-cycle setup at all gains and data rates. However, to achieve a 2kSPS single-cycle setup time, special care must be taken when using WREG to modify the configuration register interface. When operating at 2kSPS, the SCLK cycle must not exceed 520ns, and the time between the start of writing a register byte and the start of writing subsequent register bytes must not exceed 4.2us. Furthermore, when executing multiple separate write commands to the first four registers, at least 64 system clock cycles must be waited before initiating another write command.

## Digital filter reset operation

In addition to the RESET command and the RESET pin, the digital filter will automatically reset when a write operation is performed on the MUX0, VBIAS, MUX1 or SYS0 register, a SYNC or START/SYNC command is issued, or the START pin goes high.

The filter is reset four system clock cycles (tCLK) after the falling edge of the seventh SCLK following the SYNC or START/SYNC command. Similarly, if any write operation occurs in the MUX 0 register, the filter will be reset after the MUX 0 write operation is complete , regardless of whether the register value changes.

If any write operation occurs in the VBIAS, MUX1, or SYS0 registers , the filter will reset regardless of whether the register value changes. After a write operation completes, the reset pulse lasts for 32 modulator clock cycles. If there are multiple write operations, the resulting reset pulse can be considered as the AND result of different active-low pulses generated individually for each operation.

Table 9 shows the transition times after the filter is reset. These times depend on the operation that initiates the reset, and the first transition after the filter is reset takes slightly different times than the second and subsequent transitions.

Table 9. Data Conversion Time

| Nominal Data rate (SPS) | Accurate Data rate (SPS) | First data conversion time after filter reset | | | | Second and subsequent conversion time filter reset | |
|---|---|---|---|---|---|---|---|
| | | Synchronization command, MUX0 Register write | | Hardware reset, reset command, start pin high level, wake-up command, write to VBIAS, MUX1 or SYS0 register | | | |
| | | (ms) (1) | System clock cycles | (ms) (1) | System clock cycles | (ms) (1) | System clock cycles |
| 5 | 5.019 | 199.258 | 816160 | 200.26 | 820265 | 199.250 | 816128 |
| 10 | 10.038 | 99.633 | 408096 | 100.635 | 412201 | 99.625 | 408064 |
| 20 | 20.075 | 49.820 | 204064 | 50.822 | 208169 | 49.812 | 204032 |
| 40 | 40.151 | 24.92 | 102072 | 25.172 | 103106 | 24.906 | 102016 |
| 80 | 80.301 | 12.467 | 51064 | 12.719 | 52098 | 12.453 | 51008 |
| 160 | 160.602 | 6.240 | 25560 | 6.492 | 26594 | 6.226 | 25504 |
| 320 | 321.608 | 3.124 | 12796 | 3.25 | 13314 | 3.109 | 12736 |
| 640 | 643.216 | 1.569 | 6428 | 1.695 | 6946 | 1.554 | 6368 |
| 1000 | 1000 | 1.014 | 4156 | 1.141 | 4674 | 1 | 4096 |
| 2000 | 2000 | 0.514 | 2108 | 0.578 | 2370 | 0.5 | 2048 |

(1) $f_{CLK}$ = 4.096 MHz

## Calibration

The converted data is scaled by offset and gain registers to produce the final output code. As shown in Figure 20, the output of the digital filter is first subtracted from the offset register (OFC) and then multiplied by the full-scale register (FSC) to digitally adjust the gain. A digital limiting circuit ensures that the output code does not exceed 24 bits. Equation 17 shows the scaling ratio.

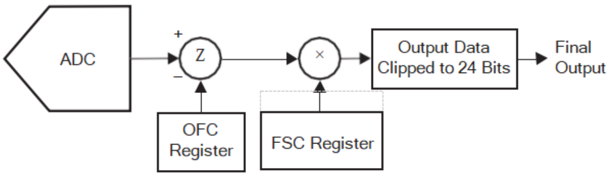



Figure 20. Calibration block diagram

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \text{FSC}[2:0] \qquad \text{(Equation 17)}$$

The values of the offset and full-scale registers can be set directly by writing to them or automatically via calibration commands . Offset and gain calibration features are designed to correct for small system-level offset and gain errors. When manually entering values into the calibration registers, care must be taken to avoid reducing the gain register to values far below the scaling factor of 1.0. In extreme cases, the ADC may over-scale. Avoid connecting analog inputs to voltages greater than VREF/gain . Exercise caution when using FSC to increase digital gain. No special care is needed when achieving a custom digital gain less than 20% above the nominal value and with offset less than 40% of full scale. When the digital gain is more than 20% above the nominal value and offset is greater than 40% of full scale, ensure the offset and gain registers meet the conditions of Equation 18.

$$2V/\text{Gain Scaling} - 1.125V > |\text{Offset Scaling}| \qquad \text{(Equation 18)}$$

## Offset Calibration Register: OFC[2:0]

The offset calibration register is a 24-bit word consisting of three 8-bit registers. The offset is in two's complement format, with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. This value is subtracted from the converted data. The register value 000000h does not provide offset correction. Note that although the offset calibration register value can correct offsets in the range of –FS to +FS (as shown in Table 10), analog input overload should be avoided.

Table 10. Relationship between the final output code and the offset calibration register settings

| Offset Register | Final output code VIN = 0 (1) |
|---|---|
| 7FFFFFh | 800000h |
| 000001h | FFFFFFh |
| 000000h | 000000h |
| FFFFFFh | 000001h |
| 800000h | 7FFFFFh |

(1) Eliminate the influence of noise and inherent misalignment error.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## Full-Scale Calibration Register: FSC[2:0]

The full-scale or gain calibration register is a 24-bit word composed of three 8-bit registers. The full-scale calibration value is a 24-bit direct binary value, normalized to 1.0 at code 400000h. Table 11 summarizes the scaling of the full-scale register. Note that while the full-scale calibration register can correct for gain errors greater than 1 (gain adjustment less than 1), ensure that analog input overload is avoided. The default or reset value of the FSC depends on the PGA gain setting. Different factory-adjusted FSC reset values are stored for each PGA gain setting, thus providing gain accuracy across all device inputs.

Note: The factory-adjusted FSC reset value is automatically loaded whenever the PGA gain setting is changed.

Table 11. Relationship between gain correction factor and full-scale calibration register setting

| Full-scale register | Gain Scale |
|---|---|
| 400000h | 2.0 |
| 200000h | 1.0 |
| 100000h | 0.5 |
| 000000h | 0 |

## Calibration Command

This device provides three types of calibration commands: system gain calibration, system offset calibration, and self-offset calibration. For absolute accuracy, we recommend performing calibration after power-on, temperature changes, gain changes, and, in some cases, channel changes. The DRDY signal goes low upon completion of calibration. The first data after calibration is always valid. Issuing commands during calibration after it has begun will result in data corruption. If this occurs, either resend the aborted calibration command or issue a device reset command.

## System Offset and Self-Offset Calibration

System offset calibration corrects for both internal and external offset errors. System offset calibration is initiated by sending the SYSOCAL command, simultaneously applying a zero-differential input (VIN=0) to the selected analog input, while the input is within its common-mode range, ideally the intermediate supply voltage. Self-offset calibration is initiated by sending the self-focus command. During self-offset calibration, the selected input is disconnected from internal circuitry, a zero-differential signal is applied internally, and the input is connected to the intermediate supply. The offset calibration register (OFC) is updated after both offset calibrations. When either offset calibration command is issued, the device stops the current conversion and immediately begins the calibration procedure. Offset calibration should be performed before gain calibration.

## System Gain Calibration

System gain calibration corrects for gain errors in the signal path. System gain calibration is initiated by sending the SYSGCAL command when a full-scale input is applied to a selected analog input. The Full-Scale Calibration Register (FSC) is then updated. When the system gain calibration command is issued, the device stops the current conversion and immediately begins the calibration procedure.

## Calibration Time

When calibration is initiated, the device performs 16 consecutive data conversions and averages the results to calculate the calibration value. This provides a more accurate calibration value. The calibration time is shown in Table 12 and can be calculated using Equation 19: Calibration Time = $t_{CAL} + 50/f_{CLK} + 32/f_{MOD} + 16/f_{DATA}$ (Equation 19) Note: where $f_{DATA}$ is the data rate.

Table 12. Relationship between calibration time and data rate

| Data rate (SPS) | Calibration time ( $t_{CAL}$ ) (ms) |
|---|---|
| 5 | 3201.01 |
| 10 | 1601.01 |
| 20 | 801.012 |
| 40 | 400.26 |
| 80 | 200.26 |
| 160 | 100.14 |
| 320 | 50.14 |

## Programming : Serial Interface

This device provides an SPI-compatible serial communication interface and a data ready signal (DRDY). Communication is full-duplex, except for some limitations of the RREG and RDATA commands. These limitations are explained in detail in the commands. For the basic serial interface timing characteristics, please refer to Figures 1 and 2 of this document.

## Film Selection (CS)

The CS pin activates SPI communication. CS must be low before data transmission and must remain low throughout the entire SPI communication cycle. When CS is high, the DOUT/DRDY pin enters a high-impedance state. Therefore, serial interface read/write operations are ignored, and the serial interface is reset. The DRDY pin operates independently of CS. Even if CS is high, DRDY will still indicate that a new transition has been completed and will be forcibly pulled high in response to SCLK.

Pulling CS high only disables SPI communication with the device. Data conversion continues, and the DRDY signal can be monitored to check if a new conversion result is ready. The master monitoring the DRDY signal can select the appropriate slave by pulling the CS pin low.

## Serial Clock (SCLK)

SCLK provides the clock for serial communication. SCLK is a Schmitt trigger input, but we recommend keeping it as free from noise as possible to prevent glitches from unintentionally shifting data. Data is shifted into DIN on the falling edge of SCLK and out dout on the rising edge of SCLK.

## Data Input (DIN)

DIN, along with SCLK, is used to send data to the device. Data on DIN is shifted into the device on the falling edge of SCLK.

The device's communication is essentially full-duplex. Even as data is being shifted out, the device monitors the commands being shifted in. When a command is sent, data is shifted out of the output shift register. Therefore, when shifting out data, ensure that any signals sent to the DIN pin are valid. When no command is sent to the device while reading data, send a NOP command on DIN.


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### Data Ready (DRDY)

When the DRDY pin goes low, it indicates that a new conversion is complete, and the conversion result is stored in the conversion result buffer. After the DRDY goes low, SCLK must remain low for tDTS (see Figure 2) to load the conversion result into the result buffer and the output shift register. Therefore, if the conversion result needs to be read later, no commands should be issued during this period. This restriction only applies when CS is set and the device is in RDATAC mode. When CS is not set, SPI communication with other devices on the SPI bus does not affect the loading of the conversion result. After the DRDY pin goes low, it is forced to go high on the first falling edge of SCLK (so that the DRDY pin can poll 0 instead of waiting for the falling edge). If the DRDY pin does not go high after the SCLKs clock cycle after going low, a short high-level pulse lasting tPWH indicates that new data is ready.



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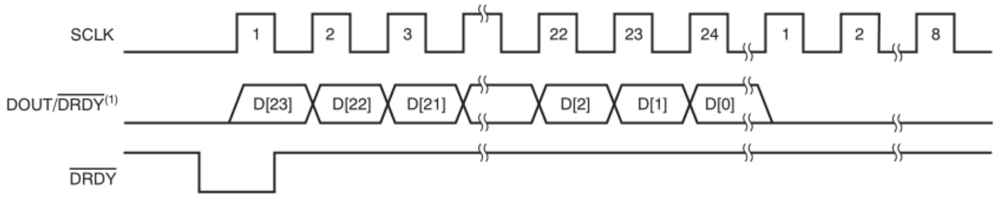
## Data Output and Data Readiness (DOUT/DRDY)

The OUT/DRDY pin has two modes: Data Output Only (DOUT) or DOUT Combined with Data Ready (DRDY). The DRDY mode bit determines the function of this pin and can be found in the IDAC0 register of the DADS1246. In either mode, the DOUT/DRDY pin enters a high-impedance state when CS goes high.

When the DRDY mode bit is set to 0 , this pin is used only for DOUT. Data is output sequentially on the rising edge of SCLK, with MSB priority (as shown in Figure 21).

When the DRDY mode is set to 1, this pin is used for both DOUT and DRDY. Like DOUT, data is shifted out, but this pin adds DRDY functionality. Note that this mode is unavailable if the device is in stop-read continuous data mode when the SDATAC command is issued.

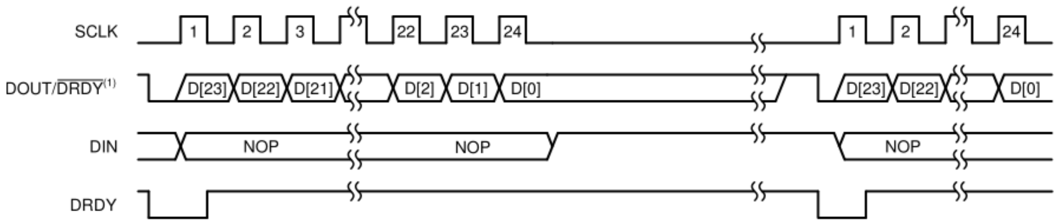
The DRDY mode bit only modifies the functionality of the DOUT/DRDY pins. The functionality of the DRDY pins remains unaffected.




(1) CS is connected to a low level

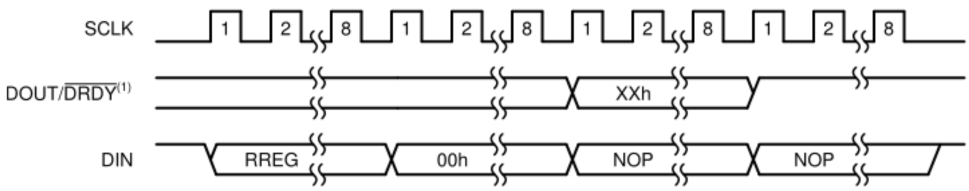
Figure 21. Data retrieval when DRDY mode bit = 0 ( disabled )

When the DRDY mode bit is enabled and a new conversion is complete, DOUT/DRDY will go low if it was high. If it was already low, DOUT/DRDY will first go high and then low (as shown in Figure 22). Similar to the DRDY pin, a falling edge on the DOUT/DRDY pin indicates that a new conversion result is ready. After DOUT/DRDY goes low, if the device is in continuous read mode, data can be output sequentially by providing 24 SCLKs. For the RREG command, the first rising edge of the SCLK forces DOUT/DRDY high after all register bits have been read. Figure 23 shows an example where sending an additional NOP command after reading a register with the RREG command forces the DOUT/DRDY pin high.




(1) CS is connected to a low level.

Figure 22. DRDY Data retrieval ( enabled ) when mode bit = 1




(1) DRDY mode bit enabled, CS connected to low level.

Figure23. After reading the register data, DOUT/ DRDY is forced high

## SPI Reset

There are several ways to reset SPI communication. To reset the serial interface (without resetting registers or digital filters), pull the CS pin high. Pulling the RESET pin low will reset the serial interface and all other digital functions. It will also restore all registers to their default values and begin a new transition.

In systems where CS is permanently connected low, register write operations must always be completed in 8-bit increments. If a minor fault on SCLK interrupts SPI communication, the device will not recognize the command. If data is corrupted and the CS pin is permanently held low, the device will perform a timeout for all listed commands. The SPI timeout will reset the interface if 64 transition cycles are idle.

## SPI Communication in Power-Down Mode

When the START pin is low or the device is in power-down mode, only the RDATA, RDATAC, SDATAC, WAKEUP, and NOP commands can be issued. The RDATA command can be used to repeatedly read the last conversion result in power-down mode. Other commands have no effect because the internal clock is turned off in power-down mode to save power.

## Data format

This device provides 24 bits of data in binary two's complement format. The size of a code (LSB) is calculated using Equation 20: $1LSB = (2 \times V_{REF} / Gain) / 2^{24} = +FS/ 2^{23}$ (Equation 20)

A positive full-scale (FS) input [VIN ≥ (+FS − 1 LSB) = (VREF / gain − 1 LSB)] produces an output code of 7FFFFFh, while a negative full-scale input (VIN ≤ −FS = −VREF / gain) produces an output code of 800000h. For signals exceeding full scale, the output is clipped at these codes. Table 13 summarizes the ideal output codes for different input signals.

Table 13. Relationship between ideal output code and input signal

| Input signal, VIN(AINP − AINN) | Ideal output code (1) |
|---|---|
| $\geq FS (2^{23} - 1)/2^{23}$ | 7FFFFFh |
| $FS / 2^{23}$ | 000001h |
| 0 | 000000h |
| $- FS /2^{23}$ | FFFFFFh |
| ≤ −FS | 800000h |

The effects of noise, linearity, offset, and gain error are eliminated.

The mapping from analog input signal to output code is shown in Figure 24.

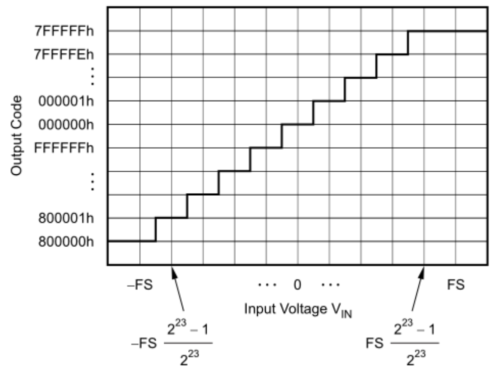



Figure 24. Code Conversion Diagram

## Command

The device provides 13 commands to control its operation, as shown in Table 14. Some commands are independent (WAKEUP, SLEEP, SYNC, RESET, SYSOCAL, SYSGCAL, and SELFOCAL). There are also three commands for controlling data reading from the device (RDATA, RDATAC, and SDATAC). Commands for reading from the device (RREG) and writing to the device (WREG) configuration register data require additional information as part of the instruction. No-Operation (NOP) commands can be used to output data from the device one by one without requiring individual command input.

Operands:

• n = number of registers to read or write (bytes – 1)

• r = registers (0 to 15)

• x = doesn't care

Table 14. SPI Commands

| Command | Description | First command byte | Second command byte |
|---|---|---|---|
| WAKEUP | Exit power saving mode | 0000 000x(00h,01h) | |
| SLEEP | Enter power saving mode | 0000 001x(02h,03h) | |
| SYNC | Synchronous ADC conversion | 0000 010x(04h,05h) | 0000 010x(04h,05h) |
| RESET | Reset to default value | 0000 011x(06h,07h) | |
| START/SYNC | Command and control conversion | 0000 100x(08h,09h) | |
| STOP | Stop command control conversion | 0000 101x(0ah,0bh) | |
| NOP | No operation | 1111 1111(FFh) | |
| RDATA | Read data once | 0001 001x(12h, 13h) | |
| RDATAC | Read data continuously mode | 0001 010x(14h, 15h) | |
| SDATAC | Stop reading data in continuous mode | 0001 011x(16h, 17h) | |
| RREG | From register rrrr read | 0010 rrrr(2xh) | 0000 nnnn |
| WREG | Write to register rrrr | 0100 rrrr(4xh) | 0000 nnnn |
| SYSOCAL | System offset calibration | 0110 0000(60h) | |
| SYSGCAL | System gain calibration | 0110 0001(61h) | |
| SELFOCAL | Self-off calibration | 0110 0010(62h) | |

## WAKEUP(0000 000x)

Use a wake-up command to power on the device after a sleep command. After the wake-up command is executed, the device powers on on the falling edge of the eighth SCLK.



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## SLEEP(0000 001x)

The SLEEP command puts the device into power-saving mode. When the SLEEP command is issued, the device completes the current transition and then enters power-saving mode. Note that this command does not automatically shut down the internal reference voltage source; see the VREFCON bit of each device in MUX1 for details. To exit power-down mode, issue a wake-up command. A single transition can be performed by issuing a wake-up command followed by a SLEEP command. Both WAKEUP and SLEEP are software commands, equivalent to using the START pin to control the device, as shown in Figure 25. Note that if the START pin is held low, or if the START/SYNC command controls the single transition mode, the wake-up command will not power on the device. When using the SLEEP command, CS must be held low during power-down mode.

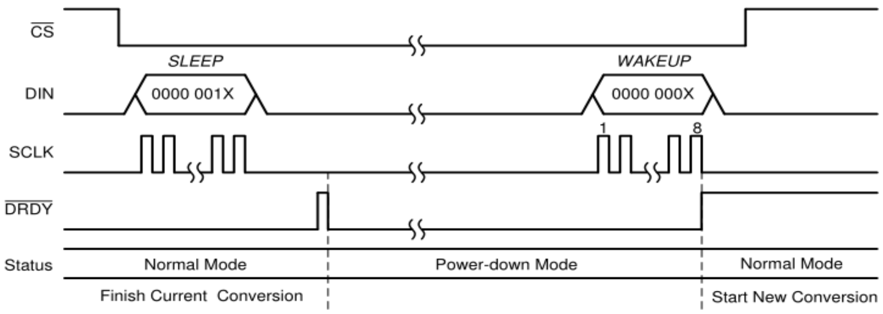


Figure 25. Sleep and Wake-up Command Operation

## SYNC(0000 010x)

The SYNC command resets the ADC digital filter and initiates a new conversion. Multiple devices connected to the same SPI bus can be synchronized by simultaneously issuing the SYNC command to all devices on their DRDY pins .

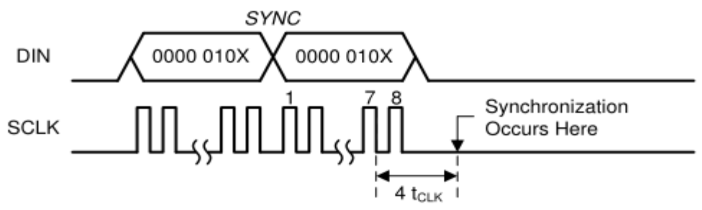


Figure 26. Synchronous Command Operation

## RESET (0000 011x)

The RESET command restores the registers to their default values. This command also resets the digital filter. The RESET command is equivalent to using the RESET pin to reset the device. However, the RESET command does not reset the serial interface. If a reset command is issued when the serial interface is out of sync due to a glitch on SCLK, the device will not reset. The CS pin can be used to reset the serial interface first, and then a reset command can be issued to reset the device. When the system clock frequency is 4.096MHz, the reset command keeps the registers and decimation filter in a reset state for 0.6ms, similar to a hardware reset. Therefore, SPI communication can only be initiated 0.6ms after the RESET command is issued, as shown in Figure 27.

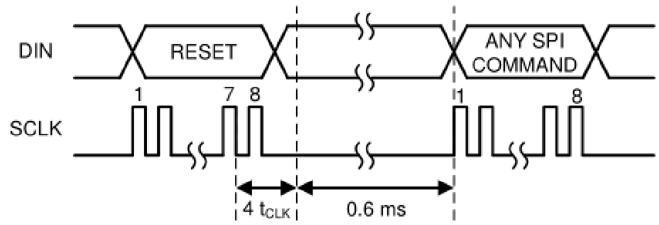


Figure 27. SPI Communication After SPI Reset

## START/SYNC (0000 100x)

The START/SYNC command controls the device to enter command-controlled conversion mode. In single-trigger mode, the START/SYNC command is used to initiate a single conversion, or (when sent during an ongoing conversion) to reset the digital filter and then restart a new single conversion. When the device is set to continuous conversion mode, a START/SYNC command must be issued to begin continuous conversion. During conversion in continuous conversion mode, sending the START/SYNC command resets the digital filter and restarts the continuous conversion.

## STOP (0000 101x)

When the device is in START/SYNC command control switching mode, it can exit this mode by sending a STOP command. The device is powered on on the falling edge of the eighth SCLK.

## RDATA (0001 001x)

The RDATA command loads the most recent conversion result into the output register. After issuing this command, the conversion result is read by sending 24 SCLKs, as shown in Figure 28. This command also applies to RDATAC mode.

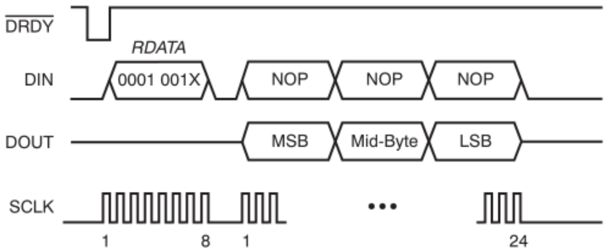


Figure 28. Read data once

When performing multiple reads on the conversion result, the full-duplex communication feature of the serial interface is utilized. When the last 8 bits of the conversion result are shifted out during the first read operation, the RDATA command can be sent, as shown in Figure 29.

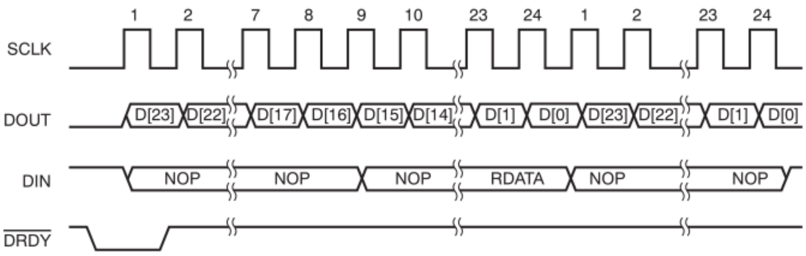


Figure 29. Use in full-duplex mode RDATA

## RDATAC (0001 010x)

The RDATAC command enables continuous read mode. This is the default mode after power-on or reset. In continuous read mode, new conversion results are automatically loaded into DOUT. Conversion results can be received from the device after the DRDY signal goes low by sending 24 SCLKs. It is not necessary to read back all bits as long as the number of bits read is a multiple of 8. The RDATAC command must be issued after DRDY goes low, and the command takes effect on the next DRDY. Ensure that data retrieval (conversion result or register readback) is completed before DRDY returns low; otherwise, the resulting data will be corrupted. Successful register read operations in RDATAC mode require knowledge of when the next falling edge of DRDY occurs.

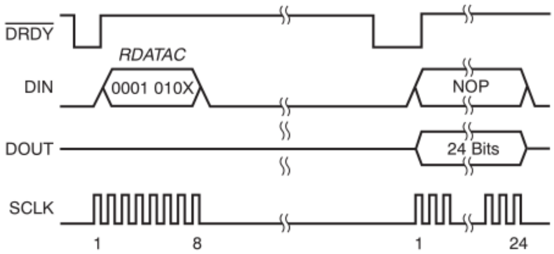

Figure 30. Continuous data reading

## SDATAC (0001 011x)

The SDATAC command terminates continuous data read mode. In continuous data read mode, when DRDY goes low, the conversion result is not automatically loaded into DOUT; register read operations can be performed without interruption due to the loading of a new conversion result into the output shift register. Use the RDATA command to retrieve the converted data. The SDATAC command takes effect after the next DRDY. If there is no active monitoring of DRDY data conversions, stopping continuous data reading mode is the preferred method for reading data. In this mode, the completion of a new ADC conversion will not interrupt the reading of ADC data.

## RREG (0010rrrr, 0000nnnn)

The RREG command starts at the register address specified in the instruction and outputs data from up to 15 registers. The number of registers read is 1 plus the value of the second byte. If the count exceeds the remaining registers, the address returns to the starting position. The two-byte command structure of RREG is shown below.

- First command byte: 0010 rrrr, where rrrr is the address of the first register to be read
- Second command byte: 0000 nnnn, where nnnn is the number of bytes to read – 1
- Byte: Data read from the register is output via nop

When reading register data, the full-duplex feature of the serial interface cannot be used. For example, when reading VBIAS and MUX1 data, the SYNC command cannot be issued, as shown in Figure 31. Any commands sent during register data reading will be ignored. Therefore, we recommend sending nop via DIN when reading register data.

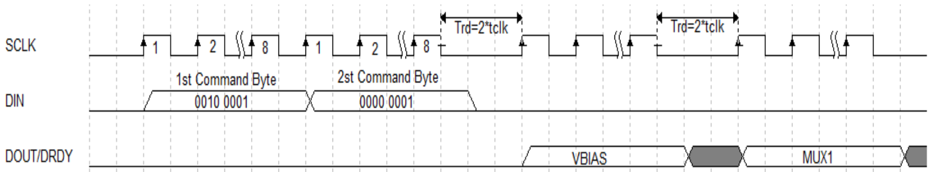

Figure 31a. Reading from the register (SCLK frequency 1MHz and above timing)

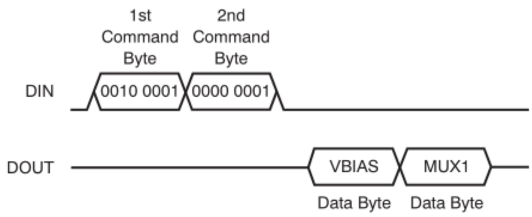

Figure 31b. Reading from the register (SCLK frequency 1MHz and below timing)

## WREG (0100rrrr,0000nnnn)

The WREG command writes to registers, starting with the register specified in the instruction. The number of registers written is 1 plus the value of the second byte. The command structure for WREG is shown below

- First command byte: 0100rrrr, where rrrr is the address of the first register to be written to
- Second command byte: 0000nnnn, where nnnn is the number of bytes to be written – 1
- Byte: The data to be written to the register

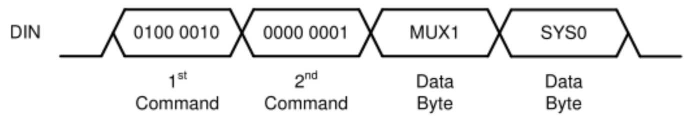


Figure 32. Write to register

## SYSOCAL (0110 0000)

The SYSOCAL command initiates system offset calibration. For system offset calibration, the input must be externally shorted to a voltage within the input common-mode range. The input should be close to the midpoint of the supply voltage (AVDD+AVSS)/2. The OFC register is updated upon command completion. The timing of the calibration command is shown in Figure 33.

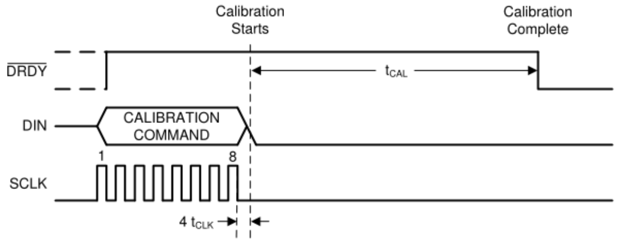


Figure 33. Calibration Command

## SYSGCAL (0110 0001)

The SYSGCAL command initiates system gain calibration. For system gain calibration, the input should be set to full scale. The FSC register is updated after this operation. The timing of the calibration command is shown in Figure 33.

## SELFOCAL (0110 0010)

The SELFOCAL command initiates self-offset calibration. Internally, the device shorts the input to the intermediate power supply and performs the calibration. The OFC register is updated after this operation. The timing of the calibration command is shown in Figure 33.

## NOP (1111 1111)

This is a no-action command. It is used to output data without requiring a command to be entered.


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## DADS1246 Register Mapping

Table 15. DADS1246 Register Mapping

| ADDRESS | REGISTER | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h | MUX0 | BCS[1:0] | | 0 | 0 | 0 | 0 | 0 | 1 |
| 01h | VBIAS | 0 | 0 | 0 | 0 | 0 | 0 | VBIAS[1:0] | |
| 02h | MUX1 | CLKSTAT | 0 | 0 | 0 | 0 | MUXCAL[2:0] | | |
| 03h | SYS0 | CM | PGA[2:0] | | | DR[3:0] | | | |
| 04h | OFC0 | OFC[7:0] | | | | | | | |
| 05h | OFC1 | OFC[15:8] | | | | | | | |
| 06h | OFC2 | OFC[23:16] | | | | | | | |
| 07h | FSC0 | FSC[7:0] | | | | | | | |
| 08h | FSC1 | FSC[15:8] | | | | | | | |
| 09h | FSC2 | FSC[23:16] | | | | | | | |
| 0Ah | ID | ID[3:0] | | | | DRDY MODE | 0 | 0 | 0 |

## Detailed register definitions for DADS1246

### Burn out the current source register (offset = 00h) [reset = 01h]

These bit control sensors burn out the detection current source.

Table 16. Multiplexer Control Registers

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **BCS[1:0]** | | **0** | **0** | **0** | **0** | **0** | **0** |
| **R/W-0h** | | **R-0h** | | | | | |

Example: R/W = Read/Write; R = Read-only; -n = Reset value; -x = Variable

Table 17. Burnout current source register field description

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | BCS[1:0] | R/W | 0h | Failure detection current source register<br>These bit control sensors are set current sources for burnout detection.<br>00: Failure current source is off (default)<br>01: Failure current source activated , 0.5 μA<br>10: Failure current source activated , 2 μA<br>11: Failure current source activated , 10 μA |
| 5:0 | RESERVED | R | 01h | Reserved bits<br>The value is 00001 |


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## Bias voltage register (offset = 01h) [reset = 00h]

Table 18. Bias Voltage Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | VBIAS[1:0] | |
| R-0h R-0h R-0h R-0h R-0h R-0h R/W-00h | | | | | | | |

Example: R/W = Read/Write; R = Read-only; -n = Reset value; -x = Variable

Table 19. Description of the Bias Voltage Register Domain

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:2 | RESERVED | R | 0 h | Reserved bits<br>The value is 000000 |
| 1 | VBIAS[1] | R/W | 0 h | VBIAS[1] V voltage enable<br>The bias voltage applied to AIN1 is the intermediate supply voltage (AVDD + AVSS) / 2.<br>0 : Bias voltage is not enabled (default)<br>1: Bias voltage applied to AINN |
| 0 | VBIAS[0] | R/W | 0 h | VBIAS[0] Voltage Enable<br>The bias voltage applied to AIN 0 is the intermediate supply voltage (AVDD + AVSS) / 2.<br>0 : Bias voltage is not enabled (default)<br>1: Bias voltage applied to AINP |

## Multiplexer control register (offset = 02h) [reset = x0h]

Table 20. Multiplexer Control Register 1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLKSTAT | 0 | 0 | 0 | 0 | MUXCAL[2:0] | | |
| R-xh | R-0h | | | | R/W-0h | | |

Example: R/W = Read/Write; R = Read-only; -n = Reset value; -x = Variable

Table 21. Description of MUX — Multiplexer Control Register Field

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CLKSTAT | R | xh | Clock status<br>This bit is read-only, indicating that an internal oscillator or an external clock is being used.<br>0: Use internal oscillator<br>1: An external clock is being used. |
| 6:3 | RESERVED | R | 0h | The reserved bit value is 0000 |
| 2:0 | MUXCAL[2:0] (1) | R/W | 0h | System monitoring<br>These bits are used to select the system monitor. The MUXCAL selection overrides the selection of the MUX0, MUX1, and VBIAS registers (including MUX_SP, MUX_SN, VBIAS, and reference voltage selection).<br>000: Normal operation (default)<br>001: Offset calibration. Analog input disconnected; AINP and AINN internally connected to intermediate power supply (AVDD + AVSS) / 2.<br>010: Gain calibration. Analog input connected to reference voltage source.<br>011: Temperature measurement. The input is connected to a diode circuit that generates a voltage proportional to the ambient temperature of the device .<br>101: REF monitor. Analog input disconnected, AINP and AINN internally connected to (V(ref P0) - V(ref n0))/4<br>110: Analog power supply monitor. Analog input disconnected, AINP and AINN.<br>Internally connected to (AVDD – AVSS)/4<br>111: Digital power supply monitor. Analog input disconnected; AINP and AINN internally connected to (DVDD – DGND)/4. |

(1) When using any reference voltage monitor, the internal reference voltage should be enabled.

Table 22 provides the ADC input connections and PGA settings for each MUXCAL configuration. When the MUXCAL resumes normal operation or offset measurement, the PGA settings revert to the original SYS0 register settings.

Table 22. Multiplexer Control Settings

| MUXCAL[2:0] | PGA gain settings | ADC input |
|---|---|---|
| 000 | Set by SYS0 register | Normal operation |
| 001 | Set by SYS0 register | Short the input to the intermediate power supply (AVDD + AVSS) / 2 |
| 010 | Forced 1 | $V_{(REFP)} - V_{(REFN)}$ (Full Scale) |
| 011 | Forced 1 | Temperature measurement diode |

## System control register 0 (offset = 03h) [reset = 00h]

Table 23. System Control Register 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CM | PGA[2:0] | | | DR[3:0] | | | |
| R/W-0h | R/W-0h | | | R/W-0h | | | |

Example: R/W = Read/Write; R = Read-only; -n = Reset value; -x = Variable

Table 24. Description of System Control Register 0 Field

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CM | R/W | 0 h | Switching modes<br>This bit sets the start/synchronization command and controls the switching mode of the device.<br>0: Single conversion mode (default)<br>1: Continuous Conversion Mode |
| 6:4 | PGA[2:0] | R/W | 0 h | PGA gain settings<br>These bits determine the PGA gain.<br>000: PGA = 1 (default)<br>001: PGA = 2<br>010: PGA = 4<br>011: PGA = 8<br>100: PGA = 16<br>101: PGA = 32<br>110: PGA = 64<br>111: PGA = 128 |
| 3:0 | DR[3:0] | R/W | 0 h | Data output rate settings<br>These bits determine the ADC's data output rate.<br>0000: DR = 5 SPS (default)<br>0001: DR = 10 SPS<br>0010: DR = 20 SPS<br>0011: DR = 40 SPS<br>0100: DR = 80 SPS<br>0101: DR = 160 SPS<br>0110: DR = 320 SPS<br>0111: DR = 640 SPS<br>1000: DR = 1000 SPS<br>1001 to 1111: DR = 2000 SPS |

## Offset calibration coefficient register (offset = 04h, 05h, 06h) [reset = 00h, 00h, 00h]

Table 25. Offset Calibration Coefficient Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OFC[7:0] | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OFC[15:8] | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OFC[23:16] | | | | | | | |
| R/W-0h | | | | | | | |

Example: R/W = Read/Write; R = Read-only; -n = Reset value; -x = Variable

Table 26. Description of Offset Calibration Coefficient Register Field

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23:0 | OFC[23:0] | R/W | 0 00000h | Offset Calibration Register<br>Three registers form the ADC 24-bit offset calibration word. This 24-bit word is in two's complement format and is internally left-shifted to align with the ADC 24-bit conversion result. Before full-scale operation, the ADC subtracts the register value from the conversion result. |

## Full-scale calibration coefficient register (offset = 07h, 08h, 09h) [reset = PGA related]

These bits constitute the full-scale calibration coefficient register. For each PGA setting, the FSC reset value is factory-adjusted. Whenever the PGA setting changes, the factory-adjusted FSC reset value is automatically loaded.

Table 27. Full -scale calibration coefficient register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FSC[7:0] | | | | | | | |
| R/W-00h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FSC[15:8] | | | | | | | |
| R/W-00h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FSC[23:16] | | | | | | | |
| R/W-20h | | | | | | | |

Example: R/W = Read/Write; R = Read-only; -n = Reset value; -x = Variable

Table 28. Description of Full-Scale Calibration Coefficient Register Field

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23:0 | FSC[23:0] | R/W | 200000h | Full-scale calibration register<br>Three registers form the ADC's 24-bit full-scale calibration word. The 24-bit word is standard binary. The ADC stores the gain coefficient obtained after gain calibration in the FSC register, and then multiplies the scaling factor by the conversion result. Whenever the PGA setting changes, the factory-tuned FSC reset value is automatically loaded. |

### Control register 0 (offset = 0Ah) [reset = x0h]

Table 29. ID Control Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ID[3:0] | | | | DRDY MODE | 0 | 0 | 0 |
| R-xh | | | | R/W-0h | R-0h | | |

Example: R/W = Read/Write; R = Read-only; -n = Reset value; -x = Variable

Table 30. Description of ID Control Register Field

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:4 | ID[3:0] | R | x h | Version identifier<br>Read-only, factory programming bit; used for version identification |
| 3 | DRDY MODE | R/W | 0 h | Data ready mode settings<br>This bit sets the function of the DOUT/DRDY pin. In either setting of the DRDY mode bit, the dedicated DRDY pin continues to indicate data ready, active low.<br>0 : The DOUT/DRDY pin is used for data output only (default).<br>1: The DOUT/DRDY pin is used for both data output and data ready.<br>Active low (1) |
| 2:0 | RESERVED | R | 0 h | Reserved bits<br>The value is 000 |

(1) Cannot be used in SDATAC mode

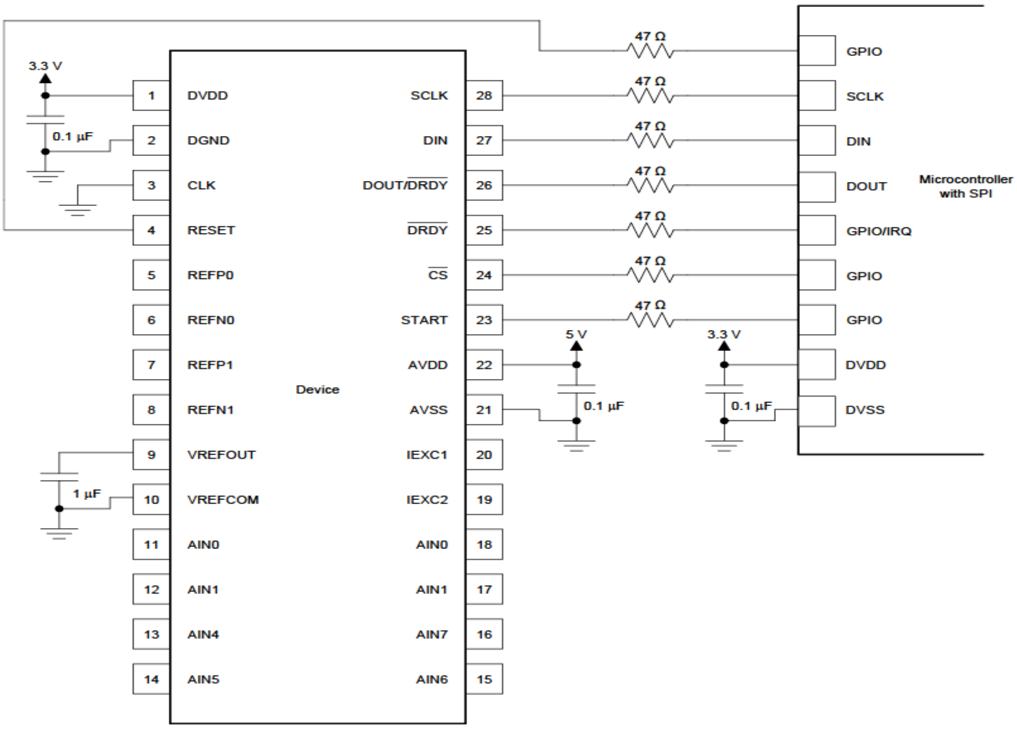
## Application and Implementation

The DADS1246 is a 24-bit ADC that offers many integrated features, making it easy to measure the most common sensor types, including a variety of temperature and bridge sensors. Key considerations when designing applications using these devices include connecting and configuring the serial interface, designing analog input filtering, establishing a suitable external reference voltage source for ratio measurements, and setting the common-mode input voltage for the internal PGA. These considerations will be discussed in the following sections.

## Serial Interface Connection

The serial interface connection principle of DADS1246 is shown in Figure 34.

Figure 34 . Serial interface connection




Most microcontroller SPI peripherals can work with the MCT1246. This interface operates in SPI mode 1, where CPOL=0 and CPHA=1. In SPI mode 1, SCLK is low and idle; data is sent or modified only on the rising edge of SCLK; data is latched or read by the master and slave on the falling edge of SCLK.

We recommend connecting a 47-Ω resistor in series with all digital input and output pins (CS, SCLK, DIN, DOUT/DRDY, DRDY, RESET, and START). This resistor smooths sharp transitions, suppresses overshoot, and provides some overvoltage protection. Care must be taken to meet all SPI timing requirements, as the additional resistor can interfere with bus capacitance on the digital signal lines.

## Analog Input Filtering

Analog input filtering serves two purposes: first, to limit aliasing during the sampling process; and second, to reduce external noise during measurement.

Many sensor signals inherently have limited bandwidth; for example, a thermocouple has a finite rate of change of output. In such cases, when using a ΔΣADC, the sensor signal will not alias back into the passband. However, any noise picked up along the sensor wiring or application circuitry can potentially alias into the passband.

## External Reference and Ratio Measurement

The full-scale range of the DADS1246 is defined by the reference voltage and the PGA gain (FSR = ±VREF/gain). An external reference can be used instead of the integrated 2.048V reference to adapt the FSR to specific system requirements. If VIN > 2.048V, an external reference must be used. For example, to measure signals up to 2.5V, an external 2.5V reference is required. Note that the input signal must be within the common-mode input range to be valid, and the reference input voltage must be between 0.5V and (AVDD - AVSS - 1V).

## Establish an Appropriate Common-Mode Input Voltage

The DADS1246 is used to measure various types of signal configurations. However, it is important to correctly configure the device's inputs for the corresponding signal type.

The DADS1246 features one differential input, ensuring that all inputs, including the common input, are within the common-mode input voltage range, regardless of the analog input configuration.

## Isolated (or Floating) Sensor Input

Isolated sensors (sensors without a reference to ADC ground) must establish a common-mode voltage within the specified ADC input range. The common-mode voltage level is shifted by biasing with an external resistor, either by connecting the negative lead to ground (bipolar analog supply) or by connecting to a DC voltage (unipolar analog supply). A 2.048V reference output voltage can also be used to provide level shifting for floating sensor inputs.

## Unused Inputs and Outputs

To minimize leakage current on analog inputs, unused analog inputs can be floated, connected to an intermediate power supply, or connected to AVDD. Connecting unused analog inputs to AVSS is also possible, but this will result in higher leakage current than the options mentioned above.

Do not float unused digital inputs, as this may cause excessive power leakage current. Connect all unused digital inputs to the appropriate level, DVDD or DGND, including in power-down mode. If the DRDY output is not used, leave the off-pin unconnected or tie it to DVDD using a weak pull-up resistor.

## Power Supply Recommendations

The device requires two power supplies: an analog power supply (AVDD, AVSS) and a digital power supply (DVDD, DGND). The analog power supply can be bipolar (e.g., AVDD=2.5V, AVSS=-2.5V) or unipolar (e.g., AVDD=3.3V, AVSS=0V) and is independent of the digital power supply. The digital power supply sets the digital I/O levels (except for GPIO levels, which are set by the analog power supply from AVDD to AVSS).

## Power Supply Sequencing

The power supplies can be arranged in any order, but under no circumstances can any analog or digital input exceed its respective analog or digital power supply voltage limit. After all power supplies have stabilized, wait at least $2^{16}$ $t_{CLK}$ cycles before communicating with the device to complete the power-on reset process.



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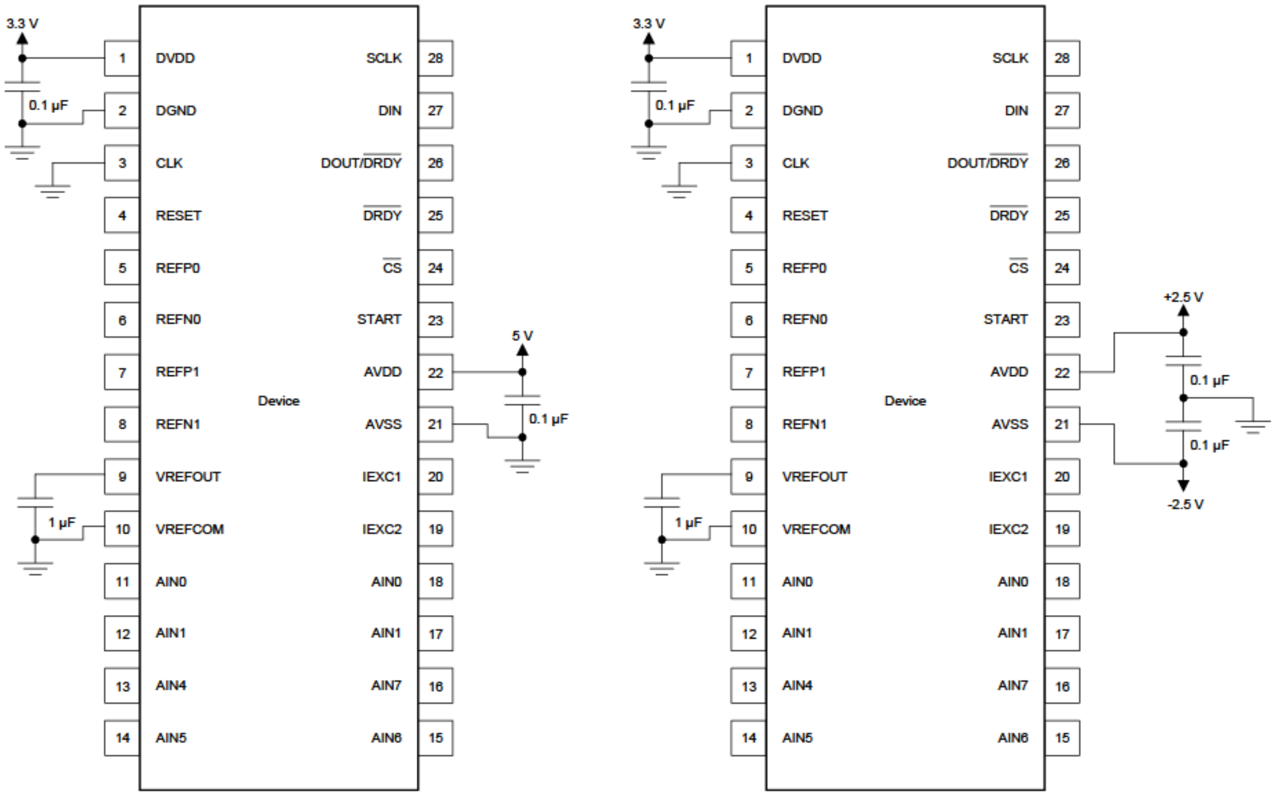
## Power Supply Decoupling

Proper power supply decoupling is crucial for optimal performance. AVDD, AVSS (when using a bipolar power supply), and DVDD must be decoupled with capacitors of at least 0.1 µF, as shown in Figure 35. Use low-impedance connections and place bypass capacitors as close as possible to the device's power supply pins. We recommend using multilayer ceramic chip capacitors (MLCCs) to provide power supply decoupling with low equivalent series resistance (ESR) and inductance (ESL) characteristics. For highly sensitive systems or systems in harsh, noisy environments, avoiding the use of vias to connect capacitors to device pins provides superior noise immunity. The use of multiple vias in parallel reduces overall inductance and facilitates connections to the ground plane. We recommend connecting analog and digital grounds together, as close as possible to the device.

Figure 35. Power decoupling in unipolar and bipolar power supply operation

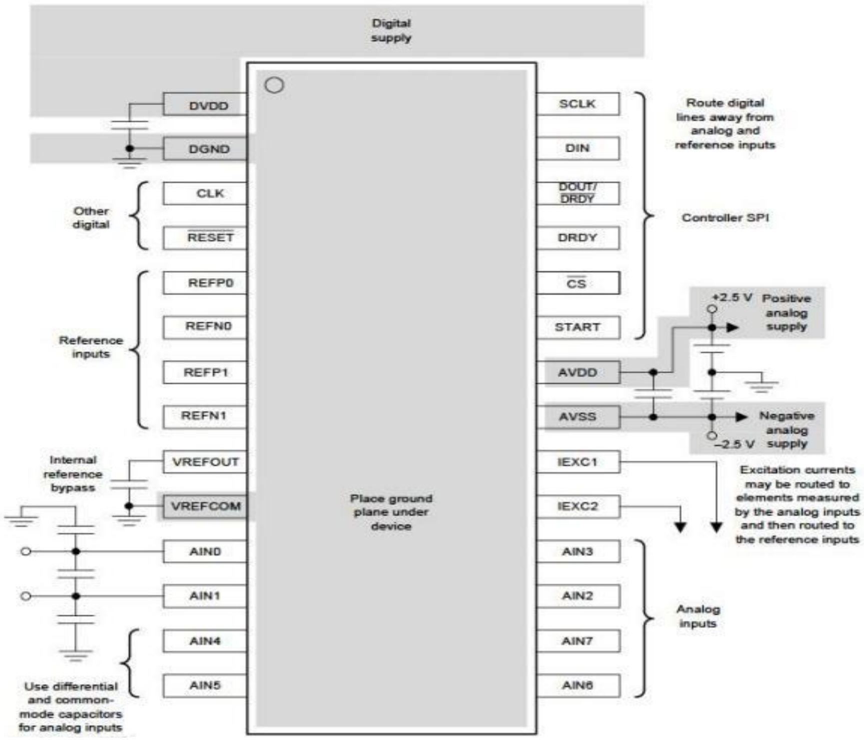



## Layout Guide

We recommend using best design practices when laying out printed circuit boards (PCBs) for analog and digital components. This recommendation generally means separating analog components [such as ADCs, amplifiers, reference devices, digital-to-analog converters (DACs), and analog muxes] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators].

## Layout Example

Figure 36. DADS1246 layout example




## Device Ordering Information

| Product Model | Temperature Range | Packaging Type | Package Quantity | RoHS |
|---|---|---|---|---|
| **DADS1246** | -40 °C to +85 °C | 16 - TSSOP | 1000/reel | Y |
| | | | | |