

Function Description

- Eight low-noise programmable gain amplifiers (PGAs) and eight high-resolution analog-to-digital converters (ADCs).
- Sampling rate: 250SPS to 32kSPS
- Low power consumption: 0.75mW per channel
- Full-temperature range input bias current: 1.5nA
- Common-mode rejection ratio (CMRR): -118dB
- Programmable gain: 1, 2, 3, 4, 6, 8, 12
- Supports systems that meet AAMI EC11, EC13, ICE60601-1, IEC60601-2-27 and IEC60601-2-51 standards.
- SPI™ compatible serial port
- Built-in right leg drive amplifier, lead disconnection detection, Wilson central terminal, pacing detection, test signal
- Digital pacing detection function
- Built-in oscillator and reference
- Single-pole or bipolar power supply:
 - AVDD: 2.7V to 5.25V
 - DVDD: 1.65V to 3.6V

Applications

- Medical instruments (electrocardiogram (ECG), electromyography (EMG), and electroencephalography (EEG))
- Patient monitoring: Holter monitoring, time, stress, and vital signs, including ECG, AED, telemedicine, and sleep monitoring.
- Sound effects/dynamic strain gauges
- Pressure sensor

Description

The DADS1294, DADS1296, and DADS1298 are a family of multi-channel, synchronous sampling 24-bit delta - sigma analog-to-digital converters (ADCs) with integrated programmable gain amplifiers (PGA), internal references, and onboard oscillators.

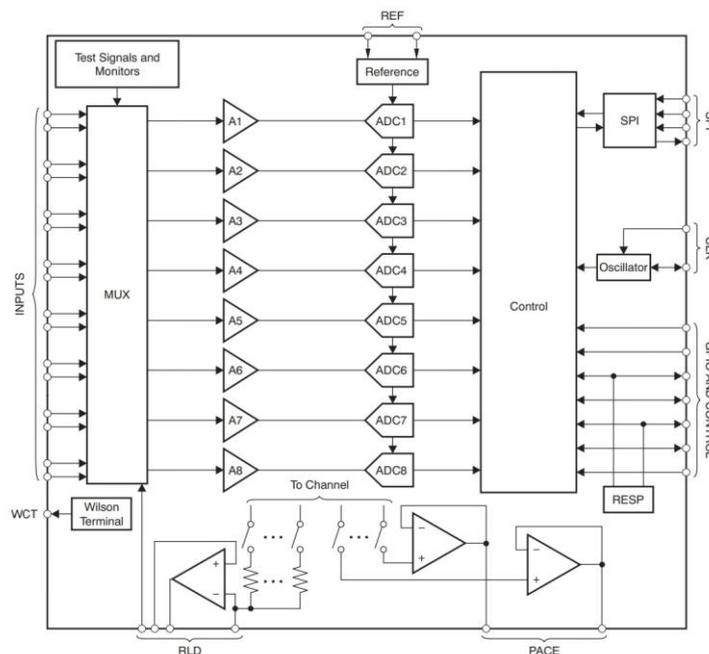
The DADS129x includes all the functionality typically required in medical electrocardiogram (ECG) and electroencephalogram (EEG) applications where these values must be kept to a minimum. With its high integration and excellent performance, the DADS129x enables the development of scalable medical instrument systems in a significantly reduced size, with significantly lower power consumption and overall cost.

Each channel of the DADS129x features a flexible input multiplexer (mux) that can be independently connected to internally generated signals for testing, temperature, and lead disconnection detection. Additionally, any configuration of the input channel can be selected to generate a right leg drive (RLD) output signal.

The DADS129x operates at a data rate of up to 32kSPS, enabling software pacing detection. Lead disconnection detection can be achieved internally via pull-up/pull-down resistors or an excitation current trap/current source. Three integrated amplifiers generate the Wilson center termination (WCT) and Goldberg center termination (GCT) required for a standard 12-lead ECG. Multiple DADS129x devices can be daisy-chained in high-channel-count systems.

The package option is TQFP-64.

The DADS129x TQFP has an industrial-grade rated temperature range of -40°C to +85°C.



Functional Block Diagram

Absolute Maximum Ratings

Unless otherwise stated, operate within the room temperature range ⁽¹⁾.

| | | Min | Max | Unit |
|---------------------------------------|---------------|------------|------------|------|
| AVDD to AVSS | | -0.3 | 5.5 | V |
| DVDD to DGND | | -0.3 | 3.9 | V |
| AVSS to DGND | | -3 | 0.2 | V |
| AVSS VREFP input | | AVSS – 0.3 | AVDD + 0.3 | V |
| Analog input voltage | | AVSS – 0.3 | AVDD + 0.3 | V |
| Digital input voltage | | DGND – 0.3 | DVDD + 0.3 | V |
| Digital output voltage | | DGND – 0.3 | DVDD + 0.3 | V |
| Input current | Instantaneous | | 100 | mA |
| | Continuous | | 10 | mA |
| Junction temperature, T _J | | -40 | 150 | °C |
| Storage temperature, T _{STG} | | -60 | 150 | °C |

(1) Stress exceeding these ratings may cause permanent damage. Prolonged exposure to absolute maximum conditions may reduce the reliability of the equipment. These are only stress ratings and do not imply functional operation of the equipment under these conditions or any other conditions exceeding the specified conditions.

Electrical Characteristics

All characteristics are available from -40°C to $+85^{\circ}\text{C}$, with typical specifications applicable to $T_A = 25^{\circ}\text{C}$. $\text{DVDD} = 1.8\text{V}$, $\text{AVDD} - \text{AVSS} = 3\text{V}$ ⁽¹⁾, $\text{VREF} = 2.4\text{V}$, external $f_{\text{CLK}} = 2.048\text{MHz}$, data rate = 500SPS, HR mode ⁽²⁾, and gain = 6, unless otherwise specified.

| Parameter | Test conditions | Min | Typ | Max | Unit |
|--------------------------------------|---|------------------------------------|-------------------------|-----------|---------------------------|
| Analog Input | | | | | |
| Input capacitor | | | 20 | | pF |
| Input bias current | $T_A = 25^{\circ}\text{C}$, Input = 1.5V | | | ± 200 | pA |
| | $T_A = 0^{\circ}\text{C}$ to 70°C , Input = 1.5V | | ± 1 | | nA |
| | $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, Input = 1.5V | | ± 1.2 | | nA |
| DC input impedance | No lead detachment | 1000 | | | $\text{M}\Omega$ |
| | Current source lead disconnection detection | | 500 | | $\text{M}\Omega$ |
| | Pull-up resistor lead detachment detection | | 10 | | $\text{M}\Omega$ |
| PGA performance | | | | | |
| Gain settings | | | 1, 2, 3, 4, 6, 8, 12 | | |
| Bandwidth | | | Please refer to Table 5 | | |
| ADC performance | | | | | |
| Resolution | Data rates up to 8kSPS with no lost codes | 24 | | | Bit |
| | 16kSPS data rate | 19 | | | Bit |
| | 32kSPS data rate | 17 | | | Bit |
| Data rate | $f_{\text{CLK}} = 2.048\text{MHz}$, HR mode | 500 | | 32000 | SPS |
| | $f_{\text{CLK}} = 2.048\text{MHz}$, HR mode | 250 | | 16000 | SPS |
| DC channel performance | | | | | |
| Input reference noise | Gain = 6 ⁽³⁾ , 10 seconds of data | | 5 | | μV_{PP} |
| | Gain = 6, 256 points, 0.5 seconds of data. | | 4 | 7 | μV_{PP} |
| | Gain setting $\neq 6$, data rate $\neq 500\text{SPS}$ | See the noise measurement section. | | | |
| Integral nonlinearity ⁽⁴⁾ | Full scale, gain = 6, best fit | | 8 | | ppm |
| Offset error | | | ± 500 | | |
| Offset error drift | | | 2 | | |
| Gain error | Excluding voltage gain error | | ± 0.2 | ± 0.5 | |
| Gain drift | Excluding voltage reference drift | | 5 | | dB |
| Gain matching between channels | | | 0.3 | | V |

(1) The performance is also applicable to 5V operation. Production testing for the limits is performed at 3V.

(2) LP mode = low power mode.

(3) Noise data tested over a 10-second interval. The test was not performed in production. The input reference noise was calculated by short-circuiting the input (without electrode resistance) over a 10-second interval.

(4) The presence of an internal demodulation circuit on channel 1 will cause INL and THD degradation. This effect is significant for full-scale signals and less so for small ECG signals.

Electrical characteristics (continued)

All characteristics are available from -40°C to +85°C, with typical specifications applicable to $T_A = 25^\circ\text{C}$. $\text{DVDD} = 1.8\text{V}$, $\text{AVDD} - \text{AVSS} = 3\text{V}$ ⁽¹⁾, $\text{VREF} = 2.4\text{V}$, external $f_{\text{CLK}} = 2.048\text{MHz}$, data rate = 500SPS, HR mode ⁽²⁾, and gain = 6, unless otherwise specified.

| Parameter | Test conditions | Min | Typ | Max | Unit |
|---|--|------------|-------------------------|------------|------------------|
| AC channel performance | | | | | |
| Common-mode rejection ratio (CMRR) | FCM = 50Hz, 60Hz ⁽⁵⁾ | -105 | -115 | | dB |
| Power Supply Rejection Ratio (PSRR) | FPS = 50Hz, 60Hz | | 90 | | dB |
| Crosstalk | FIN = 50Hz, 60Hz | | -126 | | dB |
| Signal-to-noise ratio (SNR) | FIN = 10Hz input, gain = 6 | | 112 | | dB |
| Total Harmonic Distortion (THD) | 10Hz, -0.5dBFS | | -98 | | dB |
| | 100Hz, -0.5dBFS ⁽⁶⁾ | | -100 | | dB |
| Digital Filters | | | | | |
| -3dB bandwidth | | | 0.262fDR | | Hz |
| Digital filter stabilization | Completely stable | | 4 | | Conversion |
| Right Leg Drive (RLD) Amplifier and Pacemaker Signal Amplifier | | | | | |
| RLD integral noise | BW = 150Hz | | 7 | | μVRMS |
| Pacemaker signal integral noise | BW = 8kHz | | 20 | | μVRMS |
| Pacemaker signal amplifier crosstalk | Crosstalk between pacemaker signal amplifiers | | 60 | | dB |
| Gain-bandwidth product | 50k Ω 10pF load, gain = 1 | | 100 | | kHz |
| Slewing rate | 50k Ω 10pF load, gain = 1 | | 0.25 | | V/ μs |
| Pacemaker signal and RLD amplifier drive intensity | Short-circuit GND (AVDD = 3V) | | 270 | | μA |
| | For power supply short circuit (AVDD = 3V) | | 550 | | μA |
| | Short-circuit GND (AVDD = 5V) | | 490 | | μA |
| | For power supply short circuit (AVDD = 5V) | | 810 | | μA |
| Pacemaker signal and RLD current | Peak swing (AVSS + 0.3V to AVDD + 0.3V), AVDD = 3V | | 50 | | μA |
| | Peak swing (AVSS + 0.3V to AVDD + 0.3V), AVDD = 5V | | 75 | | μA |
| Pacemaker signal amplifier output resistance | | | 100 | | Ω |
| Total Harmonic Distortion | $f_{\text{IN}} = 100\text{Hz}$, gain = 1 | | -70 | | dB |
| Common mode input range | | AVSS + 0.7 | | AVDD - 0.3 | V |
| Common mode resistor matching | Internal 200k Ω resistor matching | | 0.1% | | |
| Short circuit current | | | ± 0.25 | | mA |
| Static power consumption | RLD or pacemaker signal amplifier | | 20 | | μA |
| Wilson Center Terminal (WCT) Amplifier | | | | | |
| Integral noise | BW = 150Hz | | Please refer to Table 6 | | nV/Hz |
| Gain-bandwidth product | | | Please refer to Table 6 | | kHz |
| Slewing rate | | | Please refer to Table 6 | | V/s |
| Total Harmonic Distortion | $f_{\text{IN}} = 100\text{Hz}$ | | 90 | | dB |
| Common mode input range | | AVSS + 0.3 | | AVDD - 0.3 | V |
| Short circuit current | Through an internal 30k Ω resistor | | ± 0.25 | | mA |
| Static power consumption | | | Please refer to Table 6 | | μA |

(5) CMRR is measured using a common-mode signal from AVSS + 0.3V to AVDD - 0.3V. The values shown are the maximum values for all eight channels.

(6) Harmonics higher than the second harmonic will be attenuated by digital filters.

Electrical Characteristics (continued)

All characteristics are available from -40°C to +85°C, with typical specifications applicable to $T_A = 25^\circ\text{C}$. DVDD = 1.8V, AVDD - AVSS = 3V⁽¹⁾, VREF = 2.4V, external $f_{\text{CLK}} = 2.048\text{MHz}$, data rate = 500SPS, HR mode⁽²⁾, and gain = 6, unless otherwise specified.

| Parameter | Test conditions | Min | Typ | Max | Unit |
|---|--|-----|---|-------|--------|
| Lead detachment detection | | | | | |
| Frequency | For settings details, please refer to Table 6. | | 0, $f_{\text{DR}}/4$ | | kHz |
| Current | For settings details, please refer to Table 6. | | 6, 12, 18, 24 | | nA |
| Current accuracy | | | ±20% | | |
| Comparator threshold accuracy | | | ±30 | | mV |
| External reference | | | | | |
| Input impedance | | | 10 | | kΩ |
| Internal benchmark | | | | | |
| Output voltage | Register bit CONFIG3.VREF_4V = 0, AVDD ≥ 2.7V | | 2.4 | | V |
| | Register bit CONFIG3.VREF_4V = 1, AVDD ≥ 4.4V | | 4 | | V |
| V _{REF} accuracy | | | ±20% | | |
| Internal reference drift | T _A = 25°C | | 35 | | ppm/°C |
| | -40 °C to 85 °C | | 45 | | ppm |
| Startup time | | | 150 | | Ms |
| System monitor | | | | | |
| Analog power supply reading error | | | 2% | | |
| Digital power supply reading error | | | 2% | | |
| Device wake-up | From power-on, DRDY is at a low level. | | 150 | | ms |
| | Standby mode | | 9 | | ms |
| Temperature sensor reading, voltage | T _A = 25°C | | 145 | | mV |
| Temperature sensor reading, coefficient | | | 490 | | μV/°C |
| Test signal frequency | For settings details, please refer to Table 6. | | $f_{\text{CLK}}/2^{21} / f_{\text{CLK}}/2^{20}$ | | Hz |
| Test signal voltage | For settings details, please refer to Table 6. | | ±1, ±2 | | mV |
| Test signal accuracy | | | ±2% | | |
| Clock | | | | | |
| Internal oscillator clock frequency | Nominal frequency | | 2.048 | | MHz |
| Internal clock frequency | T _A = 25°C | | | ±0.5% | |
| | -40°C to 85°C | | | ±2.5% | |
| Internal oscillator start-up time | | | | 20 | μs |
| Internal oscillator power consumption | | | 120 | | μW |

Electrical Characteristics (continued)

All characteristics are available from -40°C to +85°C, with typical specifications applicable to $T_A = 25^\circ\text{C}$. $\text{DVDD} = 1.8\text{V}$, $\text{AVDD} - \text{AVSS} = 3\text{V}$ ⁽¹⁾, $\text{VREF} = 2.4\text{V}$, external $f_{\text{CLK}} = 2.048\text{MHz}$, data rate = 500SPS, HR mode ⁽²⁾, and gain = 6, unless otherwise specified.

| Parameter | Test conditions | | Min | Typ | Max | Unit |
|---|-----------------------------------|---------------------|------------|------|------------|---------------|
| Digital input/output (DVDD = 1.65V to 3.6V) | | | | | | |
| High-level input voltage (V_{IH}) | | | 0.8 DVDD | | DVDD + 0.1 | V |
| Low-level input voltage (V_{IL}) | | | -0.1 | | 0.2 DVDD | V |
| High-level output voltage (V_{OH}) | $I_{\text{OH}} = -500\mu\text{A}$ | | DVDD - 0.4 | | | V |
| Low-level output voltage (V_{OL}) | $I_{\text{OL}} = 500\mu\text{A}$ | | | | 0.4 | V |
| Input current (I_{IN}) | 0V to DVDD | | -10 | | 10 | μA |
| Power supply (RLD, WCT, and pacing signal amplifier off) | | | | | | |
| AVDD current (I_{AVDD}) | AVDD - AVSS = 3V | HR Model (DADS1298) | | 2.75 | | mA |
| | | LP mode (DADS1298) | | 1.8 | | mA |
| | AVDD - AVSS = 5V | HR Model (DADS1298) | | 3.1 | | mA |
| | | LP mode (DADS1298) | | 2.1 | | mA |
| DVDD current (I_{DVDD}) | DVDD = 1.8V | HR Model (DADS1298) | | 0.3 | | mA |
| | | LP mode (DADS1298) | | 0.3 | | mA |
| | DVDD = 3V | HR Model (DADS1298) | | 0.5 | | mA |
| | | LP mode (DADS1298) | | 0.5 | | mA |
| Power dissipation | AVDD - AVSS = 3V (DADS1298) | HR model | | 8.8 | 9.5 | mW |
| | | LP mode (250SPS) | | 6.0 | 7.0 | mW |
| | AVDD - AVSS = 3V (DADS1296) | HR model | | 7.2 | 7.9 | mW |
| | | LP mode (250SPS) | | 5.3 | 6.6 | mW |
| | AVDD - AVSS = 3V (DADS1294) | HR model | | 5.4 | 6 | mW |
| | | LP mode (250SPS) | | 4.1 | 4.4 | mW |
| | AVDD - AVSS = 5V (DADS1298) | HR model | | 17.5 | | mW |
| | | LP mode (250SPS) | | 12.5 | | mW |
| | AVDD - AVSS = 5V (DADS1296) | HR model | | 14.1 | | mW |
| | | LP mode (250SPS) | | 10 | | mW |
| | AVDD - AVSS = 5V (DADS1294) | HR model | | 10.1 | | mW |
| | | LP mode (250SPS) | | 8.3 | | mW |
| Power outage | AVDD - AVSS = 3V | | | 10 | | μW |
| | AVDD - AVSS = 5V | | | 20 | | μW |
| Standby mode | AVDD - AVSS = 3V | | | 2 | | mW |
| | AVDD - AVSS = 5V | | | 4 | | mW |
| Static channel power | AVDD - AVSS = 3V, PGA + ADC | | | 818 | | μW |
| | AVDD - AVSS = 5V, PGA + ADC | | | 1.5 | | mW |

Timing Requirements: Serial Interface

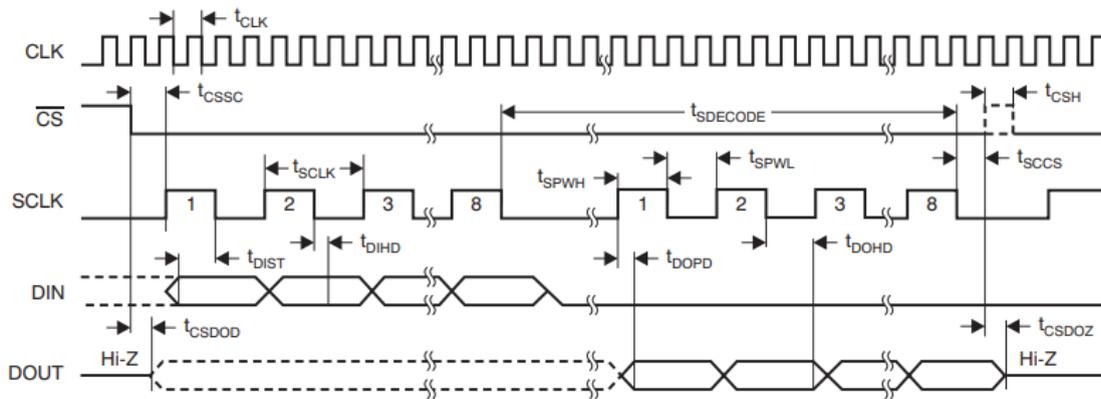
Load on D_{OUT} = 20pF || 100kΩ

| | | 2.7V ≤ DVDD ≤ 3.6V | | 1.65V ≤ DVDD ≤ 2V | | Unit |
|-----------------------|---|--------------------|-----|-------------------|-----|------------------|
| | | Min | Max | Min | Max | |
| t _{CLK} | Master clock cycle | 414 | 514 | 414 | 514 | ns |
| t _{CSSC} | CS low level until the first SCLK, setup time | 6 | | 17 | | ns |
| t _{SCLK} | SCLK cycle | 50 | | 66.6 | | ns |
| t _{SPWH,L} | SCLK pulse width, high level and low level | 15 | | 25 | | ns |
| t _{DIST} | DIN valid until SCLK falling edge, setup time | 10 | | 10 | | ns |
| t _{DIHD} | Effective DIN after the falling edge of SCLK: Hold time | 10 | | 11 | | ns |
| t _{CSH} | CS high-level pulse | 2 | | 2 | | t _{CLK} |
| t _{SCCS} | The eighth falling edge of SCLK leads to a high level on CS | 4 | | 4 | | t _{CLK} |
| t _{SDECODE} | Command decoding time | 4 | | 4 | | t _{CLK} |
| t _{DISCK2ST} | DAISY_IN valid until the rising edge of SCLK: Setup time | 10 | | 10 | | ns |
| t _{DISCK2HT} | DAISY_IN is valid after the rising edge of SCLK: Hold time | 10 | | 10 | | ns |

Switching Characteristics: Serial Interface

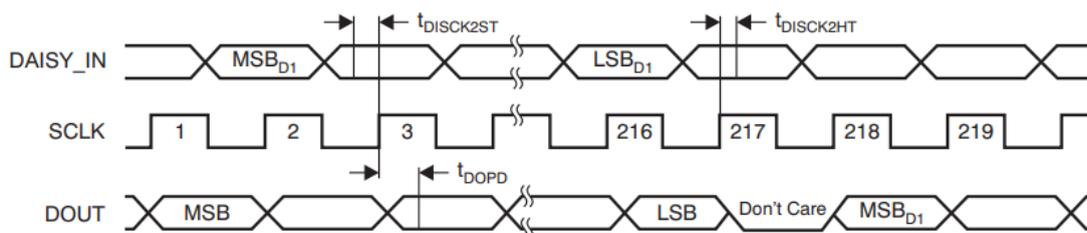
Load on D_{OUT} = 20pF || 100kΩ

| | | 2.7V ≤ DVDD ≤ 3.6V | | 1.65V ≤ DVDD ≤ 2V | | Unit |
|--------------------|--|--------------------|-----|-------------------|-----|------|
| | | Min | Max | Min | Max | |
| t _{DOHD} | SCLK falling edge to invalid DOUT: Hold time | 10 | | 10 | | ns |
| t _{DOPD} | SCLK rising edge to DOUT valid: Setup time | | 17 | | 32 | ns |
| t _{CSDOD} | CS low level to DOUT drive | 10 | | 20 | | ns |
| t _{CSDOZ} | CS high level to DOUT Hi-Z | | 10 | | 20 | ns |



Note: SPI is set to CPOL = 0 and CPHA = 1.

Figure 1. Serial interface timing



Note: The timings shown are for the daisy chain of the eight-channel DADS1298.

Figure 2. Timing of the daisy chain port

DADS1294/DADS1296/DADS1298 Pin Configuration

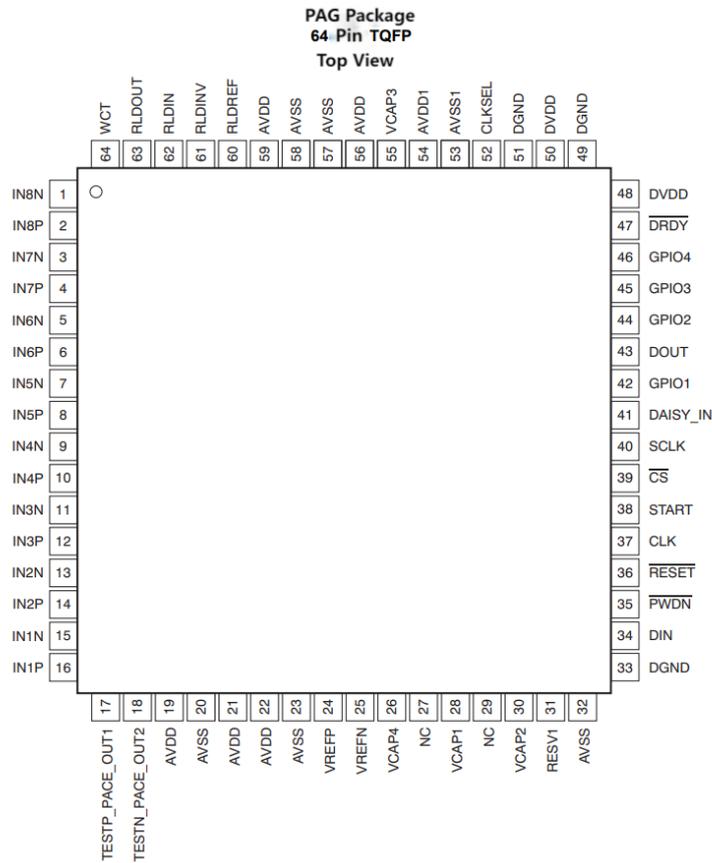


Table 1. DADS1294/DADS1296/DADS1298 Pin Definitions

| Pin | | Function | Description |
|-----|-----------------|----------------------------------|---|
| No. | Name | | |
| 1 | IN8N | Analog Input | Differential analog negative input 8 (DADS1298) |
| 2 | IN8P | Analog Input | Differential analog positive input 8 (DADS1298) |
| 3 | IN7N | Analog Input | Differential analog negative Input 7 (DADS1298) |
| 4 | IN7P | Analog Input | Differential analog positive input 7 (DADS1298) |
| 5 | IN6N | Analog Input | Differential analog negative Input 6 (DADS1296, DADS1298) |
| 6 | IN6P | Analog Input | Differential analog positive input 6 (DADS1296, DADS1298) |
| 7 | IN5N | Analog Input | Differential analog negative Input 5 (DADS1296, DADS1298) |
| 8 | IN5P | Analog Input | Differential analog positive input 5 (DADS1296, DADS1298) |
| 9 | IN4N | Analog Input | Differential analog negative Input 4 |
| 10 | IN4P | Analog Input | Differential analog positive Input 4 |
| 11 | IN3N | Analog Input | Differential analog negative Input 3 |
| 12 | IN3P | Analog Input | Differential analog positive Input 3 |
| 13 | IN2N | Analog Input | Differential analog negative Input 2 |
| 14 | IN2P | Analog Input | Differential analog negative Input 3 |
| 15 | IN1N | Analog Input | Differential analog negative Input 2 |
| 16 | IN1P | Analog Input | Differential analog negative Input 1 |
| 17 | TESTP_PACE_OUT1 | Analog Input/ Buffered Output | Internal test signal or single-ended buffered output (based on register settings) |
| 18 | TESTN_PACE_OUT2 | Analog Input/Output | Internal test signal or single-ended buffered output (based on register settings) |

Table 1. DADS1294/DADS1296/DADS1298 Pin Definitions (Continued)

| Pin | | Function | Description |
|-----|---------------------------|----------------------|--|
| No. | Name | | |
| 19 | AVDD | Power supply | Analog power supply |
| 20 | AVSS | Power supply | Analog ground |
| 21 | AVDD | Power supply | Analog power supply |
| 22 | AVDD | Power supply | Analog power supply |
| 23 | AVSS | Power supply | Analog ground |
| 24 | VREFP | Analog Input/Output | Positive reference input/output voltage |
| 25 | VREFN | Analog Input | Negative reference voltage |
| 26 | VCAP4 | — | Analog bypass capacitor; connect a 1 μ F capacitor to the AVSS. |
| 27 | NC | — | No connection is required; a 10k Ω resistor can be used to connect to AVDD or AVSS. |
| 28 | VCAP1 | — | Analog bypass capacitor; connect a 22 μ F capacitor to the AVSS. |
| 29 | NC | — | No connection is required; a 10k Ω resistor can be used to connect to AVDD or AVSS. |
| 30 | VCAP2 | — | Analog bypass capacitor; connect a 1 μ F capacitor to the AVSS. |
| 31 | RESV1 | Digital input | Reserved for future use; must be connected to logic low (DGND). |
| 32 | AVSS | Power supply | Analog ground |
| 33 | DGND | Power supply | Digital ground |
| 34 | DIN | Digital input | SPI data input |
| 35 | $\overline{\text{PWDN}}$ | Digital input | Shutdown pin; active low |
| 36 | $\overline{\text{RESET}}$ | Digital input | System reset pin; active low |
| 37 | CLK | Digital Input/Output | External master clock input or internal clock output |
| 38 | $\overline{\text{START}}$ | Digital input | Start conversion |
| 39 | $\overline{\text{CS}}$ | Digital input | SPI chip select; active low |
| 40 | SCLK | Digital input | SPI clock |
| 41 | DAISY_IN | Digital input | Daisy chain input; if not used, short to DGND. |
| 42 | GPIO1 | Digital Input/Output | General Purpose Input/Output Pin 1 |
| 43 | DOUT | Digital output | SPI data output |
| 44 | GPIO2 | Digital Input/Output | General Purpose Input/Output Pin 2 |
| 45 | GPIO3 | Digital Input/Output | General purpose input/output pin 3 |
| 46 | GPIO4 | Digital Input/Output | General purpose input/output pin 4 |
| 47 | $\overline{\text{DRDY}}$ | Digital output | Data ready; active low |
| 48 | DVDD | power supply | Digital power supply |
| 49 | DGND | power supply | Digital ground |
| 50 | DVDD | power supply | Digital power supply |
| 51 | DGND | power supply | Digital ground |

Table 1. DADS1294/DADS1296/DADS1298 Pin Definitions (Continued)

| Pin | | Function | Description |
|-----|--------|---------------------|---|
| No. | Name | | |
| 52 | CLKSEL | Digital input | Master clock selection |
| 53 | AVSS1 | Power supply | Analog ground |
| 54 | AVDD1 | Power supply | Analog power supply |
| 55 | VCAP3 | — | Analog bypass capacitor; internally generated AVDD + 1.9V; connect a 1 μ F capacitor to AVSS. |
| 56 | AVDD | Power supply | Analog power supply |
| 57 | AVSS | Power supply | Analog ground |
| 58 | AVSS | Power supply | Analog ground |
| 59 | AVDD | Power supply | Analog power supply |
| 60 | RLDREF | Analog Input | Right leg drive in-phase input |
| 61 | RLDINV | Analog Input/Output | Right leg drive input inverted input |
| 62 | RLDIN | Analog Input | Right leg drive input of the multiplexer |
| 63 | RLDOUT | Analog output | Right leg drive output |
| 64 | WCT | Analog output | Wilson center terminal output |

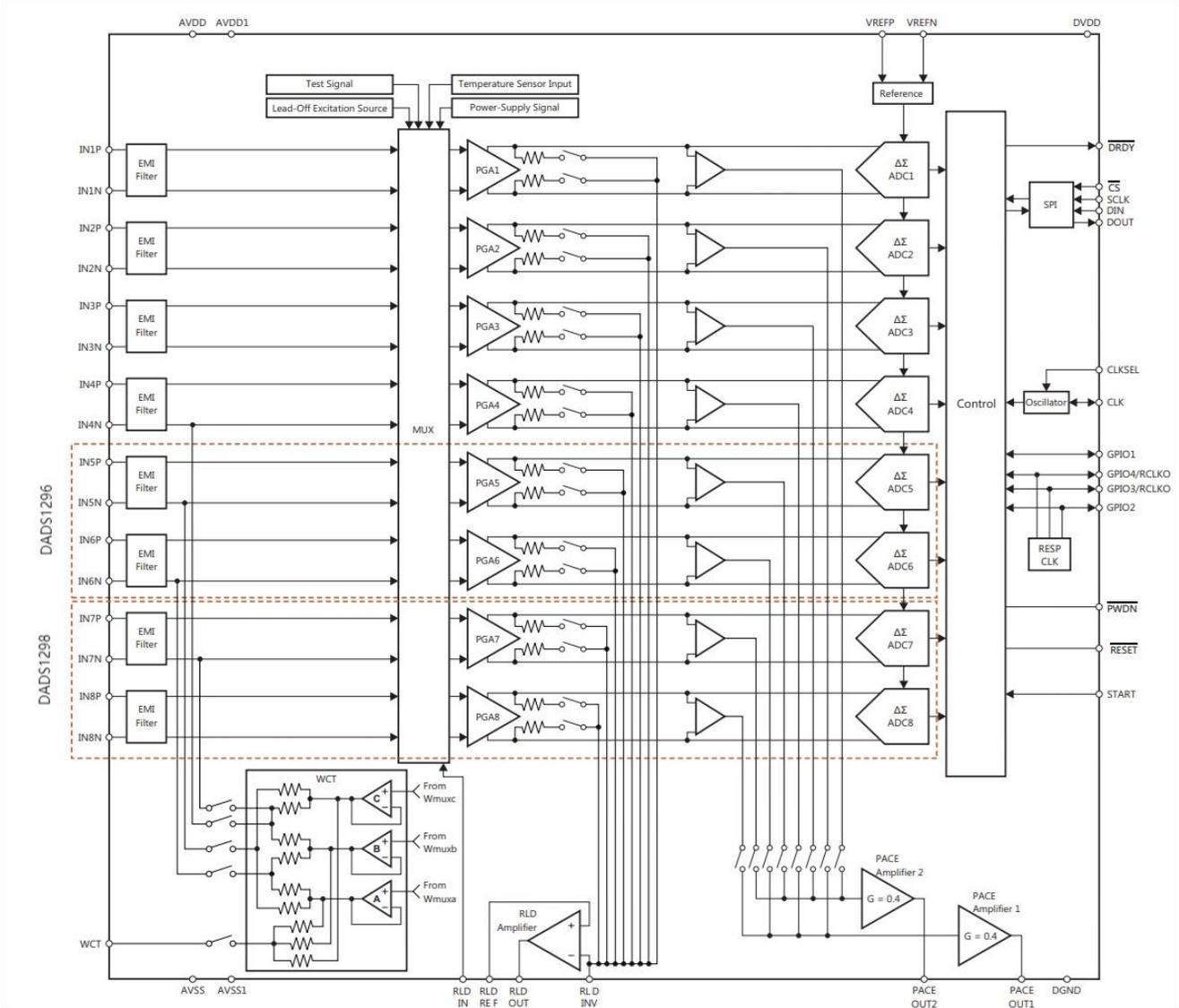
Summary

The DADS129x are low-power, multi-channel, simultaneous sampling, 24-bit Δ - Σ analog-to-digital converters (ADCs) with an integrated programmable gain amplifier (PGA). These devices include a variety of ECG-specific features, making them ideal for scalable electrocardiogram (ECG), electroencephalogram (EEG), and electromyography (EMG) applications.

By disabling the dedicated ECG circuitry, these devices can also be used in high-performance, multi-channel data acquisition systems. The DADS129x features a highly programmable multiplexer (mux) for temperature, power, input shorting, and RLD measurements. Furthermore, the multiplexer allows any input electrode to be programmed as a patient reference driver. PGA gain can be selected from seven settings: 1, 2, 3, 4, 6, 8, or 12. The on-device ADC provides data rates from 250 SPS to 32 kSPS. Communication with the device is via an SPI-compatible interface. The device provides four general-purpose GPIO pins. Multiple devices can be synchronized using the START pin.

The internal reference is programmed to 2.4V or 4V. An internal oscillator generates a 2.048MHz clock. The multi-functional right leg drive (RLD) module allows selection of the average value of any electrode combination to generate the patient drive signal. Lead dislodgement detection can be performed using pull-up or pull-down resistors, current sources, or current traps. Internal AC lead dislodgement detection is also provided. These devices support both hardware and software pacing signal detection. The Wilson center terminal (WCT) block can be used to generate the WCT point for a standard 12-lead ECG.

Functional Block Diagram



Analog Function

EMI filters

The input RC filter serves as the EMI filter for all channels. The -3dB filter bandwidth is approximately 3MHz.

Analog input structure

Figure 24 shows the analog input of the DADS129x.

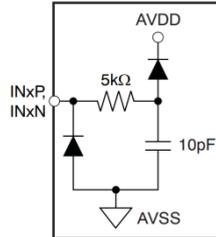
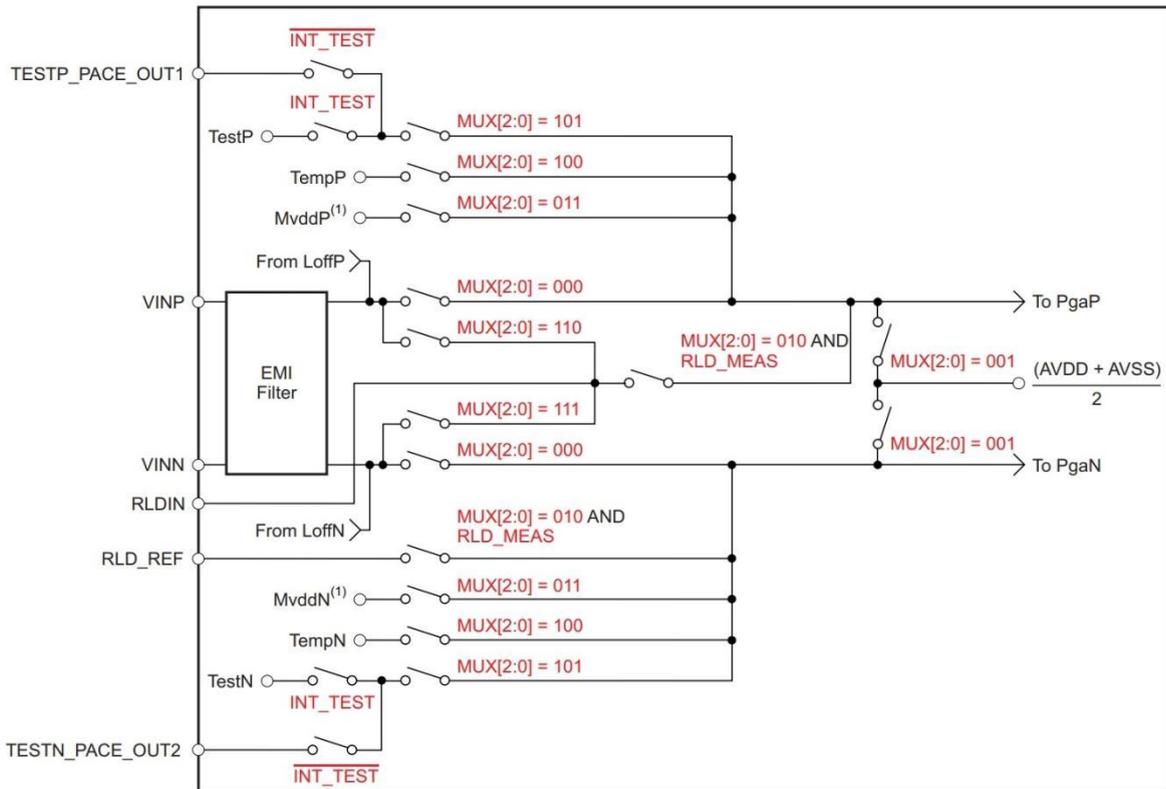


Figure 24. Analog Input Protection Circuit

Input multiplexer

The DADS129x input multiplexer is highly flexible, offering a wide range of configurable signal switching options. Figure 25 shows the multiplexer on a single channel of the device. The device has eight blocks, one for each channel. TEST_PACE_OUT1, TEST_PACE_OUT2, and RLD_IN are shared by all eight blocks. VINP and VINN are independent for each of these eight blocks. This flexibility allows for critical device and subsystem diagnostics, calibration, and configuration. Switch settings for each channel can be selected by writing 1 to the corresponding values in the CHnSET[2:0] registers (see CHnSET Registers for details) and the RLD_MEAS bit in the CONFIG3 register (see CONFIG3 Registers for details). For information on the multiplexer's ECG-specific functions, see the Input Multiplexer (Rerouting Right Leg Drive Signal) section in the ECG-Specific Functions section.



(1) The voltage supply of the MVDD monitor depends on the number of channels; please refer to the power measurement (MVDDP, MVDDN) section.

Figure 25. Input multiplexer block for one channel

Device noise measurement

Setting CHnSET[2:0] = 001 sets the common-mode voltage (AVDD - AVSS)/2 for the two inputs of this channel. This setting can be used to test the inherent noise of the device.

Test signals (TestP and TestN)

Setting CHnSET[2:0] = 101 provides internally generated test signals for subsystem verification at power-up. This function can be used to test the entire signal chain. Although the test signals are similar to the CAL signals described in the IEC 60601-2-51 specification, this function is not suitable for compliance testing. The test signals can be controlled using register settings (see CONFIG2: Configuration Register 2 (Address = 02h) (Reset = 40h) section for details). The TEST_AMP bit controls the signal amplitude, and the TEST_FREQ bit controls the switching at the desired frequency. The test signals are multiplexed on the TESTP_PACE_OUT1 and TESTN_PACE_OUT2 pins and transmitted outward from the device. The bit register (CONFIG2.INT_TEST = 0) disables the internal test signals so that test signals can be driven externally. This function allows multiple devices to be calibrated using the same signal. The test signal function cannot be used in conjunction with external hardware pacing functions (see External Hardware Approaches for details).

Auxiliary differential inputs (TESTP_PACE_OUT1, TESTN_PACE_OUT2)

When hardware pacing signal detection is not used, the TESTP_PACE_OUT1 and TESTN_PACE_OUT2 signals can be used as multiplexed differential input channels. These inputs can be multiplexed to any of the eight channels. The differential input signals fed through these pins have the same performance as the normal channels.

Temperature sensors (TempP, TempN)

The DADS129x includes an on-chip temperature sensor. This sensor uses two internal diodes, one of which has a current density 16 times that of the other, as shown in Figure 26. This difference in diode current density produces a voltage difference proportional to the absolute temperature.

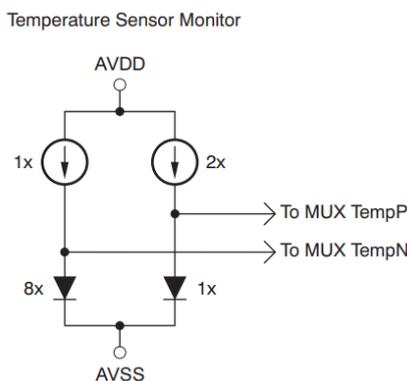


Figure 26. Temperature sensor measurement at the input end

Due to its low thermal resistance when packaged onto a printed circuit board (PCB), the internal sensor closely tracks the PCB temperature. The self-heating of the DADS129x can cause readings to be higher than the temperature of the surrounding PCB.

The scaling factor in Equation 1 converts the temperature reading to °C. The temperature reading code should be converted to μV before using this Equation.

$$\text{Temperature (}^{\circ}\text{C)} = \left[\frac{\text{Temperature Reading (}\mu\text{V)} - 145,300 \mu\text{V}}{490 \mu\text{V}/^{\circ}\text{C}} \right] + 25^{\circ}\text{C} \quad (1)$$

Power supply measurement (MVDDP, MVDDN)

Setting CHnSET[2:0] = 011 allows you to configure the channel inputs for different power supply voltages of the device.

For channels 1, 2, 5, 6, 7, and 8, (MVDDP - MVDDN) = [0.5 × (AVDD - AVSS)].

For channels 3 and 4, (MVDDP - MVDDN) = DVDD/4.

To avoid saturating the PGA when measuring the power supply, set the gain to 1.

For example, if AVDD = 2.5V and AVSS = -2.5V, the measurement result will be 2.5V.

Lead detachment excitation signals (LoffP, LoffN)

The lead-drop excitation signal is fed to the multiplexer before the switch. A comparator for detecting lead-drop conditions is also connected to the multiplexer block before the switch. For detailed information on the lead-drop block, see below.

Please refer to the lead detachment detection section.

Auxiliary single-ended input

The RLD_IN pin is primarily used to route the Right Foot Drive (RLD) signal to any electrode in case the RLD electrode falls off. However, the RLD_IN pin can be used as multiple single-ended input channels. The signal on the RLD_IN pin can be measured using any of the eight channels relative to the voltage on the RLD_REF pin.

This measurement can be performed by setting the channel multiplexer to 010 and setting the RLD_MEAS bit in the CONFIG3 register to 1.

Analog Input

The analog inputs of the DADS129x are fully differential. Assuming $PGA = 1$, the differential input ($INP - INN$) can span from $-V_{REF}$ to V_{REF} . The absolute ranges of INP and INN must be between $AVSS - 0.3V$ and $AVDD + 0.3V$. See Table 13 for an explanation of the correlation between analog inputs and digital codes. As shown in Figures 27 and 28, the analog inputs of the DADS129x can be driven in two general ways: single-ended and differential. In the differential input method, INP and INN have a 180° phase difference. When the input is single-ended, the INN input remains at the common-mode voltage (CM), preferably at the midpoint. The INP input swings around the same common-mode voltage, with the peak-to-peak amplitude swinging from $CM - V_{REF}$ to $CM + V_{REF}$. When the input is differential, the common-mode voltage is given by $(INP + INN)/2$. Both the INP and INN inputs swing from $CM + \frac{1}{2} V_{REF}$ to $CM - \frac{1}{2} V_{REF}$. For optimal performance, the DADS129x device should be used in a differential configuration.

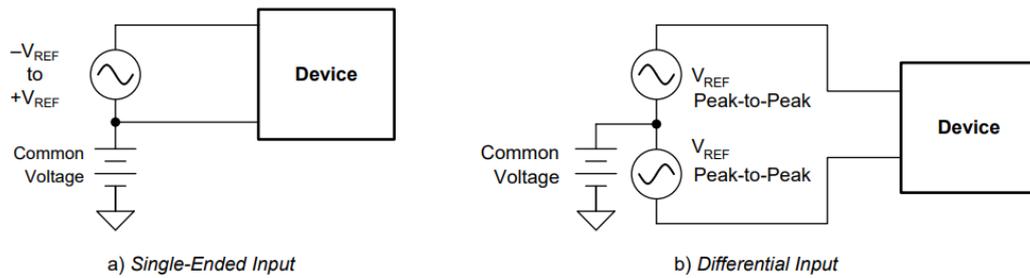
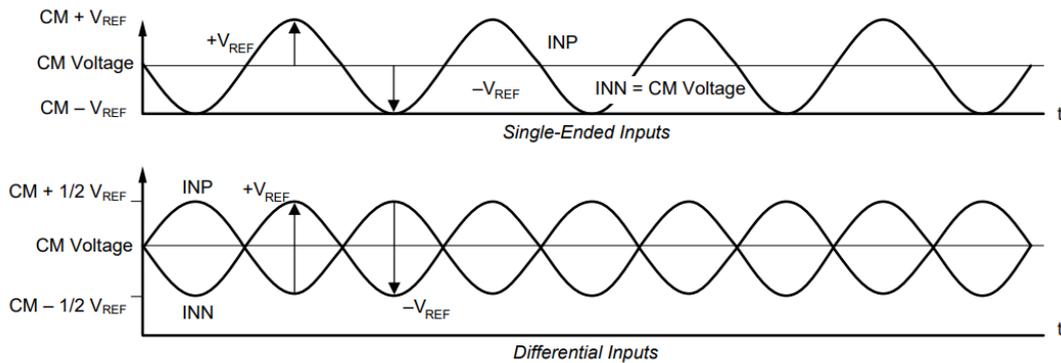


Figure 27. Methods for driving DADS129x: single-ended or differential



$$\text{Common-Mode Voltage (Differential Mode)} = \frac{(INP) + (INN)}{2}, \text{ Common-Mode Voltage (Single-Ended Mode)} = INN$$

$$\text{Input Range (Differential Mode)} = (AINP - AINN) = 2 V_{REF}$$

Figure 28. Using DADS129x in single-ended and differential input modes

PGA settings and input range

The PGA is a differential input and differential output amplifier, as shown in Figure 29. The PGA has seven gain settings (1, 2, 3, 4, 6, 8, and 12), which can be implemented by writing to the CHnSET register (see the CHnSET: Individual Channel Settings (n = 1 to 8) (Addresses = 05h to 0Ch) (Reset = 00h) section). The DADS129x has CMOS inputs, therefore exhibiting negligible current noise. Table 5 shows typical bandwidth values for the various gain settings. Table 5 also shows the small-signal bandwidth.

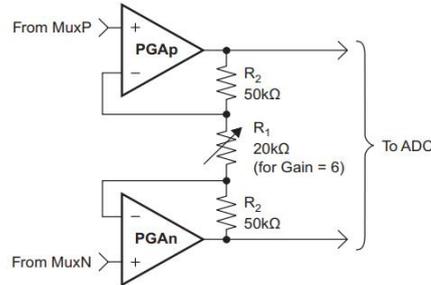


Figure 29. PGA Implementation

Table 5. Relationship between PGA gain and small-signal bandwidth

| Gain | Nominal bandwidth (kHz) at room temperature |
|------|---|
| 1 | 237 |
| 2 | 146 |
| 3 | 127 |
| 4 | 96 |
| 6 | 64 |
| 8 | 48 |
| 12 | 32 |

For a gain of 6, the resistor string of the PGA that implements the gain has a resistance of 120kΩ. This resistor provides a current path across the PGA output in the presence of a differential input signal. This current complements the quiescent current specified for the device when a differential signal is present at the input.

Common mode input range

The available input common-mode range of the front end depends on various parameters, including the maximum differential input signal, supply voltage, PGA gain, etc. Equation 2 illustrates this range:

$$AVDD - 0.2 \text{ V} - \left(\frac{\text{Gain} \times V_{\text{MAX_DIFF}}}{2} \right) > \text{CM} > AVSS + 0.2 \text{ V} + \left(\frac{\text{Gain} \times V_{\text{MAX_DIFF}}}{2} \right)$$

where

- $V_{\text{MAX_DIFF}}$ = maximum differential signal at the input of the PGA
- CM = common-mode range

(2)

For example, if $VDD = 3\text{V}$, gain = 6, and $V_{\text{MAX_DIFF}} = 350\text{mV}$, then $1.25\text{V} < \text{CM} < 1.75\text{V}$.

Input differential dynamic range

differential (INP – INN) signal depends on the analog power supply and reference used in the system. Equation 3 shows this range.

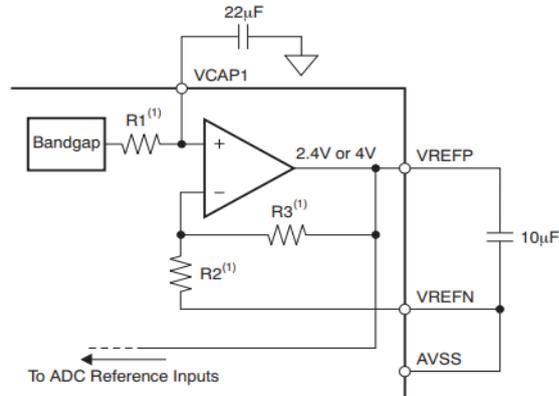
$$\text{Full-Scale Range} = \frac{\pm V_{\text{REF}}}{\text{Gain}} = \frac{2V_{\text{REF}}}{\text{Gain}}$$

(3)

The 3V supply (reference voltage 2.4V, ECG gain 6) is optimized for power, with a differential input signal of approximately 300mV. For higher dynamic range, use a 5V supply and a 4V reference voltage (set by the VREF_4V bit in the CONFIG3 register) to increase the differential dynamic range.

Reference

Figure 31 shows a simplified block diagram of the DADS129x internal reference. This reference voltage is generated relative to the AVSS. When using the internal voltage reference, VREFN needs to be connected to the AVSS.



(1) For VREF = 2.4V: R1 = 12.5kΩ, R2 = 25kΩ, R3 = 25kΩ. For VREF = 4V: R1 = 10.5kΩ, R2 = 15kΩ, R3 = 35kΩ.

Figure 31. Internal reference

The external bandwidth limiting capacitor determines the contribution of the reference noise. For high-end ECG systems, select a capacitor value with a bandwidth limit below 10Hz to prevent reference noise from becoming a major source of system noise. When using a 3V analog power supply, the internal reference should be set to 2.4V. For a 5V analog power supply, the internal reference should be set to 4V by setting the VREF_4V position in the CONFIG2 register.

Alternatively, the power supply to the internal reference buffer can be turned off, and an external VREFP can be applied. Figure 32 shows a typical external reference drive circuit. Power is turned off by the CONFIG3 register. The PD_REFBUF bit controls this. By default, the device wakes up in external reference mode.

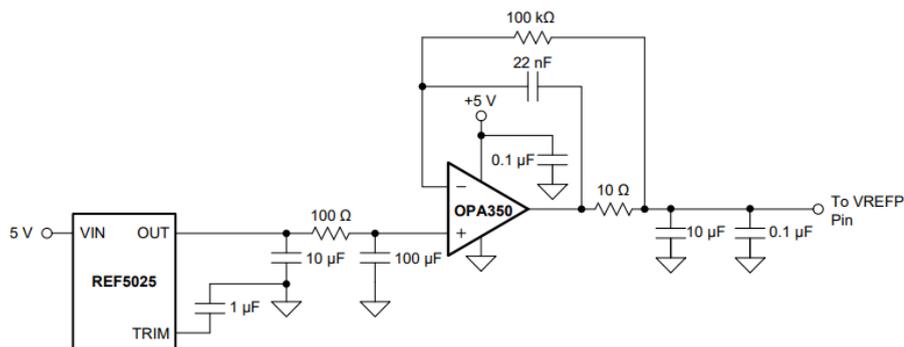


Figure 32. External reference driver

Wilson central terminal (WCT) and chest leads

In a standard 12-lead ECG, the WCT voltage is defined as the average of the right arm (RA), left arm (LA), and left leg (LL) electrodes. This voltage is used as a reference voltage for chest lead measurements. The DADS129x features three integrated low-noise amplifiers that generate the WCT voltage. Figure 35 shows a block diagram of the implementation.

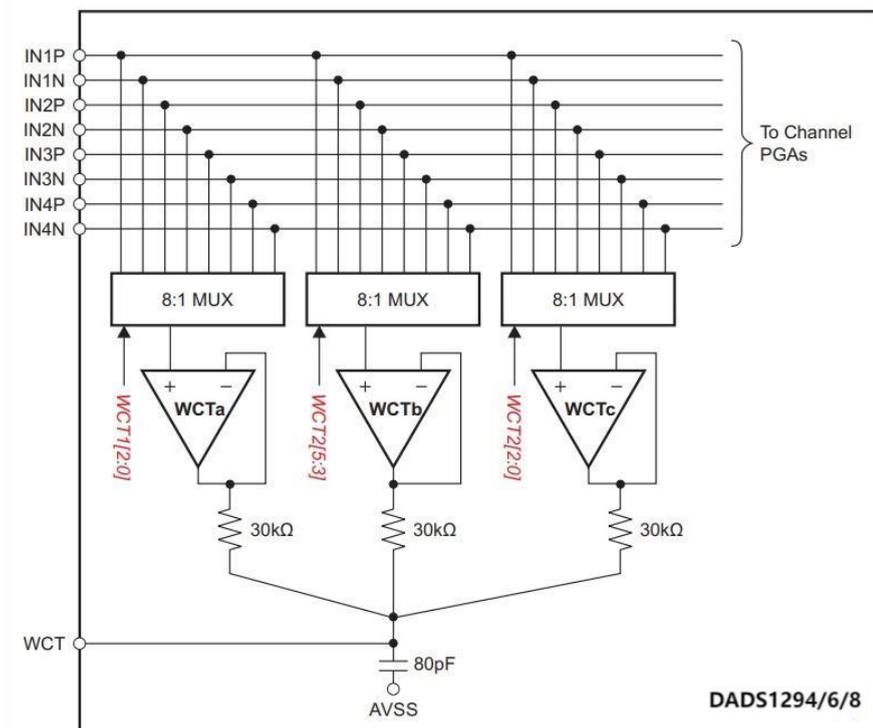


Figure 35. WCT voltage

These devices allow for the flexible routing of any one of the eight signals (IN1P to IN4N) to each amplifier to generate an average value. This flexibility allows the RA, LA, and LL electrodes to be connected to any input of the first four channels, depending on the lead configuration.

Each of the three amplifiers in the WCT circuit can be individually powered down via register settings. By powering on two amplifiers, an average value can be generated at any two electrodes on the WCT pin. Powering on one amplifier provides a buffered electrode voltage on the WCT pin. The WCT amplifiers have limited drive strength, therefore, they should be buffered if they are used to drive low-impedance loads.

Table 6 shows typical WCT performance when using any 1, 2, or 3 WCT buffers.

Table 6. Typical WCT Performance

| Parameter | Any one (A, B, or C) | Any two (A+B, A+C, or B+C) | All three (A+B+C) | Unit |
|----------------|-------------------------|-------------------------------|----------------------|-------------------|
| Integral noise | 540 | 382 | 312 | nV _{RMS} |
| power | 53 | 59 | 65 | μW |
| -3dB BW | 30 | 59 | 89 | kHz |
| Slewing rate | BW restrictions | BW restrictions | BW restrictions | V/μs |

As shown in Table 6, the overall noise decreases when multiple WCT amplifiers are powered on. This noise reduction occurs because the noise is averaged by the passive summing network at the amplifier outputs.

The power savings from shutting down the individual buffers are negligible, as a large portion of the circuitry is shared among the three amplifiers. The bandwidth of the WCT node is limited by the RC network. The internal summing network consists of three 30kΩ resistors and one 80pF capacitor. For optimal performance, add an external 100pF capacitor. The effective bandwidth depends on the number of amplifiers powered on, as shown in Table 6.

Use only the WCT node to drive very high input impedances (typically greater than 500MΩ). A typical application connects this WCT signal to the negative input of the DADS129x as a reference signal for the chest leads.

DADS1294/1296/1298 Low-Power, 4/6/8-Channel, Low-Noise, 24-Bit ADC for Physiological Signal Measurement

As previously mentioned, all three WCT amplifiers can be connected to one of the eight analog input pins. The amplifier inputs are chopped, with the chopping frequency varying depending on the DADS129x's data rate. The chopping frequencies for the three highest data rates are in a 1:1 ratio. For example, at a 32kSPS data rate, the chopping frequency in HR mode is 32kHz (WCT_CHOP = 0). The chopping frequencies for the four lower data rates are fixed at 4kHz. When WCT_CHOP = 1, the chopping frequency is fixed at the highest data rate frequency (i.e., $f_{MOD}/16$), as shown in Table 7. The chopping frequency appears as a small square wave over DC at the output of the WCT amplifier. The amplitude of the square wave is the amplifier offset, typically 5mV_{PP}.

Due to out-of-band chopping, this artifact does not interfere with ECG-related measurements. Due to the chopping function, input current leakage on the pins of the connected WCT amplifier increases at higher data rates and when the input common voltage swings close to 0V (AVSS), as shown in Figure 36.

If the output of a channel connected to the WCT amplifier (e.g., the V lead channel) is connected to one of the pacing signal amplifiers used for external pacing signal detection, a chopping artifact will appear at the output of the pacing signal amplifier.

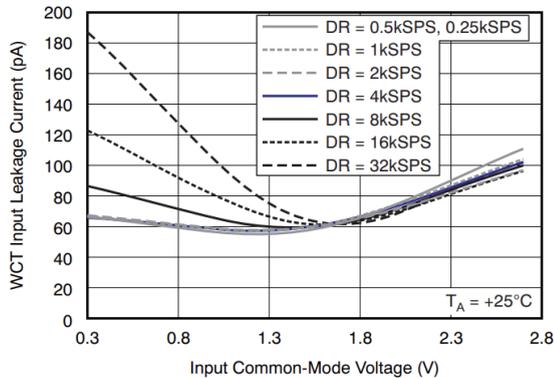


Figure 36. WCT Input Leakage Current vs Input Voltage (WCT_CHOP = 0)

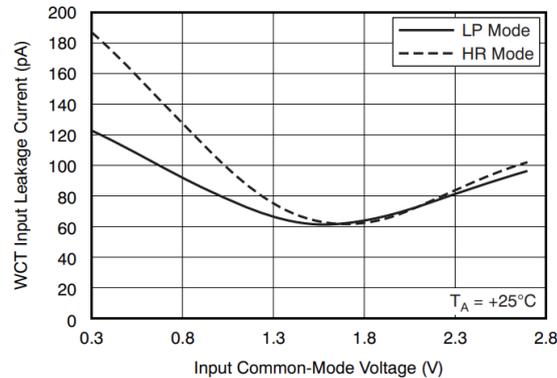


Figure 37. WCT Input Leakage Current vs Input Voltage (WCT_CHOP = 1)

Table 7. WCT Amplifier Chop Frequency

| CONFIG1.DR[2:0] bits | CONFIG2.WCT_CHOP = 0 | CONFIG2.WCT_CHOP = 1 |
|----------------------|----------------------|----------------------|
| 000 | $f_{MOD}/16$ | $f_{MOD}/16$ |
| 001 | $f_{MOD}/32$ | $f_{MOD}/16$ |
| 010 | $f_{MOD}/64$ | $f_{MOD}/16$ |
| 011 | $f_{MOD}/128$ | $f_{MOD}/16$ |
| 100 | $f_{MOD}/128$ | $f_{MOD}/16$ |
| 101 | $f_{MOD}/128$ | $f_{MOD}/16$ |
| 110 | $f_{MOD}/128$ | $f_{MOD}/16$ |

Augmented Leads

In a typical implementation of a 12-lead ECG with eight channels, the enhanced leads are calculated digitally. In some applications, it may be necessary for all leads to be derived analog (rather than digital).

The DADS1298 provides the option to generate enhanced leads by routing the corresponding average values to channels 5, 6, and 7. The same three amplifiers used to generate the WCT signal are also used to generate the Goldberg center terminal (GCT) signal.

Figure 38 shows an example of generating enhanced leads in the analog domain. In this implementation, more than eight channels are used to generate the standard 12 leads.

Note: This functionality is not provided in the DADS1294 and DADS1296.

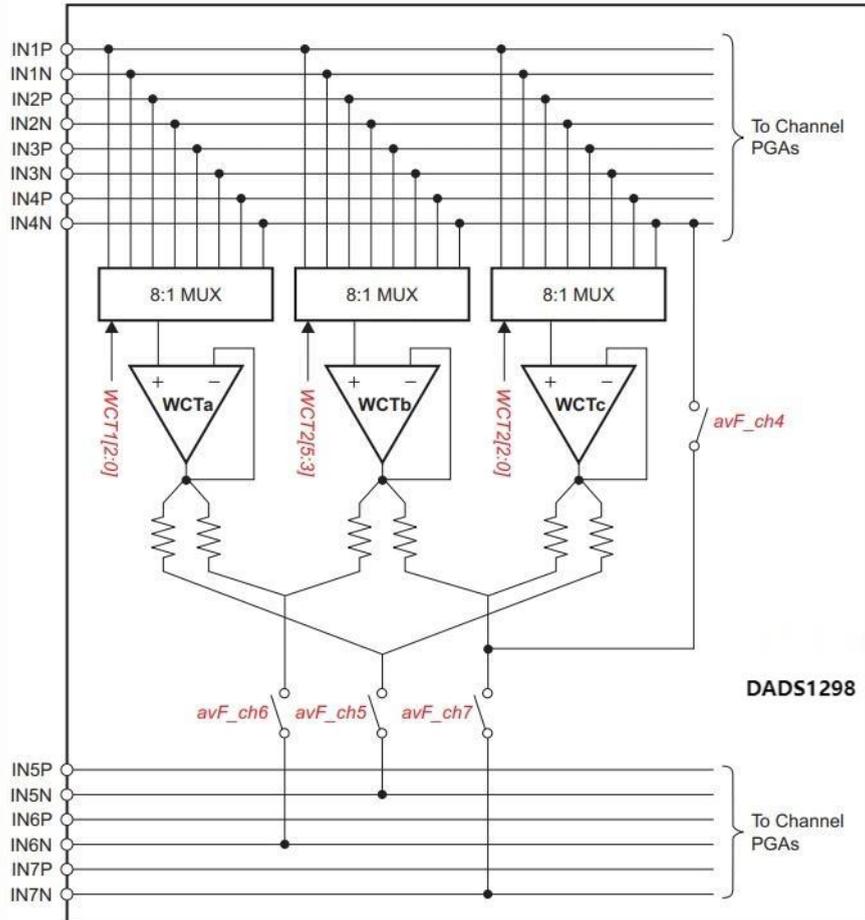


Figure 38. Analog or Augmented leads

Right leg drive with WCT point

In some applications, an out-of-phase version of WCT is used as the RLD reference. The DADS1298 provides the option to implement a buffered version of the WCT terminal on the RLD_OUT pin. This signal can be used externally.

The amplifier is inverted and then used as the right leg drive. See the Right Leg Drive (RLD) DC Bias Current section for more details.

Lead-Off Detection

Patient electrode impedance decays over time; therefore, these electrode connections must be continuously monitored to verify the presence of a suitable connection. The DADS129x lead-off detection function block provides great flexibility in selecting from various lead detachment detection strategies. Although the function is called lead detachment detection, it is actually electrode off detection. The basic principle is to inject an excitation signal and measure the response to determine whether the electrode has detached.

As shown in the lead-off detection function block diagram in Figure 39, this circuit provides two different methods for determining the patient electrode status. These methods have different excitation signal frequency components. Lead-off can be selectively performed on a per-channel basis using the LOFF_SENSP and LOFF_SENSN registers. The internal excitation circuit can be disabled when the detection circuit is enabled.

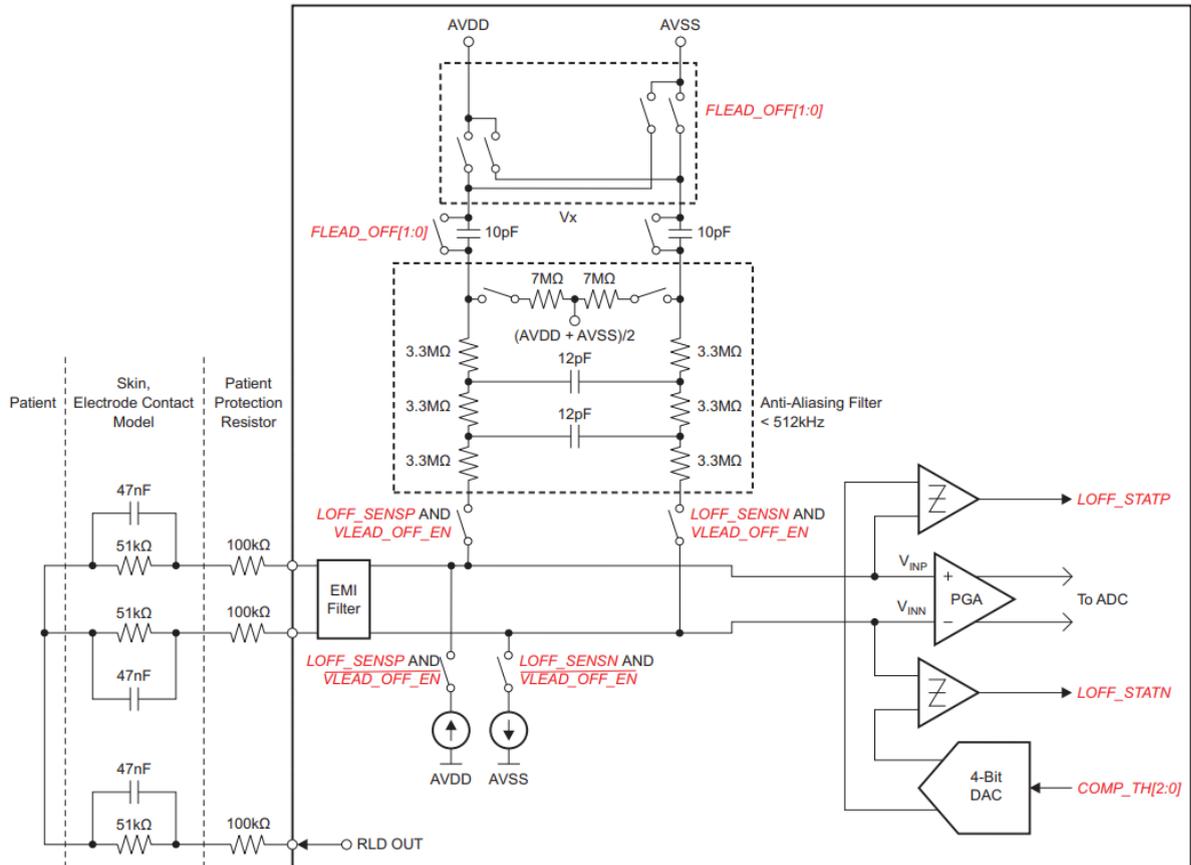
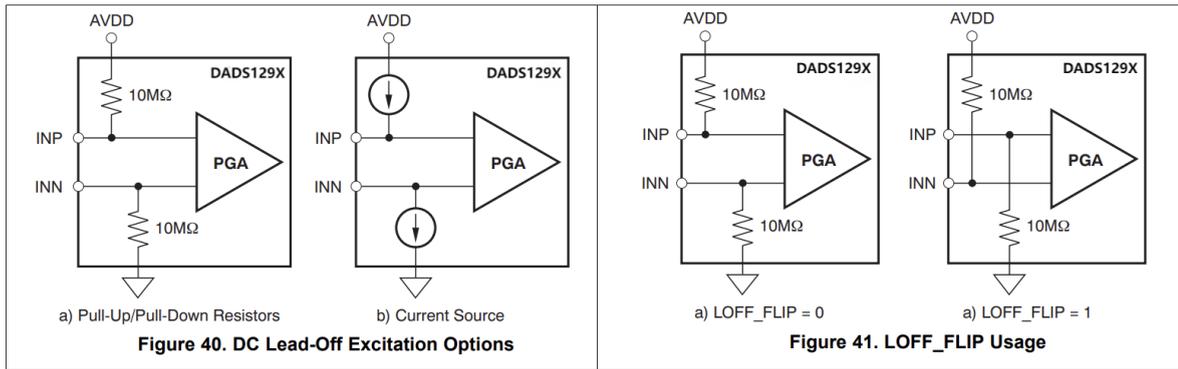


Figure 39. Lead-off detection

DC Lead-Off

In this approach, the lead-off excitation is accomplished with a dc signal. Choose a DC excitation signal from either a pullup or pulldown resistor, or from a current source or sink system, as shown in Figure 40. Select by setting the VLEAD OFF EN bit in the LOFF register. One side of the channel is pulled to supply, and the other side is pulled to ground. Swap the pullup resistor and pulldown resistor by setting the bits in the LOFF_FLIP register, as shown in Figure 41. If using a current source or sink, set the magnitude of the current by using the ILEAD OFF[1:0] bits in the LOFF register. The current source or sink gives larger input impedance compared to the 10-M Ω pullup or pulldown resistor.



Response sensing is achieved either by looking at the digital output code from the device, or by monitoring the input voltages with on-chip comparators. If either of the electrodes is off, the pullup or pulldown resistors saturate the channel. Look at the output code to determine if either the P-side or the N-side is off. To pinpoint which side is off, check the comparator outputs. During conversion, the input voltage is simultaneously monitored by using a comparator and a 4-bit DAC with levels that are set by the COMP_TH[2:0] bits in the LOFF register. The comparator outputs are stored in the LOFF_STATP and LOFF_STATN registers. These two registers are available as a part of the output data stream (see the Data Output Pin (DOUT) section). If dc lead-off is not used, the lead-off comparators can be powered down by setting the PD_LOFF_COMP bit in the CONFIG4 register.

An example procedure to turn on dc lead-off is given in the Lead-Off section.

AC Lead-Off

This method uses an out-of-band ac signal for excitation. The ac signal is generated by providing pullup and pulldown resistors at the input with a fixed frequency. The ac signal is passed through an antialiasing filter to prevent aliasing. Select the frequency with the FLEAD_OFF[1:0] bits in the LOFF register. The excitation frequency is a function of the output data rate and is $f_{DR} / 4$. This out-of-band excitation signal is passed through the channel and measured at the output.

AC signal sensing is achieved by passing the signal through the channel to digitize the signal, and measuring the output. The ac excitation signals are introduced at a frequency that is above the band of interest, generating an out-of-band differential signal that can be filtered out separately and processed. By measuring the magnitude of the excitation signal at the output spectrum, the lead-off status is calculated. Therefore, the ac lead-off detection is accomplished simultaneously with the ECG signal acquisition.

RLD Lead-Off

Determine if the RLD electrode is connected in the DADS129x by powering down the RLD amplifier. After power down, there are two measurement procedures to determine the RLD electrode connect status: a pullup or pulldown resistor, or a sink or source current source, as shown in Figure 42. Set the reference level of the comparator to determine the acceptable RLD impedance threshold.

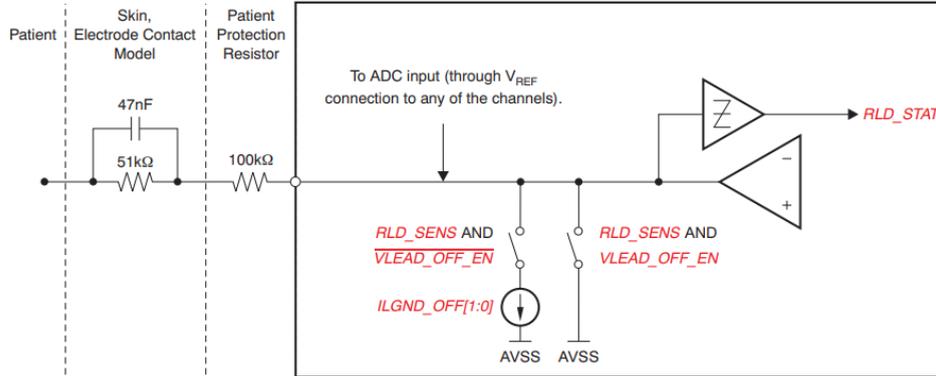


Figure 42. RLD Lead-Off Detection at Power Up

The current source, or pullup or pulldown resistor method has no function when the RLD amplifier is powered on. Use the comparator to sense the voltage at the output of the RLD amplifier. The comparator threshold is set by the same LOFF[7:5] bits that are used to set the thresholds for the other negative inputs.

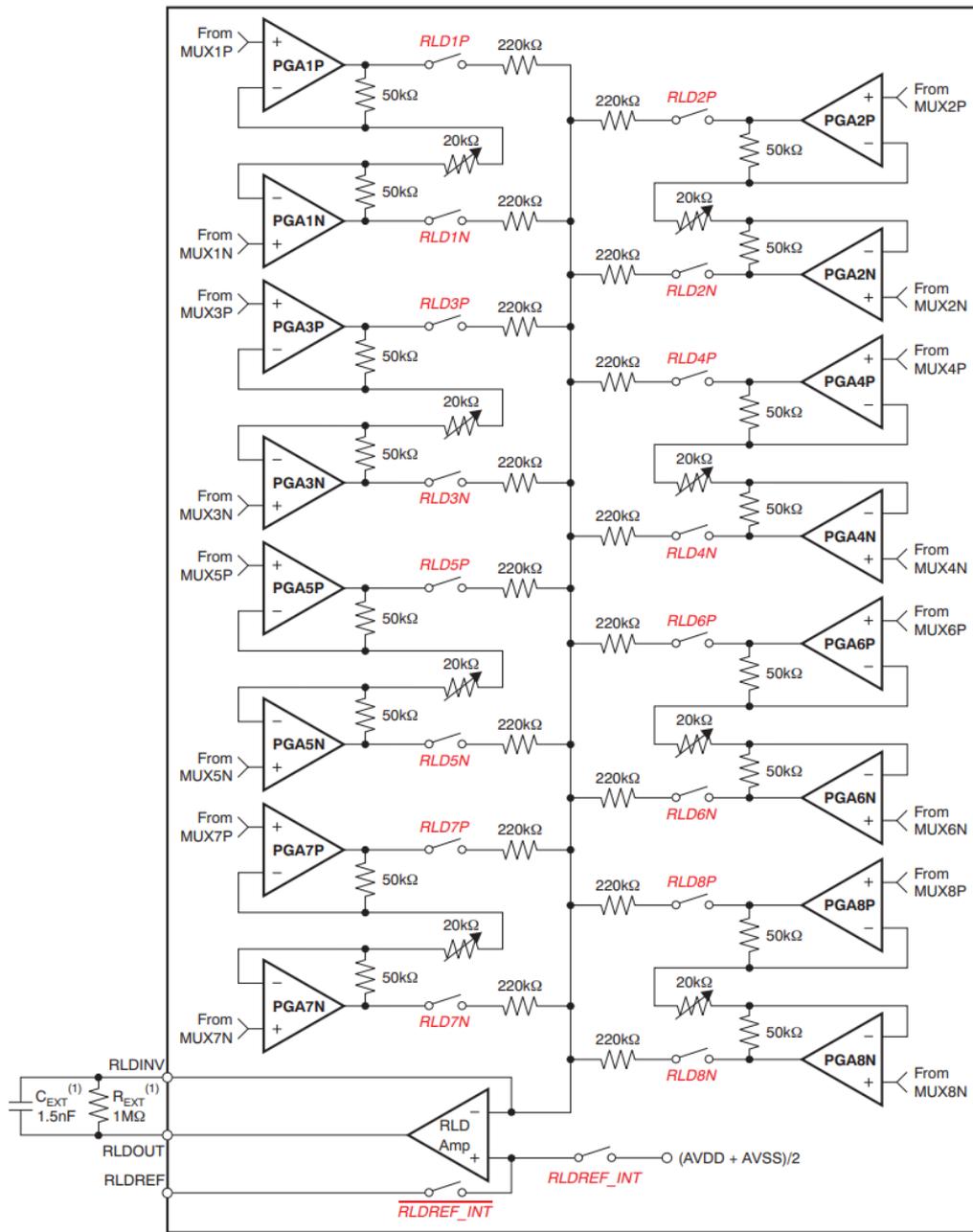
Right Leg Drive (RLD) DC Bias Current

Use the right leg drive (RLD) circuitry to counter the common-mode interference in a ECG system as a result of power lines and other sources, including fluorescent lights. The RLD circuit senses the common-mode voltage of a selected set of electrodes and creates a negative feedback loop by driving the body with an inverted commonmode signal. The negative feedback loop restricts the common-mode movement to a narrow range, depending on the loop gain. Stabilizing the entire loop is specific to the individual system, based on the various poles in the loop. The DADS129x incorporate muxes that are used to select the channel to the operational amplifier. All the amplifier terminals are available at the pins, allowing selection of the components for the feedback loop. The circuit shown in Figure 43 shows the overall functional connectivity for the RLD bias circuit.

Set the reference voltage for the RLD to be generated internally ($(AVDD + AVSS) / 2$), or provided externally with a resistive divider. The selection of an internal versus external reference voltage for the RLD loop is defined by writing the appropriate value to the RLDREF_INT bit in the CONFIG3 register.

If the RLD function is not used, power down the amplifier using the PD_RLD bit (see the CONFIG3: Configuration Register 3 (address = 03h) (reset = 40h) section for details). This bit is also used in daisy-chain mode to power down all but one of the RLD amplifiers.

The functionality of the RLDIN pin is explained in the Input Multiplexer section. An example procedure to use the RLD amplifier is shown in the Right Leg Drive section of the Power-Supply Recommendations



(1) Typical value.

(2) When the CONFIG3 bit RLDREF_INT = 0, the RLDREF_INT switch is closed and the RLDREF_INT switch is open. When the CONFIG3 bit RLDREF_INT = 1, the RLDREF_INT switch is open and the RLDREF_INT switch is closed.

Figure 43. RLD Channel Selection ⁽²⁾

WCT used as RLD

In certain applications, the RLD is derived as the average of RA, LA, and LL. This level is the same as the WCT voltage. The WCT amplifier has limited drive strength; therefore, only use the WCT to drive very high impedances directly. The ADS129x provide an option to internally buffer the WCT signal by setting the WCT_TO_RLD bit in the CONFIG4 register. Short the RLD_OUT and RLD_INV pins external to the device. Before the RLD_OUT signal is connected to the RLD electrode, use an external amplifier to invert the phase of the signal for negative feedback.

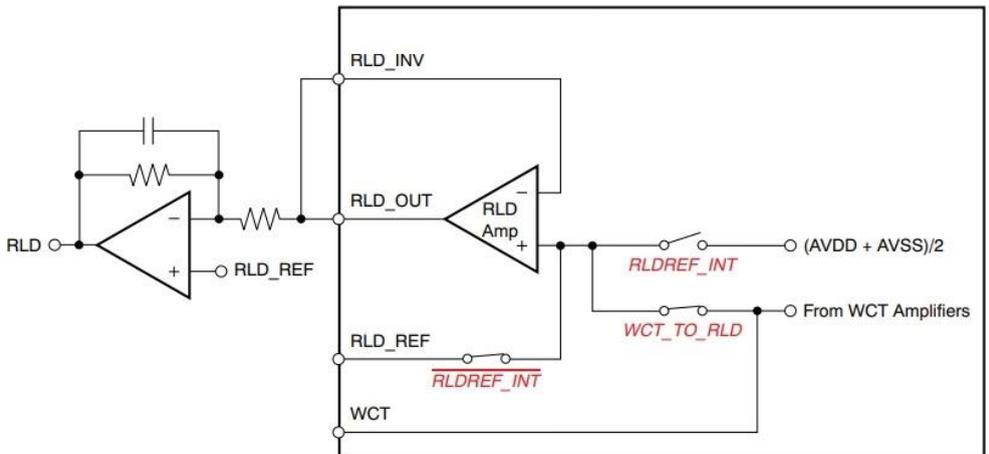


Figure 44. Using WCT as right leg drive (RLD)

RLD configuration using multiple devices

Figure 45 shows multiple devices connected to a single RLD.

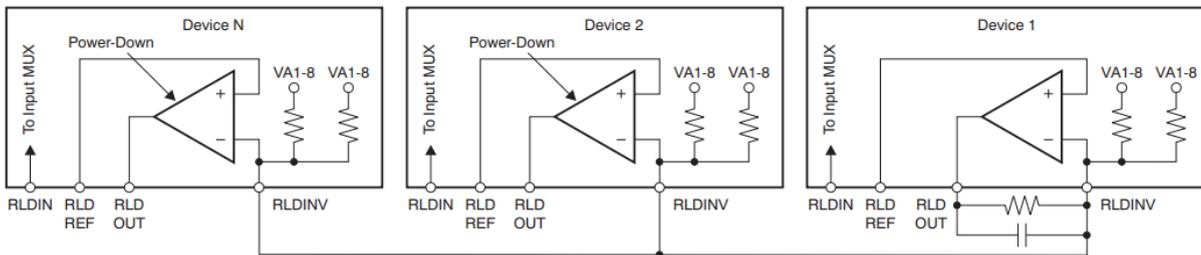


Figure 45. RLD connection of multiple devices

Pace Detect

The DADS129x provide flexibility for pace detection by using either software or external hardware. The software approach is made possible by providing sampling rates up to 32 kSPS. The external hardware approach is made possible by bringing out the output of the PGA at two pins: TESTP_PACE_OUT1 and TESTN_PACE_OUT2. If the WCT amplifier is connected to the signal path, switching noise occurs as a result of chopping; see the **Wilson Central Terminal (WCT) and Chest Leads** section for details.

Software Methods

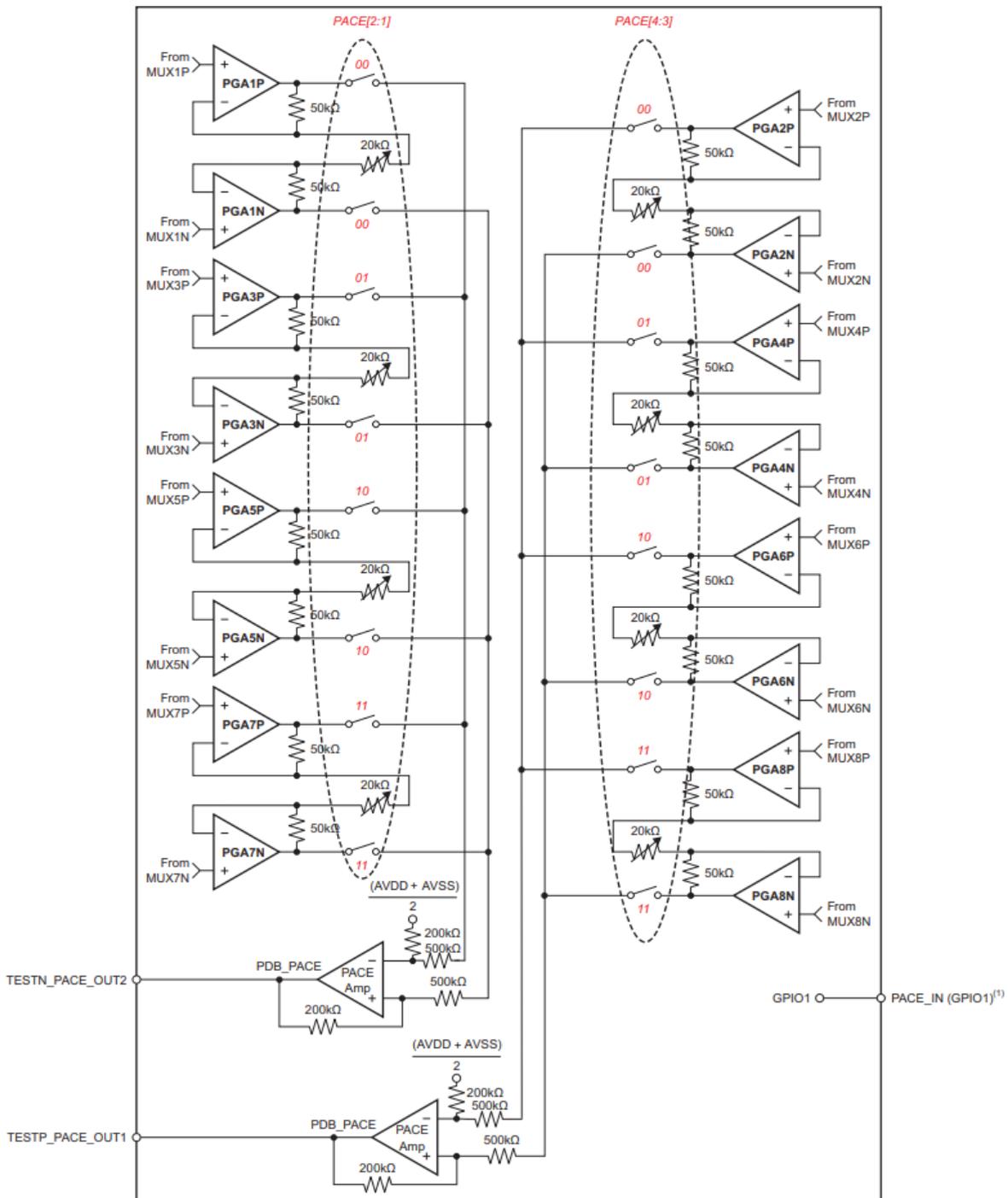
To use the software approach, operate the device at 8 kSPS or more to capture the fastest pulse. Afterwards, digital signal processing is used to identify the presence of the pacemaker pulse. The software approach gives the utmost flexibility to program the pace detect threshold on-the-fly (dynamically) using software. This flexibility is increasingly important as pacemakers evolve over time. Two parameters must be considered while measuring fast pace pulses:

1. PGA Bandwidth: Determines the available gain settings; as shown in Table 5.
2. Settling Time: Determines the operating data rate of the device. For a step change in the input, the digital decimation filter requires $3 \times t_{DR}$ time to stabilize.

External Hardware Method

One of the drawbacks of using the software approach is that all channels on a single device must operate at higher data rates. For systems where high data rates are a problem, the DADS129x provide the option of connecting external hardware to the output of the PGA to detect the presence of the pulse. The output of the pace detection logic is then fed into the device through one of the GPIO pins. The GPIO data are transmitted through the SPI port and loaded 2 tCLKs before DRDY goes low. Two of the eight channels are selected using register bits in the PACE register: one from the odd-numbered channels, and the other from the even-numbered channels. During the differential to single-ended conversion, there is an attenuation of 0.4; therefore, the total gain in the pace path is equal to $(0.4 \times \text{PGA_GAIN})$. The pace output signals are multiplexed with the TESTP and TESTN signals through the TESTP_PACE_OUT1 and TESTN_PACE_OUT2 pins, respectively. Channel selection is achieved by setting bits[4:1] of the PACE register. If the pace circuitry is not used, turn off the pace amplifiers by using the PD_PACE bit in the PACE register.

If the output of a channel connected to the WCT amplifier (for example, the V-lead channels) is connected to one of the pace amplifiers for external pace detection, chopping artifacts appear at the pace amplifier output. See the **Wilson Central Terminal (WCT) and Chest Leads** section for more details.



(1) GPIO1 can be used as the PACE_IN signal.

Figure 46. Hardware pace detection option

Digital Functions

GPIO pins (GPIO[4:1])

The DADS129x has a total of four general purpose digital input/output (GPIO) pins during normal operation. Each digital I/O pin can be individually configured as an input or output via the GPIOC bit in the GPIO register. The GPIOD bit in the GPIO register controls the logic level of the pin. When reading the GPIOD bit, the returned data is the logic level of the pin, regardless of whether it is programmed as an input or output. When a GPIO pin is configured as an input, writing to the corresponding GPIOD bit has no effect. When configured as an output, writing to the GPIOD bit will set the output value.

If configured as inputs, these pins must be driven; do not float these pins. The GPIO pins are set as inputs after power-on or after a reset. Figure 51 shows the GPIO port structure. If not used, short these pins to DGND.

For example, one configuration is to use GPIO1 as the PACEIN signal, multiplex GPIO2 with RESP_BLK signal, multiplex GPIO3 with the RESP signal, and multiplex GPIO4 with the RESP_PH signal.

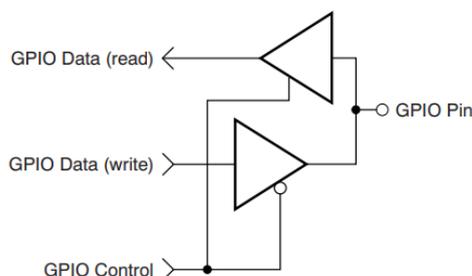


Figure 51. GPIO port pins

Power-down pin (PWDN)

Pulling PWDN low will power down all on-chip circuitry. To exit shutdown mode, bring the PWDN pin high. Once out of shutdown mode, the internal oscillator and reference will need to be powered on. It takes some time to wake up. During shutdown, the external clock is turned off to save power.

Reset (RESET pin and reset command)

The DADS129x can be reset in two ways: by pulling the RESET pin low or by sending a RESET opcode command (see the RESET: Reset Registers to Default Values section). Setting the RESET pin low forces a reset. Before setting the RESET pin high again, ensure that the minimum pulse width timing specification is followed. The RESET command takes effect on the eighth SCLK falling edge of the opcode command. After reset, it takes $18 t_{CLK}$ cycles to initialize the configuration registers to their default state and initiate a transition cycle. For more information, see RESET: Reset Registers to Default Values. An internal reset command is automatically sent to the digital filter whenever the CONFIG1 and RESP registers are set to their new values using the WREG command.

Digital Decimation Filter

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs are made between resolution and data rate: filter more for higher resolution, filter less for higher data rates. Higher data rates are typically used in ECG applications to implement software pace detection and ac lead-off detection. The digital filter on each channel consists of a third-order sinc filter. The decimation ratio on the sinc filters is adjusted by the DR bits in the CONFIG1 register (see Table 16 for details). This setting is a global setting that affects all channels; therefore, in these devices, all channels operate at the same data rate.

Clock

The DADS129x offers two different device timing methods: internal and external. The internal clock is ideal for low-power, battery-powered systems. The internal oscillator is calibrated for accuracy at room temperature. This accuracy varies over a specified temperature range; see Electrical Characteristics. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit.

Use the CLKSEL pin to select the internal or external clock. The CLK_EN bit in the CONFIG1 register enables and disables the oscillator clock output on the CLK pin. Table 11 shows the truth table for these two pins. Use the CLK_EN bit when multiple devices are daisy-chained. During shutdown, the external clock is turned off to save power.

Table 11. CLKSEL pin and CLK_EN bit

| CLKSEL pin | CONFIG1.CLK_EN bit | Clock source | CLK pin status |
|------------|--------------------|---------------------------|-----------------------------------|
| 0 | X | External clock | Input: External clock |
| 1 | 0 | Internal clock oscillator | Tri-state |
| 1 | 1 | Internal clock oscillator | Output: Internal clock oscillator |

Device Functional Mode

Data collection

This section describes the data acquisition process related to the START and DRDY pins, stable data, and data readback.

Start mode

Pull the START pin high for at least 2 t_{CLK} periods, or send the START command to begin conversions. When the START pin is low, or if the START command has not been sent, the device does not issue a DRDY signal (conversions are halted).

When using the START opcode to begin conversions, hold the START pin low. The DADS129x feature two modes to control conversion: continuous and single-shot. The mode is selected by SINGLE_SHOT (bit 3 of the CONFIG4 register). In multiple device configurations, the START pin is used to synchronize devices (see the Multiple-Device Configuration section for more details).

Establishment time

The setup time (t_{SETTLE}) is the time required for the converter to output fully stable data when the START signal is pulled high.

When the START pin is pulled high, or when the START command is sent, the device ADCs convert the input signals and DRDY is pulled high. The next falling edge of DRDY indicates that data are ready. Figure 57 shows the timing diagram and Table 12 shows the settling time for different data rates as a function of t_{CLK} . The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR[2:0] bits in the CONFIG1 register).

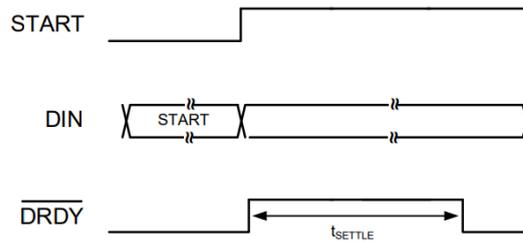


Figure 57. Setup time for the initial conversion

Table 12. Setup time for different data rates (t_{SETTLE})

| DR[2:0] | Setup time (t_{CLK} cycle) | |
|---------|-------------------------------|----------------|
| | High resolution mode | Low power mode |
| 000 | 296 | 584 |
| 001 | 584 | 1160 |
| 010 | 1160 | 2312 |
| 011 | 2312 | 4616 |
| 100 | 4616 | 9224 |
| 101 | 9224 | 18440 |
| 110 | 18440 | 36872 |

When the START pin is held high and there is a step change in the input signal, $3 \times t_{DR}$ conversion cycles are required for the filter to settle to the new value, as shown in Figure 58. Settled data are available on the fourth DRDY pulse. This settling time must be considered when trying to measure narrow pace pulses for pace detection. Data are available to read at each DRDY high-to-low transition, but can be ignored.

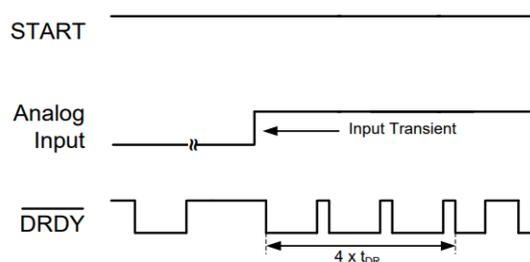


Figure 58. Settlement time of input transient

Data Ready Pin (DRDY)

The DRDY pin is the output pin. When DRDY transitions low, new transition data is ready. The CS signal has no effect on the data ready signal. Regardless of the state of the CS signal, a rising edge on SCLK will pull DRDY high. Therefore, when using multiple devices on the SPI bus, CS is used to strobe SCLK. The behavior of DRDY depends on whether the device is in RDATA mode or whether data is read on demand using the RDATA command. For more details, see the RDATA: Continuous Data Reading and RDATA: Reading Data sections. When reading data using the RDATA command, the read operation may overlap with the next DRDY, but this will not cause data corruption. Use the START pin or the START command to put the device into normal data capture mode or pulse data capture mode. Figure 59 shows the relationship between DRDY, DOUT, and SCLK during data retrieval (for the DADS129x with a selected data rate that provides 24-bit resolution). DOUT is latched on the rising edge of SCLK. Whether retrieving data from the device or sending commands via the DIN pin, the device will pull DRDY high on the first falling edge of SCLK. Data begins with the MSB of the status word and then sequentially enters the ADC channel data (i.e., channel 1, channel 2, ..., channel x). Power-off channels still have a position in the data stream; however, the data is invalid and can be ignored.

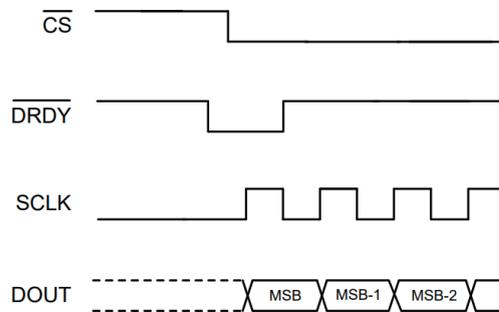


Figure 59. DRDY (CS = 0) with data retrieval

Regardless of the state of CS, the DRDY signal will be cleared on the first falling edge of SCLK. The DRDY signal will still be cleared even if no data is output with the clock. Consider this scenario if using the SPI bus to communicate with other devices on the same bus. Figure 60 shows the timing diagram for this multiplexing.

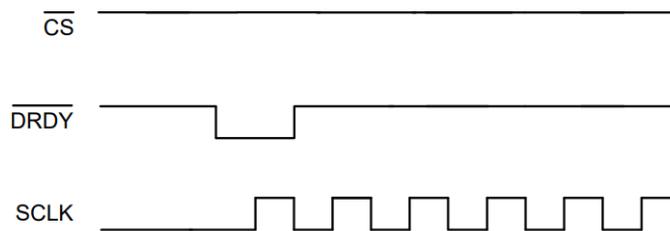


Figure 60. DRDY and SCLK behavior of SPI bus multiplexing

Data retrieval

Data retrieval can be completed using one of the following two methods:

1. RDATA: Continuous Read Data Command sets the device mode for continuously reading data without sending opcodes. For more details, please refer to RDATA: Continuous Data Reading section.
2. RDATA: The Read Data command reads only one data output from the device. For more details, see the RDATA: Read Data section. For more details, please refer to the SPI command definition section.

The conversion data are read by shifting the data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. DRDY returns to high on the first SCLK falling edge. Keep DIN low for the entire readoperation.

Status word

The DADS129x data readback is preceded by a status word that provides information on the state of the ADC. The status word is 24 bits long and contains the values for LOFF_STATP, LOFF_STATN, and part of the GPIO registers. The content alignment is shown in Figure 61.

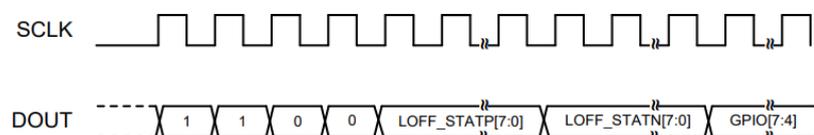


Figure 61. Status word content

Readback length

The number of bits in the data output depends on the number of channels and the number of bits per channel. The data format for each channel data is two's complement and MSB first. For the DADS129x with 32-kSPS and 64-kSPS data rates, the number of data bits is 24 status bits + 16 bits per channel × 8 channels = 152 bits. For all other data rates, the number of data bits is 24 status bits + 24 bits per channel × 8 channels = 216 bits. When channels are powered down using the user-register setting, the corresponding channel output is set to 0. However, the sequence of channel outputs remains the same. The DADS1294 outputs four channels of data and the DADS1296 outputs six channels of data.

The DADS129x also provide a multiple-readback feature. Set the DAISY_IN bit in the CONFIG1 register to 1 for multiple readbacks. Simply provide additional SCLKs to read data multiple times; the MSB data byte repeats after reading the last byte.

Data format

The DADS129x output 24 bits of data per channel in binary two's complement format, MSB first. The LSB has a weight of $V_{REF} / (2^{23} - 1)$. A positive full-scale input produces an output code of 7FFFFFFh and the negative fullscale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 13 summarizes the ideal output codes for different input signals. For DR[2:0] = 000 and 001, the device has only 17 and 19 bits of resolution, respectively. The last seven (in 17-bit mode) or five (in 19-bit mode) bits can be ignored.

Table 13. Relationship between ideal output code and input signal ⁽¹⁾

| Input signal, V_{IN} (INxP - INxN) | Ideal output code ⁽²⁾ |
|---|----------------------------------|
| $\geq V_{REF}$ | 7FFFFFFh |
| $V_{REF} / (2^{23} - 1)$ | 000001h |
| 0 | 000000h |
| $-V_{REF} / (2^{23} - 1)$ | FFFFFFh |
| $\leq -V_{REF} / (2^{23} / (2^{23} - 1))$ | 800000h |

(1) Only valid for 24-bit resolution data rates (gain = 1).

(2) Excludes the effects of noise, linearity, offset and gain error.

Single-shot mode

Enable single-shot mode by setting the SINGLE_SHOT bit in CONFIG4 register to 1. In single-shot mode, the DADS129x perform a single conversion when the START pin is taken high, or when the START opcode command is sent. As seen in Figure 62, when a conversion completes, DRDY goes low and further conversions are stopped. Regardless of whether the conversion data are read or not, DRDY remains low. To begin a new conversion, take the START pin low and then back high for at least two t_{CLK} s, or transmit the START opcode again. When switching from continuous conversion mode to single-shot mode, make sure the START signal is pulsed, or issue a STOP command followed by a START command.

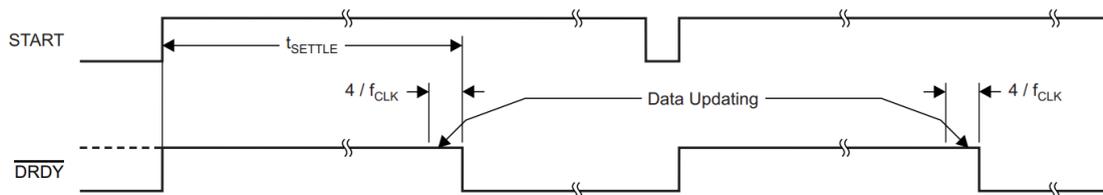


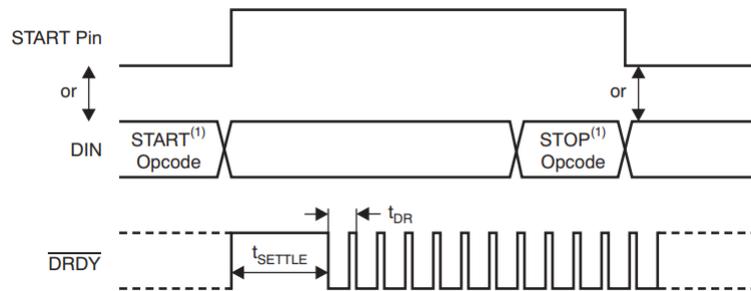
Figure 62. DRDY (Single-shot mode) without data retrieval

Single-shot conversion mode is provided for applications that require nonstandard or noncontinuous data rates. Issue a START command or toggle the START pin high to reset the digital filter, effectively dropping the data rate by a factor of four. This mode leaves the system more susceptible to aliasing effects, thus requiring more complex analog or digital filtering. Loading on the host processor increases because it must toggle the START pin or send a START command to initiate a new conversion cycle.

Continuous conversion mode

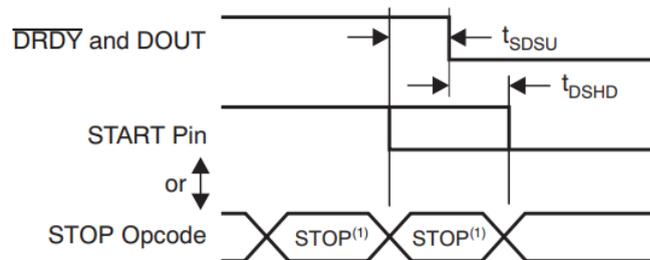
A conversion begins when the START pin is set high and held for at least two t_{CLK} cycles, or when a START opcode command is sent. As shown in Figure 63, DRDY goes high after the conversion begins and low once the data is ready. The conversion continues indefinitely until the START pin is set low or a STOP opcode command is sent. The ongoing conversion is allowed to complete when the START pin is pulled low or a stop command is issued.

Figure 64 and Table 14 show the timing of the START pin and the DRDY commands required to control the conversion in this mode. To keep the converter running continuously, the START pin should be permanently held high. Switching from single-pulse mode to continuous conversion mode is achieved by sending a START pulse signal, or by issuing a STOP command followed by a START command. This conversion mode is ideal for applications requiring a continuous stream of conversion results.



(1) The START and STOP commands take effect on the seventh falling edge of SCLK at the end of the opcode transmission.

Figure 63. Continuous Conversion Mode



(1) The START and STOP commands take effect on the seventh falling edge of SCLK at the end of the opcode transmission.

Figure 64. Timing from START to DRDY

Table 14. Timing requirements of Figure 64 (1)

| | | Min | Max | Unit |
|------------|---|-----|-----|-----------|
| T_{SDSU} | START pin is set low or a STOP opcode is sent to DRDY to abort further conversion during the setup time | 16 | | t_{CLK} |
| T_{DSHD} | START pin is set low or a STOP opcode is sent to complete the current conversion | 16 | | t_{CLK} |

(1) The START and STOP commands take effect on the seventh falling edge of SCLK at the end of the opcode transmission.

Multi-device configuration

The DADS129x provide configuration flexibility when multiple devices are connected in a system. The serial interface typically requires four signals: DIN, DOUT, SCLK, and CS. With one additional chip select signal per device, multiple devices can be connected together. The number of signals required to interface n devices is 3 + n.

Daisy-chain the RLD amplifiers as explained in the RLD Configuration with Multiple Devices section. To use the internal oscillator in a daisy-chain configuration, set one of the devices as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock brought out of the device by setting the CLK_EN register bit to 1. Use this master device clock as the external clock source for the other devices.

When using multiple devices, synchronize the devices with the START signal. The delay from the START signal to the DRDY signal is fixed for a fixed data rate (see the Start Mode section for more details on the settling times). As an example, Figure 65 shows the behavior of two devices when synchronized with the START signal.

There are two configurations used to connect multiple devices with a optimal number of interface pins: cascade or daisy-chain.

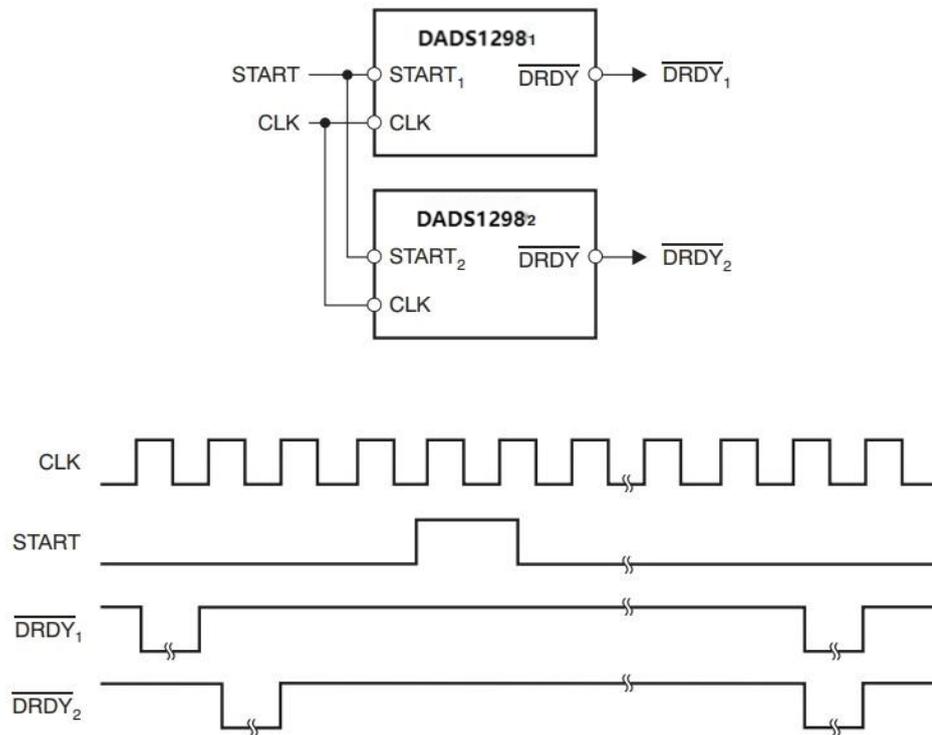


Figure 65. Synchronizing multiple converters

Cascade configuration

Figure 66(a) shows a configuration with two devices cascaded together. One of the devices is an DADS1298 (eight channels) and the other

is an DADS1294 (four channels). Together, they create a system with 12 channels. DOUT, SCLK, and DIN are shared. Each device has its own

chip select. When a device is not selected by the corresponding CS being driven to logic 1, the DOUT of this device is high-impedance. This

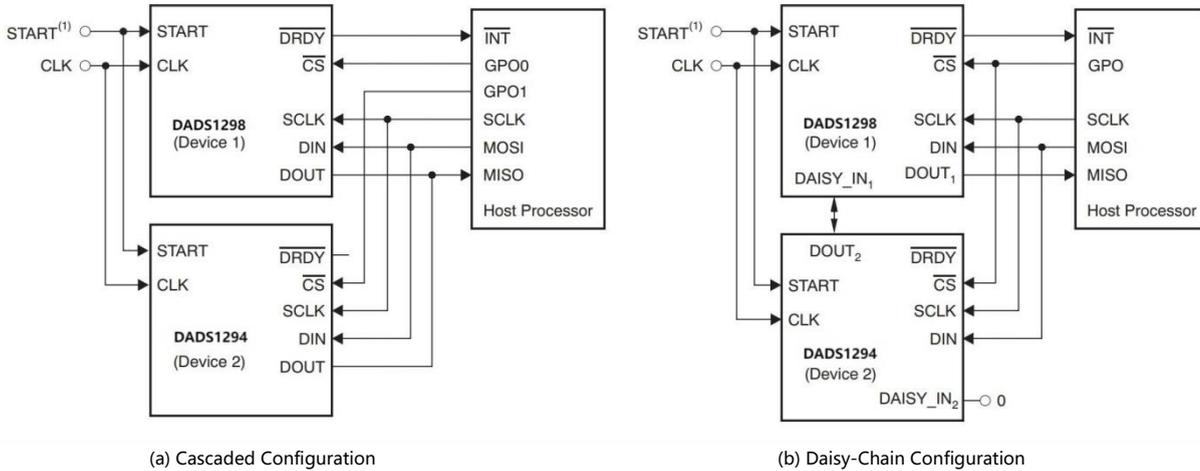
structure allows the other device to take control of the DOUT bus. This configuration method is suitable for the majority of applications.

Daisy-chain configuration

Enable daisy-chain mode by setting the DAISY_EN bit in the CONFIG1 register. Figure 66(b) shows the daisychain configuration. In this configuration, SCLK, DIN, and CS are shared across multiple devices. Connect the DOUT pin of the first device to the DAISY_IN pin of the next device, thereby creating a chain. Issue one extra SCLK between each data set. Note that when using daisy-chain mode, the multiple readback feature is not available. Short the DAISY_IN pin to digital ground if not used. Figure 2 describes the required timing for the

DADS1294/1296/1298 Low-Power, 4/6/8-Channel, Low-Noise, 24-Bit ADC for Physiological Signal Measurement

DADS1298 shown in Figure 67. Data from the DADS1298 appear first on DOUT, followed by a don't care bit, and finally by the status and data words from the DADS1294.



(a) Cascaded Configuration (1) To reduce the number of pins, set the START pin to low and use the START opcode command to synchronize and start the conversion.

Figure 66. Multi-device configuration

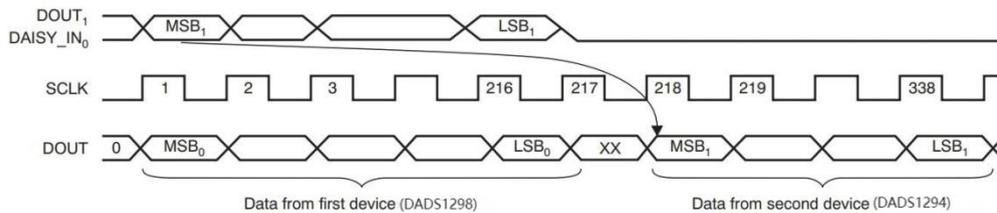


Figure 67. Daisy chain timing of Figure 66(b)

Important reminder when using the daisy chain pattern:

1. Issue one extra SCLK between each data set (see Figure 67).
2. All devices are configured to the same register values because CS is shared.
3. Device register readback (RREG) is only valid for device 0 in the daisy chain. Only conversion data can be read from device 1 to device N, where N is the last device in the chain; register data cannot be read.

If all devices in the chain operate in the same register setting, DIN can be shared, thereby reducing the SPI communication signals to four, regardless of the number of devices. However, the individual devices cannot be programmed; therefore, the RLD driver cannot be shared among the multiple devices. Furthermore, an external clock must be used.

As shown in Figure 2, the SCLK rising edge shifts data out of the DADS129x on DOUT. The SCLK rising edge is also used to latch data into the device DAISY_IN pin down the chain. This architecture allows for a faster SCLK rate speed, but it also makes the interface sensitive to board-level signal delays. The more devices in the chain, the more challenging it becomes to adhere to setup and hold times. A star-pattern connection of SCLK to all devices, minimizing length of DOUT, and other PCB layout techniques help. Placing delay circuits such as buffers between DOUT and DAISY_IN is another way to mitigate this challenge. One other option is to insert a D flip-flop between DOUT and DAISY_IN clocked on an inverted SCLK. In addition, note that daisy-chain mode requires some software overhead to recombine data bits spread across byte boundaries.

The maximum number of daisy-chained devices depends on the data rate at which the device is operated. The maximum number of devices can be estimated with Equation 6:

$$N_{\text{DEVICES}} = \frac{f_{\text{SCLK}}}{f_{\text{DR}} (N_{\text{BITS}})(N_{\text{CHANNELS}}) + 24}$$

where

- N_{BITS} = device resolution (depends on data rate)
 - N_{CHANNELS} = number of channels in the device (4, 6, or 8)
- (6)

For example, when the DADS1298 (8-channel, 24-bit version) is running at a data rate of 2kSPS and a 4MHz f_{SCLK} , up to 10 devices can be daisy-chained together.

Programming

SPI Interface

The SPI-compatible serial interface includes four signals: CS, SCLK, DIN, and DOUT. This interface reads converted data, reads and writes registers, and controls the operation of the DADS129x. The DRDY output serves as a status signal to indicate when data is ready. DRDY goes low when new data is available.

Chip Select Pin (CS)

The Chip Select (CS) option selects the DADS129x device for SPI communication. When CS is low, the serial interface is active. CS must remain low throughout the entire serial communication process. After serial communication is complete, always wait four or more t_{CLK} cycles before setting CS high. When CS is high, the serial interface resets, SCLK and DIN are ignored, and DOUT enters a high-impedance state. DRDY becomes active when data conversion is complete, regardless of whether CS is high or low.

When the DADS129x is selected, the device attempts to decode and execute a command every eight serial clock cycles. If the device stops executing serial commands, an extra clock pulse may have occurred, causing the serial interface to enter an unknown state. To reset the serial interface to a known state, set CS high and then low again.

Serial Clock (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. It is used to shift in commands and shift out data from the device. The serial clock (SCLK) features a Schmitt-triggered input, and clocks data on the DIN and DOUT pins into and out of the DADS129x. Even though the input has hysteresis, keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. The absolute maximum limit for SCLK is specified in the Timing Requirements: Serial Interface table.

While DADS129x is selected (CS = low), the device attempts to decode and execute commands every eight serial clocks. Therefore, present multiples of eight SCLKs every serial transfer to keep the interface in a normal operating mode. If the interface ceases to function because of extra serial clocks, reset by toggling CS high and back low.

For a single device, the minimum speed required for SCLK depends on the number of channels, number of bits of resolution, and output data rate. For multiple cascaded devices, see the Cascade Configuration section. Equation 7 shows the calculation for minimum SCLK speed.

$$t_{SCLK} < (t_{DR} - 4t_{CLK}) / (N_{BITS} \times N_{CHANNELS} + 24) \quad (7)$$

For example, if the DADS1298 is used at 500-SPS (eight channels, 24-bit resolution), the minimum SCLK speed is 110 kHz.

Retrieve data either by putting the device in RDATA mode or by issuing a RDATA command for data on demand. The SCLK rate limitation of Equation 7 also applies to RDATA. For the RDATA command, the limitation applies if data must be read between two consecutive DRDY signals. Equation 7 assumes that there are no other commands issued between data captures.

SCLK timing method

As shown in Figure 68, there are two different SCLK clocking methods to satisfy the decode timing specification shown in Figure 1 for multiple-byte commands.

For SCLK speeds that meet the $t_{SDECODE}$ timing requirement shown in Figure 1, transmit SCLK in a continuous stream when CS is low. This method is not to be confused with a free-running SCLK, where SCLK operates when CS is high. Free-running SCLK operation is not supported by this device.

For faster SCLK speeds that do not meet the $t_{SDECODE}$ timing requirement, SCLK is transmitted in 8-bit bursts with a delay between bursts. The

absolute

maximum SCLK limit is specified in the Timing Requirements: Serial Interface table. Figure 68 shows the difference between the two SCLK clocking methods for this device.

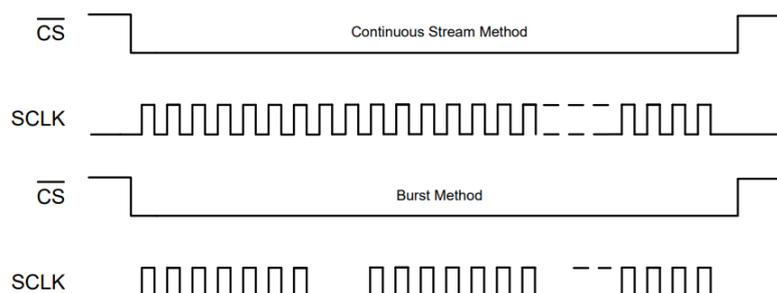


Figure 68. SCLK timing method

Data input pin (DIN)

The data input pin (DIN), along with SCLK, is used for communication with the DADS129x (opcode commands and register data). The device latches the data in DIN on the falling edge of SCLK.

Data output pin (DOUT)

The data output pin (DOUT), along with SCLK, is used to read conversion and register data from the DADS129x. Data in DOUT is shifted out on the rising edge of SCLK.

DOUT enters a high-impedance state when CS is high. In continuous read mode (see the SPI command definition section for more details), the DOUT output line also indicates when new data is available. Using this feature minimizes the number of connections between the device and the system controller. **Figure 69** shows the data output protocol of DADS1298.

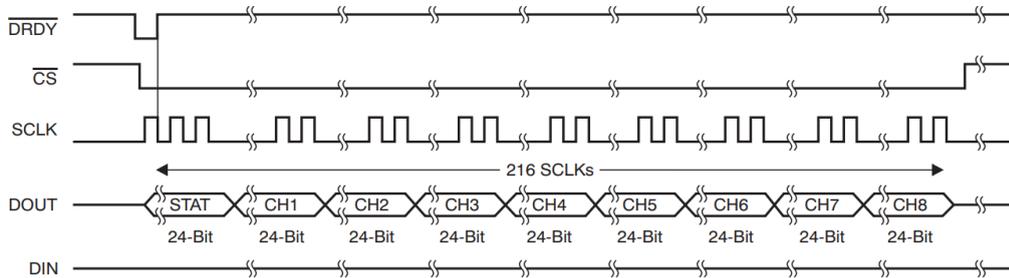


Figure 69. SPI bus data output of DADS1298 (eight channels)

SPI command definition

The DADS129x offers flexible configuration control. The opcode commands summarized in Table 15 control and configure the operation of the DADS129x. Opcode commands are independent, except for register read and register write operations that require a second command byte plus data. CS can be brought high or held low between opcode commands, but must remain low throughout the entire command operation (especially for multi-byte commands). System opcode commands and the RDATA command are decoded by the DADS129x on the seventh falling edge of SCLK.

Register read and write opcodes are decoded on the eighth falling edge of SCLK. When pulling CS high after issuing a command, ensure adherence to SPI timing requirements.

Table 15. Opcode Command Definitions

| Command | Description | First byte | Second byte |
|------------------------------|--|--------------------------------|--------------------------|
| System commands | | | |
| WAKEUP | Wake up from standby mode | 0000 0010 (02h) | -- |
| STANDBY | Enter standby mode | 0000 0100 (04h) | -- |
| RESET | Reset device | 0000 0110 (06h) | -- |
| START | Startup/Restart (Synchronous Conversion) | 0000 1000 (08h) | -- |
| STOP | Stop conversion | 0000 1010 (0Ah) | -- |
| Data read command | | | |
| RDATA | Start the continuous data reading mode, which is the default mode when powered on ⁽¹⁾ . | 0001 0000 (10h) | -- |
| SDATA | Stop continuous data reading mode | 0001 0001 (11h) | -- |
| RDATA | Data can be read via command; multiple readbacks are supported. | 0001 0010 (12h) | -- |
| Register read command | | | |
| RREG | Read register n starting from address r rrrr. | 001r rrrr (2xh) ⁽²⁾ | 000n nnnn ⁽²⁾ |
| WREG | Write to register n starting from address r rrrr. | 010r rrrr (4xh) ⁽²⁾ | 000n nnnn ⁽²⁾ |

(1) When in RDATA mode, the RREG command will be ignored.

(2) n nnnn = Number of registers to read/write – 1. For example, to read/write three registers, set n nnnn = 0 (0100). r rrrr = Start of read/write opcode Register address.

WAKEUP: Exit standby mode

The WAKEUP command can exit the low-power sleep mode; please refer to the STANDBY section: Entering Sleep Mode for details. It takes some time to exit the sleep mode (for more information, please refer to the electrical characteristics). For this command, there is no limit on the SCLK rate; the command can be issued at any time. Any subsequent commands must be sent after 4 t_{CLK} cycles.

STANDBY: Enter standby mode

The STANDBY operation code command can enter the low-power standby mode. All parts of the circuit except the reference part will be turned off. The power consumption in the standby mode is specified in the electrical characteristics. For this command, there is no limit on the SCLK rate; the command can be issued at any time. Sending the WAKEUP command can restore the device to its normal operating state. The serial interface is in an active state; therefore, register read and write commands can be executed in this mode.

RESET: Resets registers to their default values.

The RESET command can reset the digital filter cycle and restore all registers to their corresponding default values. For more detailed information, please refer to the "Reset (RESET Pin and Reset Command)" section. For this command, there is no limit on the SCLK rate; the command can be issued at any time. Executing the RESET command requires 18 t_{CLK} cycles. Do not send any commands during this period.

START: Begin conversion

This operation code can initiate data conversion. Keeping the START pin at a low level can control the conversion through commands. If the conversion is in progress, this command is invalid. The STOP operation code command is used to stop the conversion. If the START command is followed immediately by the STOP command, there must be a 4 t_{CLK} period interval between these two commands. When sending the START operation code to the device, keep the START pin at a low level until the STOP command is issued. (For more detailed information, please refer to the Startup Mode section of the SPI interface part.) For this command, there is no limit on the SCLK rate and the command can be issued at any time.

STOP: Stop the conversion

The STOP opcode stops the conversion. Holding the START pin low allows you to control the conversion via command. Sending the STOP command completes the ongoing conversion and stops any further conversions.

If the conversion has already stopped, then this command is invalid. There is no limit to the SCLK rate for this command; it can be issued at any time.

RDATAC: Continuous data reading

The RDATAC opcode enables the output of conversion data on each DRDY without the need to issue subsequent read data opcodes. This opcode places the conversion data in the output register where it may be shifted out directly. The read data continuous mode is the default mode of the device and the device defaults to this mode on power up and reset.

RDATAC mode is cancelled by the stop read data continuous command (SDATAC). If the device is in RDATAC mode, an SDATAC command must be issued before any other commands can be sent to the device. There is no restriction on the SCLK rate for this command. However, subsequent data retrieval SCLKs or the SDATAC opcode command must wait at least 4 t_{CLK} cycles. As shown in Figure 70, the timing for RDATAC illustrates the keep-out zone of 4 t_{CLK} periods around the DRDY pulse when this command cannot be issued. If no data are retrieved from the device, DOUT and DRDY behave similarly in this mode. To retrieve data from the device after RDATAC command is issued, make sure that either the START pin is high or the START command is issued. Figure 70 shows the recommended way to use the RDATAC command. RDATAC is ideally suited for applications such as data loggers or recorders, where registers are set once and do not need to be reconfigured.

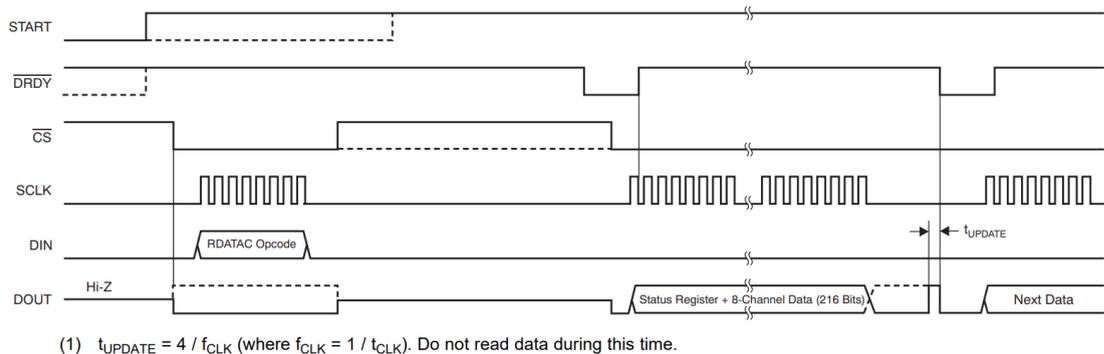


Figure 70. RDATAC Usage

Send multibyte command

The DADS129x serial interface decodes commands in bytes, and requires 4 t_{CLK} periods to decode and execute. Therefore, when sending multibyte commands, a 4 t_{CLK} period must separate the end of one byte (or opcode) and the next.

For example, if CLK is 2.048 MHz, then $t_{SDECODE}$ ($4 \times t_{CLK}$) is 1.96 μs . When SCLK is 16 MHz, the maximum transfer speed for one byte is 500

ns. This byte transfer time does not meet the $t_{SDECODE}$ specification; therefore, a delay must be inserted so that the end of the second byte arrives 1.46 μ s later. However, if SCLK is 4 MHz, one byte is transferred in 2 μ s. Because this transfer time exceeds the $t_{SDECODE}$ specification, the processor can send subsequent bytes without delay. In the second scenario, the serial port can be programmed to use multiplebyte transfers instead of the single-byte transfers required to meet the timing of the first scenario.

RREG: Read from register

The RREG opcode command can read the register data. The RREG command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to be read – 1.

The first opcode byte: 001r rrrr, where r rrrr is the starting register address.

The second opcode byte: 000n nnnn, where n nnnn is the number of registers to be read – 1.

On the 17th rising edge of the SCLK, the first register's MSB is output as shown in Figure 72. When the device is in the continuous read data mode, the SDATAC command must be issued first before the RREG command can be issued. The RREG command can be issued at any time. However, since this command is a multi-byte command, the SCLK rate is limited, depending on the way the SCLK is issued. For more details, please refer to the Serial Clock (SCLK) section. The CS must remain at a low level throughout the command operation.

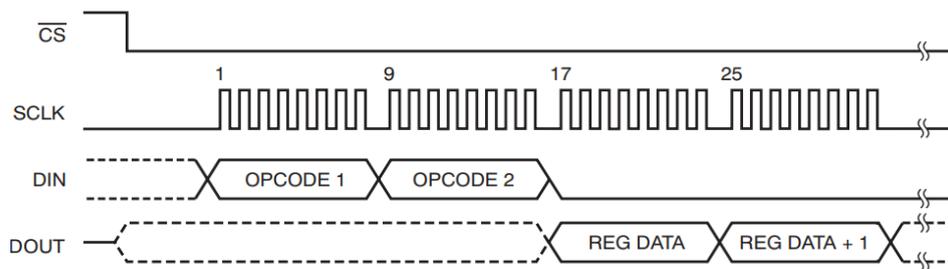


Figure 72. Example of RREG command: Read two registers starting from register 00h (ID register). (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

WREG: Write to a register

The WREG opcode command can write to register data. The WREG command is a two-byte opcode followed by the input of register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to be written – 1.

The first opcode byte: 010r rrrr, where r rrrr is the starting register address.

The second opcode byte: 000n nnnn, where n nnnn is the number of registers to be written – 1.

The opcode byte is followed by the register data (in the MSB-first format), as shown in Figure 73. The WREG command can be issued at any time. However, since this command is a multi-byte command, the SCLK rate is limited, depending on the way the SCLK is issued. For more details, please refer to the Serial Clock (SCLK) section. The CS must be at a low level throughout the command operation.

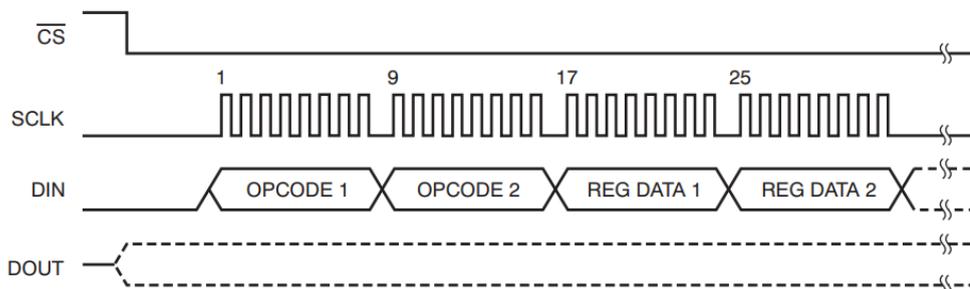


Figure 73. Example of the WREG command: Writing to two registers starting from register 00h (ID register). (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

Register mapping

| Address | Register | Reset value | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---------------------------|-------------|-------------|------------|------------|--------------|-----------------|------------|---------------|------------|
| Device settings (read-only registers) | | | | | | | | | | |
| 00h | ID | xx | REV_ID[2:0] | | | 1 | DEV_ID[1:0] | | NU_CH[1:0] | |
| Global settings on each channel | | | | | | | | | | |
| 01h | CONFIG1 | 06 | HR | DAISY_EN | CLK_EN | 0 | 0 | DR2 | DR1 | DR0 |
| 02h | CONFIG2 | 40 | 0 | 0 | WCT_CHOP | INT_TEST | 0 | TEST_AMP | TEST_FREQ1 | TEST_FREQ0 |
| 03h | CONFIG3 | 40 | PD_REFBUF | 1 | VREF_4V | RLD_MEAS | RLDREF_INT | PD_RLD | RLD_LOFF_SENS | RLD_STAT |
| 04h | LOFF | 00 | COMP_TH2 | COMP_TH1 | COMP_TH0 | VLEAD_OFF_EN | ILEAD_OFF1 | ILEAD_OFF0 | FLEAD_OFF1 | FLEAD_OFF0 |
| Determined by channel settings | | | | | | | | | | |
| 05h | CH1SET | 61 | PD1 | GAIN12 | GAIN11 | GAIN10 | 0 | MUX12 | MUX11 | MUX10 |
| 06h | CH2SET | 61 | PD2 | GAIN22 | GAIN21 | GAIN20 | 0 | MUX22 | MUX21 | MUX20 |
| 07h | CH3SET | 61 | PD3 | GAIN32 | GAIN31 | GAIN30 | 0 | MUX32 | MUX31 | MUX30 |
| 08h | CH4SET | 61 | PD4 | GAIN42 | GAIN41 | GAIN40 | 0 | MUX42 | MUX41 | MUX40 |
| 09h | CH5SET ⁽¹⁾ | 61 | PD5 | GAIN52 | GAIN51 | GAIN50 | 0 | MUX52 | MUX51 | MUX50 |
| 0Ah | CH6SET ⁽¹⁾ | 61 | PD6 | GAIN62 | GAIN61 | GAIN60 | 0 | MUX62 | MUX61 | MUX60 |
| 0Bh | CH7SET ⁽¹⁾ | 61 | PD7 | GAIN72 | GAIN71 | GAIN70 | 0 | MUX72 | MUX71 | MUX70 |
| 0Ch | CH8SET ⁽¹⁾ | 61 | PD8 | GAIN82 | GAIN81 | GAIN80 | 0 | MUX82 | MUX81 | MUX80 |
| 0Dh | RLD_SENSP ⁽²⁾ | 00 | RLD8P | RLD7P | RLD6P | RLD5P | RLD4P | RLD3P | RLD2P | RLD1P |
| 0Eh | RLD_SENSN ⁽²⁾ | 00 | RLD8N | RLD7N | RLD6N | RLD5N | RLD4N | RLD3N | RLD2N | RLD1N |
| 0Fh | LOFF_SENSP ⁽²⁾ | 00 | LOFF8P | LOFF7P | LOFF6P | LOFF5P | LOFF4P | LOFF3P | LOFF2P | LOFF1P |
| 10h | LOFF_SENSN ⁽²⁾ | 00 | LOFF8N | LOFF7N | LOFF6N | LOFF5N | LOFF4N | LOFF3N | LOFF2N | LOFF1N |
| 11h | LOFF_FLIP | 00 | LOFF_FLIP8 | LOFF_FLIP7 | LOFF_FLIP6 | LOFF_FLIP5 | LOFF_FLIP4 | LOFF_FLIP3 | LOFF_FLIP2 | LOFF_FLIP1 |
| Lead detachment status register (read-only register) | | | | | | | | | | |
| 12h | LOFF_STATP | 00 | IN8P_OFF | IN7P_OFF | IN6P_OFF | IN5P_OFF | IN4P_OFF | IN3P_OFF | IN2P_OFF | IN1P_OFF |
| 13h | LOFF_STATN | 00 | IN8N_OFF | IN7N_OFF | IN6N_OFF | IN5N_OFF | IN4N_OFF | IN3N_OFF | IN2N_OFF | IN1N_OFF |
| GPIO and other registers | | | | | | | | | | |
| 14h | GPIO | 0F | GPIOD4 | GPIOD3 | GPIOD2 | GPIOD1 | GPIOC4 | GPIOC3 | GPIOC2 | GPIOC1 |
| 15h | MISC1 | 00 | 0 | 0 | SRB1 | 0 | 0 | 0 | 0 | 0 |
| 16h | MISC2 | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17h | CONFIG4 | 00 | 0 | 0 | 0 | 0 | SINGLE_SH OT | 0 | PD_LOFF_COMP | 0 |
| 18h | WCT1 | 00 | aVF_CH6 | aVF_CH5 | aVR_CH7 | aVR_CH4 | PD_WCTA | WCTA2 | WCTA1 | WCTA0 |
| 19h | WCT2 | 00 | PD_WCTC | PD_WCTB | WCTB2 | WCTB1 | WCTB0 | WCTC2 | WCTC1 | WCTC0 |

(1) CH5SET and CH6SET are not applicable to DADS1294. CH7SET and CH8SET registers are not applicable to DADS1294 and DADS1296.

(2) Register bits [5:4] of RLD_SENSP, PACE_SENSP, LOFF_SENSP, LOFF_SENSN, and LOFF_FLIP are not applicable to DADS1294. Bits [7:6] are not applicable to DADS1294 and DADS1296.

Register Description

During device manufacturing, the read-only ID control register is programmed to indicate device characteristics.

ID: ID Control Register (Address = 00h) (Reset = xxh)

Figure 74. ID Control Register

| | | | | | | | |
|-------------|---|---|------|-------------|---|------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REV_ID[2:0] | | | 1 | DEV_ID[1:0] | | NU_CH[1:0] | |
| R-xh | | | R-1h | R-3h | | R-xh | |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 17. Description of ID Control Register Fields

| Bit | Fields | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7:5 | REV_ID[2:0] | R | xh | Device ID These bits indicate the chip version and are subject to change without notice. |
| 4 | reserve | R | 1h | Reserved Always read back 1 hour |
| 3:2 | DEV_ID[1:0] | R | 0h | Chip identifier. These bits indicate the chip type These bits indicate the number of channels. 00 = DADS1294/1296/1298 |
| 1:0 | NU_CH[1:0] | R | xh | Number of channels 00: 4-channel DADS1294 01: 6-channel DADS1296 10: 8-channel DADS1298 |

CONFIG1: Configuration Register 1 (Address = 01h) (Reset = 06h)
Figure 75. CONFIG1: Configuration Register 1

| | | | | | | | |
|--------|----------|--------|--------|--------|---------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HR | DAISY_EN | CLK_EN | 0 | 0 | DR[2:0] | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-6h | | |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 17. Description of ID Control Register Fields

| Bit | Fields | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7 | HR | R/W | 0h | High resolution or low power mode This bit determines whether the device operates in low-power mode or high-resolution mode. 0 = LP mode 1 = HR Model |
| 6 | DAISY_EN | R/W | 0h | Daisy chain or multi-read-back mode This bit determines which mode to enable. 0 = Daisy chain pattern 1 = Multiple readback mode |
| 5 | CLK_EN | R/W | 0h | CLK connection This bit determines whether the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1. 0 = Disable oscillator clock output 1 = Enable oscillator clock output |
| 4:3 | Reserved | R/W | 0h | Reserved Always write 0h |
| 2:0 | DR[2:0] | R/W | 6h | Output data rate For high-resolution mode, $f_{MOD} = f_{CLK} / 4$. Below low-power mode, $f_{MOD} = f_{CLK} / 8$. These bits determine the output data rate of the device. 000: $f_{MOD} / 16$ (HR mode: 32kSPS, LP mode: 16kSPS) 001: $f_{MOD} / 32$ (HR mode: 16kSPS, LP mode: 8kSPS) 010: $f_{MOD} / 64$ (HR mode: 8kSPS, LP mode: 4kSPS) 011: $f_{MOD} / 128$ (HR mode: 4kSPS, LP mode: 2kSPS) 100: $f_{MOD} / 256$ (HR mode: 2kSPS, LP mode: 1kSPS) 101: $f_{MOD} / 512$ (HR mode: 1kSPS, LP mode: 500SPS) 110: $f_{MOD} / 1024$ (HR mode: 500SPS, LP mode: 250SPS) 111: Reserved (not used) |

(1) It consumes additional power when driving external devices.

CONFIG2: Configuration Register 2 (Address = 02h) (Reset = 40h)

Configuration register 2 allows you to configure test signal generation. See the Input Multiplexer section for more details.

Figure 76. CONFIG2: Configuration Register 2

| | | | | | | | |
|--------|--------|----------|----------|--------|----------|----------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | WCT_CHOP | INT_TEST | 0 | TEST_AMP | TEST_FREQ[1:0] | |
| R/W-1h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 19. Description of Fields in Configuration Register 2

| Bit | Fields | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7:6 | Reserved | R/W | 0h | Reserved Always write 0h |
| 5 | WCT_CHOP | R/W | 0h | WCT chopper solution This bit determines whether the chopping frequency of the WCT amplifier is variable or fixed. 0 = The chopping frequency is variable; please refer to Table 7. 1 = The chopping frequency remains constant at $f_{MOD} / 16$ |
| 4 | INT_TEST | R/W | 0h | Test source This bit determines the test signal source. 0 = Externally driven test signal 1 = Generate test signals internally |
| 3 | Reserved | R/W | 0h | Reserved Always write 0h |
| 2 | TEST_AMP | R/W | 0h | Test signal amplitude These bits determine the amplitude of the calibration signal. 0 = $1 \times - (VREFP - VREFN) / 2400V$ 1 = $2 \times - (VREFP - VREFN) / 2400V$ |
| 1:0 | TEST_FREQ[1:0] | R/W | 0h | Test signal frequency These bits determine the frequency of the calibration signal. Send pulse signals at a frequency of $f_{CLK} / 2^{21}$ 01 = Send pulse signals at a frequency of $f_{CLK} / 2^{20}$ 10 = Unused 11 = DC |

CONFIG3: Configuration register 3 (address = 03h) (reset = 40h)

Configuration register 3 can be configured for multi-baseline and RLD operations.

Figure 77. CONFIG3: Configuration Register 3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|--------|---------|----------|------------|--------|---------------|----------|
| PD_REFBUF | 1 | VREF_4V | RLD_MEAS | RLDREF_INT | PD_RLD | RLD_LOFF_SENS | RLD_STAT |
| R/W-0h | R/W-1h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 20. Description of the 3 fields in the configuration register

| Bit | Fields | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 7 | PD_REFBUF | R/W | 0h | Shutdown reference buffer This bit determines the state of the reference buffer when it is turned off. 0 = Turn off internal reference buffer 1 = Enable internal reference buffer |
| 6 | Reserved | R/W | 1h | Reserved Always write for 1 hour |
| 5 | VREF_4V | R/W | 0h | Reference voltage This bit determines the reference voltage VREFP. 0 = VREFP is set to 2.4V. 1 = VREFP is set to 4V (only works with 5V analog power supplies). |
| 4 | RLD_MEAS | R/W | 0h | RLD Measurement This bit enables RLD measurement. The RLD signal can be measured using any channel. 0 = Open path 1 = The RLD_IN signal is routed to the channel with MUX_Setting 010 (V_{REF}). |
| 3 | RLDREF_INT | R/W | 0h | RLDREF signal This bit determines the source of the RLDREF signal. 0 = RLDREF signal fed from outside 1 = Internally generate RLDREF signal $(AVDD - AVSS)/2$ |
| 2 | PD_RLD | R/W | 0h | RLD buffer power supply This bit determines the power supply state of the RLD buffer. 0 = RLD buffer de-energized 1 = Enable RLD buffer |
| 1 | RLD_LOFF_SENS | R/W | 0h | RLD sensing function This bit enables RLD sensing functionality. 0 = Disable RLD sensing 1 = Enable RLD sensing |
| 0 | RLD_STAT | R | 0h | RLD lead detachment status This bit determines the RLD state. 0 = RLD is connected 1 = RLD is not connected |

LOFF: Lead detachment control register (address = 04h) (reset = 00h)

The lead detachment control register configures the lead detachment detection operation.

Figure 78. LOFF: Lead detachment control register

| | | | | | | | |
|---------------|---|---|--------|----------------|---|----------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMP_TH2[2:0] | | | 0 | ILEAD_OFF[1:0] | | FLEAD_OFF[1:0] | |
| R/W-0h | | | R/W-0h | R/W-0h | | R/W-0h | |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 21. Description of Lead Detachment Control Register Fields

| Bit | Fields | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7:5 | COMP_TH[2:0] | R/W | 0h | Lead-off comparator threshold positive side of comparator 000 = 95% 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70% negative side of comparator 000 = 5% 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30% |
| 4 | Reserved | R/W | 0h | Reserved. Always write 0h. |
| 3:2 | ILEAD_OFF[1:0] | R/W | 0h | Lead-off current amplitude These bits determine the current amplitude of the current lead detachment mode. 00 = 6mA 01 = 24mA 10 = 6μA 11 = 24μA |
| 1:0 | FLEAD_OFF[1:0] | R/W | 0h | Lead drop frequency These bits determine the frequency of lead detachment detection for each channel. 00 = DC lead detection 01 = AC lead detachment detection at 7.8Hz ($f_{CLK} / 2^{18}$) 10 = AC lead detachment detection at 31.2Hz ($f_{CLK} / 2^{16}$) 11 = AC lead dropout detection at $f_{DR} / 4$ |

CHnSET: Channel settings (n = 1 to 8) (address = 05h to 0Ch) (reset = 00h)

The CH[1:8]SET control register configures the power mode, PGA gain, and multiplexer settings for the channels. See the Input Multiplexer section for more information. CH[2:8]SET is similar to CH1SET (corresponding to the corresponding channels).

Figure 79. CHnSET: Channel setting registers

| | | | | | | | |
|--------|------------|---|---|--------|-----------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PDn | GAINn[2:0] | | | SRB2 | MUXn[2:0] | | |
| R/W-0h | R/W-6h | | | R/W-0h | R/W-0h | | |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 22. Description of Fields for Each Channel Setting (n = 1 to 8)

| Bit | Fields | Type | Reset | Description |
|-----|------------|------|-------|---|
| 7 | PDn | R/W | 0h | Power outage This bit determines the channel power mode for the corresponding channel. 0 = Normal operation 1 = Channel power failure When powering off a channel, TI recommends setting the CHnSET register. MUXn[2:0] = 001, so that the channel is set to short-circuit input. |
| 6:4 | GAINn[2:0] | R/W | 6h | PGA gain These bits determine the PGA gain settings. 0 00 = 1 001 = 2 010 = 4 011 = 6 100 = 8 101 = 12 110 = 24 |
| 3 | SRB2 | R/W | 0h | SRB2 connection This bit determines the SRB2 connection of the corresponding channel. 0 : Disconnect 1 : Closed |
| 2:0 | MUXn[2:0] | R/W | 1h | Channel input These bits determine the channel input selection. 000 = Normal electrode input 001 = Input short circuit (for offset or noise measurements) 010 = Used in conjunction with the RLD_MEAS bit used for RLD measurements. 011 = MVDD, used for power supply measurement 100 = Temperature sensor 101 = Test signal 110 = RLD_DRP (positive electrode is the driver) 111 = RLD_DRN (Negative electrode is the driver) |

RLD_SENSP: RLD positive signal export register (address = 0Dh) (reset = 00h)

This register controls the positive signal selection for each channel (used for the right leg drive (RLD)). See the Right Leg Drive (RLD) DC Bias Current section for more information.

Register bits [5:4] are not applicable to DADS1294. Bits [7:6] are not applicable to DADS1294 and DADS1296.

Figure 80. RLD_SENSP: RLD Positive Signal Derivation Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| RLD8P | RLD7P | RLD6P | RLD5P | RLD4P | RLD3P | RLD2P | RLD1P |
| R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 23. Description of RLD Positive Signal Derived Fields

| Bit | Fields | Type | Reset | Description |
|-----|--------|------|-------|--|
| 7 | RLD8P | R/W | 0h | N8P to RLD Route the positive signal of channel 8 to the RLD export. 0 : Disabled 1 : Enable |
| 6 | RLD7P | R/W | 0h | N7P to RLD Route the positive signal of channel 7 to the RLD export. 0 : Disabled 1 : Enable |
| 5 | RLD6P | R/W | 0h | N6P to RLD Route the positive signal of channel 6 to the RLD export. 0 : Disabled 1 : Enable |
| 4 | RLD5P | R/W | 0h | N5P to RLD Route the positive signal of channel 5 to the RLD export. 0 : Disabled 1 : Enable |
| 3 | RLD4P | R/W | 0h | N4P to RLD Route the positive signal of channel 4 to the RLD export. 0 : Disabled 1 : Enable |
| 2 | RLD3P | R/W | 0h | N3P to RLD Route the positive signal of channel 3 to the RLD export. 0 : Disabled 1 : Enable |
| 1 | RLD2P | R/W | 0h | N2P to RLD Route the positive signal from channel 2 to the RLD export. 0 : Disabled 1 : Enable |
| 0 | RLD1P | R/W | 0h | N1P to RLD Route the positive signal of channel 1 to the RLD export. 0 : Disabled 1 : Enable |

RLD_SENSN: RLD negative signal export register (address = 0Eh) (reset = 00h)

This register controls the selection of the negative signal (used for the right leg drive output) for each channel. See the Right Leg Drive (RLD) DC Bias Current section for more information.

Register bits [5:4] are not applicable to DADS1294. Bits [7:6] are not applicable to DADS1294 and DADS1296.

Figure 80. RLD_SENSN: RLD Negative Signal Derivation Register

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RLD8N | RLD7N | RLD6N | RLD5N | RLD4N | RLD3N | RLD2N | RLD1N |
| R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 23. Description of RLD Negative Signal Derived Fields

| Bit | Fields | Type | Reset | Description |
|-----|--------|------|-------|---|
| 7 | RLD8N | R/W | 0h | IN8N to RLD Route the negative signal of channel 8 to the RLD export. 0 : Disabled 1 : Enable |
| 6 | RLD7N | R/W | 0h | IN7N to RLD Route the negative signal of channel 7 to the RLD export. 0 : Disabled 1 : Enable |
| 5 | RLD6N | R/W | 0h | IN6N to RLD Route the negative signal of channel 6 to the RLD export. 0 : Disabled 1 : Enable |
| 4 | RLD5N | R/W | 0h | IN5N to RLD Route the negative signal of channel 5 to the RLD export. 0 : Disabled 1 : Enable |
| 3 | RLD4N | R/W | 0h | IN4N to RLD The negative signal from channel 4 is routed to the RLD export. 0 : Disabled 1 : Enable |
| 2 | RLD3N | R/W | 0h | IN3N to RLD The negative signal from channel 3 is routed to the RLD export. 0 : Disabled 1 : Enable |
| 1 | RLD2N | R/W | 0h | IN2N to RLD The negative signal from channel 2 is routed to the RLD export. 0 : Disabled 1 : Enable |
| 0 | RLD1N | R/W | 0h | IN1N to RLD Routing the negative signal from channel 1 to the RLD export. 0 : Disabled 1 : Enable |

RLD_SENSN: RLD negative signal export register (address = 0Eh) (reset = 00h)

This register controls the selection of the negative signal (used for the right leg drive output) for each channel. See the Right Leg Drive (RLD) DC Bias Current section for more information.

Register bits [5:4] are not applicable to DADS1294. Bits [7:6] are not applicable to DADS1294 and DADS1296.

Figure 81. RLD_SENSN: RLD Negative Signal Derivation Register

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RLD8N | RLD7N | RLD6N | RLD5N | RLD4N | RLD3N | RLD2N | RLD1N |
| R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 23. Description of RLD Negative Signal Derived Fields

| Bit | Fields | Type | Reset | Description |
|-----|--------|------|-------|---|
| 7 | RLD8N | R/W | 0h | IN8N to RLD Route the negative signal of channel 8 to the RLD export. 0 : Disabled 1 : Enable |
| 6 | RLD7N | R/W | 0h | IN7N to RLD Route the negative signal of channel 7 to the RLD export. 0 : Disabled 1 : Enable |
| 5 | RLD6N | R/W | 0h | IN6N to RLD Routing the negative signal of channel 6 to the RLD export. 0 : Disabled 1 : Enable |
| 4 | RLD5N | R/W | 0h | IN5N to RLD Route the negative signal of channel 5 to the RLD export. 0 : Disabled 1 : Enable |
| 3 | RLD4N | R/W | 0h | IN4N to RLD The negative signal from channel 4 is routed to the RLD export. 0 : Disabled 1 : Enable |
| 2 | RLD3N | R/W | 0h | IN3N to RLD The negative signal from channel 3 is routed to the RLD export. 0 : Disabled 1 : Enable |
| 1 | RLD2N | R/W | 0h | IN2N to RLD The negative signal from channel 2 is routed to the RLD export. 0 : Disabled 1 : Enable |
| 0 | RLD1N | R/W | 0h | IN1N to RLD Routing the negative signal from channel 1 to the RLD export. 0 : Disabled 1 : Enable |

LOFF_SENSP: Positive signal lead disconnection detection register (address = 0Fh) (reset = 00h)

This register selects the positive side of each channel (for lead detachment detection). See the Lead Detachment Detection section for details.

The LOFF_STATP register bits are only valid if the corresponding LOFF_SENSP bits are set to 1.

Register bits [5:4] are not applicable to DADS1294. Bits [7:6] are not applicable to DADS1294 and DADS1296.

Figure 82. LOFF_SENSP: Positive signal lead dropout detection register

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOFF8P | LOFF7P | LOFF6P | LOFF5P | LOFF4P | LOFF3P | LOFF2P | LOFF1P |
| R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 25. Description of Positive Signal Lead Dropout Detection Field

| Bit | Fields | Type | Reset | Description |
|-----|--------|------|-------|---|
| 7 | LOFF8P | R/W | 0h | IN8P lead detachment Enable lead detachment detection on IN8P 0 : Disabled 1 : Enable |
| 6 | LOFF7P | R/W | 0h | IN7P lead detachment Enable lead detachment detection on IN7P 0 : Disabled 1 : Enable |
| 5 | LOFF6P | R/W | 0h | IN6P lead detachment Enable lead detachment detection on IN6P 0 : Disabled 1 : Enable |
| 4 | LOFF5P | R/W | 0h | IN5P lead detachment Enable lead detachment detection on IN5P 0 : Disabled 1 : Enable |
| 3 | LOFF4P | R/W | 0h | IN4P lead detachment Enable lead detachment detection on IN4P 0 : Disabled 1 : Enable |
| 2 | LOFF3P | R/W | 0h | IN3P lead detachment Enable lead detachment detection on IN3P 0 : Disabled 1 : Enable |
| 1 | LOFF2P | R/W | 0h | IN2P lead detachment Enable lead detachment detection on IN2P 0 : Disabled 1 : Enable |
| 0 | LOFF1P | R/W | 0h | IN1P lead detachment Enable lead detachment detection on IN1P 0 : Disabled 1 : Enable |

LOFF_SENSN: Negative signal lead detachment detection register (address = 10h) (reset = 00h)

This register selects the negative side of each channel (for lead detachment detection). See the Lead Detachment Detection section for details.

The LOFF_STATN register bits are only valid if the corresponding LOFF_SENSN bits are set to 1.

Register bits [5:4] are not applicable to DADS1294. Bits [7:6] are not applicable to DADS1294 and DADS1296.

Figure 83. LOFF_SENSN: Negative signal lead dropout detection register

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOFF8N | LOFF7N | LOFF6N | LOFF5N | LOFF4N | LOFF3N | LOFF2N | LOFF1N |
| R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 26. Description of the negative signal lead detachment detection field

| Bit | Fields | Type | Reset | Description |
|-----|---------|------|-------|---|
| 7 | LOFF8N | R/W | 0h | IN8N lead detachment Enable lead detachment detection on IN8N 0 : Disabled 1 : Enable |
| 6 | LOFF7PN | R/W | 0h | IN7N lead detachment Enable lead detachment detection on IN7N 0 : Disabled 1 : Enable |
| 5 | LOFF6N | R/W | 0h | IN6N lead detachment Enable lead detachment detection on IN6N 0 : Disabled 1 : Enable |
| 4 | LOFF5N | R/W | 0h | IN5N lead detachment Enable lead detachment detection on IN5N 0 : Disabled 1 : Enable |
| 3 | LOFF4N | R/W | 0h | IN4N lead detachment Enable lead detachment detection on IN4N 0 : Disabled 1 : Enable |
| 2 | LOFF3N | R/W | 0h | IN3N lead detachment Enable lead detachment detection on IN3N 0 : Disabled 1 : Enable |
| 1 | LOFF2N | R/W | 0h | IN2N lead detachment Enable lead detachment detection on IN2N 0 : Disabled 1 : Enable |
| 0 | LOFF1N | R/W | 0h | IN1N lead detachment Enable lead detachment detection on IN1N 0 : Disabled 1 : Enable |

LOFF_FLIP: Lead detachment toggle register (address = 11h) (reset = 00h)

This register controls the direction of the current derived from lead detachment. See the lead detachment detection section for more information.

Figure 84. LOFF_FLIP: Lead detachment toggle register

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOFF_FLIP8 | LOFF_FLIP7 | LOFF_FLIP6 | LOFF_FLIP5 | LOFF_FLIP4 | LOFF_FLIP3 | LOFF_FLIP2 | LOFF_FLIP1 |
| R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 27. Explanation of Lead Drop-Off Flip Register Fields

| Bit | Fields | Type | Reset | Description |
|-----|------------|------|-------|---|
| 7 | LOFF_FLIP8 | R/W | 0h | Channel 8 LOFF polarity reversal Reverse the upper pull-up/pull-down polarity of the current source or resistor on channel 8 (for lead-off output). 0 : No flip: IN8P dragged to AVDD, IN8N dragged to AVSS 1 : Flip: Drag IN8P to AVSS, drag IN8N to AVDD |
| 6 | LOFF_FLIP7 | R/W | 0h | Channel 7 LOFF polarity reversal Reverse the upper pull-up/pull-down polarity of the current source or resistor on channel 7 (for lead-off output). 0 : No flip: IN7P dragged to AVDD, IN7N dragged to AVSS 1 : Flip: Drag IN7P to AVSS, drag IN7N to AVDD |
| 5 | LOFF_FLIP6 | R/W | 0h | Channel 6 LOFF polarity reversal Reverse the upper pull-up/pull-down polarity of the current source or resistor on channel 6 (for lead-off output). 0 : No flip: IN6P pulled to AVDD, IN6N pulled to AVSS 1 : Flip: Drag IN6P to AVSS, drag IN6N to AVDD |
| 4 | LOFF_FLIP5 | R/W | 0h | Channel 5 LOFF polarity reversal Reverse the upper pull-up/pull-down polarity of the current source or resistor on channel 5 (for lead-off output). 0 : No flip: IN5P pulled to AVDD, IN5N pulled to AVSS 1 : Flip: Drag IN5P to AVSS, drag IN5N to AVDD |
| 3 | LOFF_FLIP4 | R/W | 0h | Channel 4 LOFF polarity reversal Reverse the upper pull-up/pull-down polarity of the current source or resistor on channel 4 (for lead-off output). 0 : No flip: IN4P pulled to AVDD, IN4N pulled to AVSS 1 : Flip: Drag IN4P to AVSS, drag IN4N to AVDD |
| 2 | LOFF_FLIP3 | R/W | 0h | Channel 3 LOFF polarity reversal Reverse the upper pull-up/pull-down polarity of the current source or resistor on channel 3 (for lead-off output). 0 : No flip: IN3P dragged to AVDD, IN3N dragged to AVSS 1 : Flip: Drag IN3P to AVSS, drag IN3N to AVDD |
| 1 | LOFF_FLIP2 | R/W | 0h | Channel 2 LOFF polarity reversal Reverse the upper pull-up/pull-down polarity of the current source or resistor on channel 2 (for lead-off output). 0 : No flip: IN2P pulled to AVDD, IN2N pulled to AVSS 1 : Flip: Move IN2P to AVSS, move IN2N to AVDD |
| 0 | LOFF_FLIP1 | R/W | 0h | Channel 1 LOFF polarity reversal Reverse the upper pull-up/pull-down polarity of the current source or resistor on channel 1 (for lead-off output). 0 : No flip: IN1P dragged to AVDD, IN1N dragged to AVSS 1 : Flip: Drag IN1P to AVSS, drag IN81N to AVDD |

LOFF_STATP: Lead-off positive signal status register (address = 12h) (reset = 00h)

This register stores the state of whether the positive electrode on each channel is on or off. See the lead detachment detection section for details. Ignore the LOFF_STATN values if the corresponding LOFF_SENSN bits are not set to 1.

When the LOFF_SENSEP bit is 0, the LOFF_STATP bit should be ignored.

Figure 85. LOFF_STATP: Lead detachment positive signal status register (read-only)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| IN8P_OFF | IN7P_OFF | IN6P_OFF | IN5P_OFF | IN4P_OFF | IN3P_OFF | IN2P_OFF | IN1P_OFF |
| R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 28. Explanation of Lead Disconnection Positive Signal Status Fields

| Bit | Fields | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | IN8P_OFF | R | 0h | Channel 8 Positive Channel Lead Dislodgement Status Regarding the state of IN8P electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 6 | IN7P_OFF | R | 0h | Channel 7 Positive Channel Lead Dislodgement Status Regarding the state of the IN7P electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 5 | IN6P_OFF | R | 0h | Channel 6 Positive Channel Lead Dislodgement Status Regarding the state of IN6P electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 4 | IN5P_OFF | R | 0h | Channel 5 Positive Channel Lead Dislodgement Status Regarding the state of IN5P electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 3 | IN4P_OFF | R | 0h | Channel 4 Positive Channel Lead Dislodgement Status Regarding the state of IN4P electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 2 | IN3P_OFF | R | 0h | Channel 3 Positive Channel Lead Dislodgement Status Regarding the state of the IN3P electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 1 | IN2P_OFF | R | 0h | Channel 2 Positive Channel Lead Dislodgement Status Regarding the state of the IN2P electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 0 | IN1P_OFF | R | 0h | Channel 1 Positive Channel Lead Disconnection Status Regarding the state of IN1P electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |

LOFF_STATN: Lead-off negative signal status register (address = 13h) (reset = 00h)

This register stores the state of whether the negative electrode on each channel is on or off. See the lead detachment detection section for details. Ignore the LOFF_STATN values if the corresponding LOFF_SENSN bits are not set to 1.

When the LOFF_SENSEN bit is 0, the LOFF_STATN bit should be ignored.

Figure 86. LOFF_STATN: Lead-off Negative Signal Status Register (Read-only)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| IN8N_OFF | IN7N_OFF | IN6N_OFF | IN5N_OFF | IN4N_OFF | IN3N_OFF | IN2N_OFF | IN1N_OFF |
| R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 29. Description of Lead-Off Negative Signal Status Fields

| Bit | Fields | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | IN8N_OFF | R | 0h | Channel 8 negative channel lead detachment status Regarding the state of the IN8N electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 6 | IN7N_OFF | R | 0h | Channel 7 negative channel lead detachment status Regarding the state of the IN7N electrode: whether it is on or off. 0 : Electrode open 1: Electrode off |
| 5 | IN6N_OFF | R | 0h | Channel 6 negative channel lead detachment status Regarding the state of the IN6N electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 4 | IN5N_OFF | R | 0h | Channel 5 negative channel lead detachment status Regarding the state of the IN5N electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 3 | IN4N_OFF | R | 0h | Channel 4 negative channel lead detachment status Regarding the state of the IN4N electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 2 | IN3N_OFF | R | 0h | Channel 3 negative channel lead detachment status Regarding the state of the IN3N electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 1 | IN2N_OFF | R | 0h | Channel 2 negative channel lead detachment status Regarding the state of the IN2N electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |
| 0 | IN1N_OFF | R | 0h | Channel 1 Negative Channel Lead Dislodgement Status Regarding the state of the IN1N electrode: whether it is on or off. 0 : Electrode open 1 : Electrode off |

GPIO: General Purpose I/O Register (Address = 14h) (Reset = 0Fh)

The general-purpose I/O register controls the operation of three GPIO pins. When RESP_CTRL[1:0] is in modes 01 and 11, GPIO2, GPIO3, and... GPIO4 pin is unavailable.

Figure 87. GPIO: General Purpose I/O Registers

| | | | | | | | |
|------------|---|---|---|------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GPIOD[4:1] | | | | GPIOC[4:1] | | | |
| R/W-0h | | | | R/W-Fh | | | |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 30. Description of General I/O Fields

| Bit | Fields | Type | Reset | Description |
|-----|------------|------|-------|---|
| 7:4 | GPIOD[4:1] | R/W | 0h | GPIO data These bits are used to read and write data to the GPIO ports. When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect. GPIO is not available in certain respiration modes. |
| 3:0 | GPIOC[4:1] | R/W | 0h | GPIO control (corresponding GPIOD) These bits determine whether the corresponding GPIOD pin is an input or an output. 0 = Output 1 = Input |

MISC1: Miscellaneous 1 register (address = 15h) (reset = 00h)

This register provides control over routing the SRB1 pin to all inverting inputs of the four, six, or eight channels (DADS1294/1296/1298).

Figure 88. MISC1: Miscellaneous 1 Register

| | | | | | | | |
|--------|--------|--------|----------|---|----------|---|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | SRB1 | SRB1_SEL | | SRB2_SEL | | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | | R/W-0h | | R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 31. Description of the fields in the pacemaker signal detection register

| Bit | Fields | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7:6 | Reserved | R/W | 0h | Reserved Always write 0h |
| 5 | SRB1 | R/W | 0h | Incentives, References, and Bias 1 This bit connects SRB1 to the inverting input of all channels. 0 = Switch on 1 = Switch off |
| 4:3 | SRB1_SEL | R/W | 0h | Even-numbered channel selection These bits control the selection of the channel driving SRB1. 00 = Select Channel 2 01 = Select channel 4 10 = Select Channel 6 11 = Select Channel 8 |
| 2:1 | SRB2_SEL | R/W | 0h | Odd-number channel selection These bits control the selection of the channel driving SRB2. 00 = Select Channel 1 01 = Select Channel 3 |

| | | | | |
|---|----------|-----|----|--|
| | | | | 10 = Select Channel 5 11 = Select Channel 7 |
| 0 | Reserved | R/W | 0h | Reserved |

CONFIG4: Configuration register 4 (address = 17h) (reset = 00h)
Figure 89. CONFIG4: Configuration Register 4

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|-------------|------------|------------------------------------|--------|
| 0 | 0 | 0 | 0 | SINGLE_SHOT | WCT_TO_RLD | $\overline{\text{PD_LOFF_COMP}}$ | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 32. Description of Fields in Configuration Register 4

| Bit | Fields | Type | Reset | Description |
|-----|------------------------------------|------|-------|---|
| 7:4 | Reserved | R/W | 0h | Reserved |
| 3 | SINGLE_SHOT | R/W | 0h | Single-stroke conversion This bit sets the conversion mode. 0 = Continuous switching mode 1 = Single-stroke mode |
| 2 | WCT_TO_RLD | R/W | 0h | Connect WCT to RLD This bit connects WCT to RLD. 0 = Connection from WCT to RLD closed 1 = WCT to RLD connection enabled |
| 1 | $\overline{\text{PD_LOFF_COMP}}$ | R/W | 0h | Lead detachment and comparator power failure This bit de-energizes the comparator when the lead is disconnected. 0 = Disable lead-drop comparator 1 = Enable lead-drop comparator |
| 0 | Reserved | R/W | 0h | Reserved Always write 0h |

WCT1: Wilson Center Terminal and Enhanced Lead Control Register (Address = 18h) (Reset = 00h)

The WCT1 control register configures the WCT circuit channel selection and enhancement leads.

Figure 90. WCT1: Wilson center terminal and enhanced lead control register

| | | | | | | | |
|---------|---------|---------|---------|---------|-----------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| aVF_CH6 | aVL_CH5 | aVR_CH7 | aVR_CH4 | PD_WCTA | WCTA[2:0] | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 33. Description of Fields in Configuration Register 4

| Bit | Fields | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7 | aVF_CH6 | R/W | 0h | Make $(WCTA + WCTB)/2$ the negative input of channel 6 (DADS1296, DADS1298). 0 = Disabled 1 = Enabled |
| 6 | aVL_CH5 | R/W | 0h | Make $(WCTA + WCTC)/2$ the negative input of channel 5 (DADS1296, DADS1298). 0 = Disabled 1 = Enabled |
| 5 | aVR_CH7 | R/W | 0h | Make $(WCTB + WCTC)/2$ the negative input of channel 7 (DADS1298). 0 = Disabled 1 = Enabled |
| 4 | aVR_CH4 | R/W | 0h | Make $(WCTB + WCTC)/2$ the negative input of channel 4. 0 = Disabled 1 = Enabled |
| 3 | PD_WCTA | R/W | 0h | Power off WCTA 0 = Power outage 1 = Power on |
| 2:0 | WCTA[2:0] | R/W | 0h | The WCT amplifier A channel selector is typically connected to the RA electrode. These are one of the eight electrode inputs for the bit selection channels 1 through 4. 000 = Channel 1 positive input connected to WCTA amplifier 001 = Channel 1 negative input connected to WCTA amplifier 010 = Channel 2 positive input connected to WCTA amplifier 011 = Channel 2 negative input connected to WCTA amplifier 100 = Channel 3 positive input connected to WCTA amplifier 101 = Channel 3 negative input connected to WCTA amplifier 110 = Channel 4 positive input connected to WCTA amplifier 111 = Channel 4 negative input connected to WCTA amplifier |

WCT2: Wilson Center Terminal and Enhanced Lead Control Register (Address = 19h) (Reset = 00h)

The WCT2 control register configures the WCT circuit channel selection.

Figure 91. WCT2: Wilson Center Terminal Control Register

| | | | | | | | |
|---------|---------|-----------|---|---|-----------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PD_WCTC | PD_WCTB | WCTB[2:0] | | | WCTC[2:0] | | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | | |

Legend: R/W = Read/Write; R = Read Only; -n = Reset value

Table 34. Description of Wilson Center Terminal Control Fields

| Bit | Fields | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7 | PD_WCTC | R/W | 0h | Power off WCTC 0 = Power outage 1 = Power on |
| 6 | PD_WCTB | R/W | 0h | Power off WCTB 0 = Power outage 1 = Power on |
| 5:3 | WCTB[2:0] | R/W | 0h | The WCT amplifier B channel selector is typically connected to the LA electrode. These are one of the eight electrode inputs for the bit selection channels 1 through 4. 000 = Channel 1 positive input connected to WCTB amplifier 001 = Channel 1 negative input connected to WCTB amplifier 010 = Channel 2 positive input connected to WCTB amplifier 011 = Channel 2 negative input connected to WCTB amplifier 100 = Channel 3 positive input connected to WCTB amplifier 101 = Channel 3 negative input connected to WCTB amplifier 110 = Channel 4 positive input connected to WCTB amplifier 111 = Channel 4 negative input connected to WCTB amplifier |
| 2:0 | WCTC[2:0] | R/W | 0h | The WCT amplifier B channel selector is typically connected to the LA electrode. These are one of the eight electrode inputs for the bit selection channels 1 through 4. 000 = Channel 1 positive input connected to WCTB amplifier 001 = Channel 1 negative input connected to WCTB amplifier 010 = Channel 2 positive input connected to WCTB amplifier 011 = Channel 2 negative input connected to WCTB amplifier 100 = Channel 3 positive input connected to WCTB amplifier 101 = Channel 3 negative input connected to WCTB amplifier 110 = Channel 4 positive input connected to WCTB amplifier 111 = Channel 4 negative input connected to WCTB amplifier |

Application Information

The DADS129x measures the full differential signal, where the common-mode voltage point is the midpoint of the positive and negative analog inputs. Due to the margin required for operation, the internal PGA limits the common-mode input range. Human bodies are prone to common-mode drift because, similar to antennas, noise can easily couple onto the body. These common-mode drifts may push the input common-mode voltage of the DADS129x out of the measurable range of the ADC.

If the system uses patient-driven electrodes, the DADS129x includes an on-chip right-leg drive (RLD) amplifier connected to the patient-driven electrodes. The RLD amplifier function is to bias the patient to maintain the common-mode voltage of other electrodes within an effective range. After power-on, the amplifier uses the analog intermediate power supply voltage or the voltage on the RLDREF pin as the reference input to stabilize an output close to that voltage.

The DADS129x provides an option of using the input electrode voltage as feedback for the amplifier, by setting the corresponding bits in the RLD_SENSP and RLD_SENSN registers, to more effectively stabilize to the output of the amplifier's reference voltage. For examples of three-electrode systems using this technology, please refer to Figure 94.

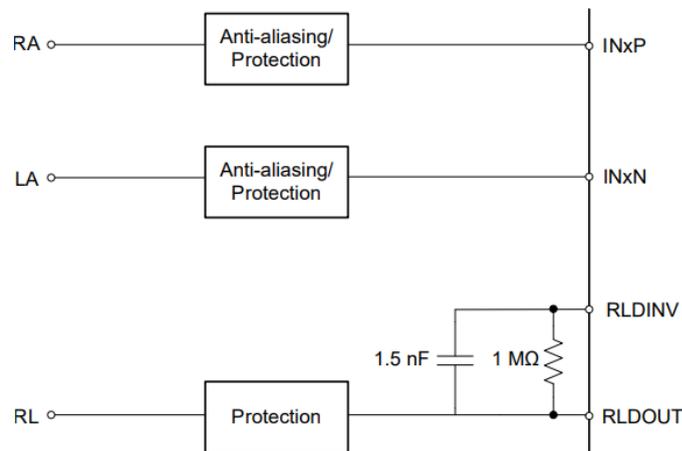


Figure 94. Setting common mode using RLD electrodes

The second strategy for maintaining an effective common-mode voltage is to perform AC coupling on the analog input, which is particularly useful when patient-driven electrodes are not used. The voltage divider or pull-up resistor between the DC-blocking capacitor and the analog power supply, combined with the RLD amplifier on the DADS129x, can set the DC bias at a known point, effectively ensuring that the DC common-mode voltage does not drift. Applications that do not use patient-driven electrodes can still use the RLD amplifier on the DADS129x as a buffered intermediate power supply voltage to bias the input. Be careful when selecting passive components, as capacitors and resistors form an RC high-pass filter. If the passive components are not selected correctly, the filter will cause the frequency at the lower end of the signal bandwidth to decay undesirably. Figure 95 shows an example of this configuration.

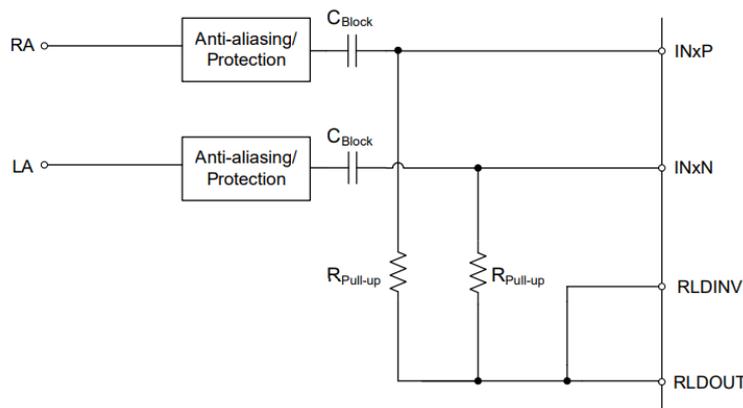


Figure 95. Setting the common mode without using RLD electrodes

Anti-Aliasing

Like all analog-to-digital systems, it is important to prevent accidental aliasing effects. The DADS129x modulator samples the input at a frequency of 256kHz or 512kHz, depending on whether the device is in low-power (LP) mode or high-resolution (HR) mode. Just like in the case of all digital filters, the on-chip digital decimation filter on the DADS129x repeats its response at integer multiples of the modulator frequency.

The advantage of the Δ - Σ architecture is that the digital decimation filter significantly attenuates the frequency between the signal band of the modulator frequency and the aliased signal band. This attenuation, combined with the limited bandwidth of the PGA (please refer to Table 5), makes the steepness requirement for the analog anti-aliasing filter response less strict.

In many cases, the acceptable attenuation of the modulator frequency is provided by a single-pole or double-pole RC low-pass filter.

When choosing anti-aliasing components, be careful as well. Due to component mismatch (including anti-aliasing components), the conversion from common mode to differential mode can lead to a decrease in common mode suppression performance.

Figure 96 shows a typical front-end configuration.

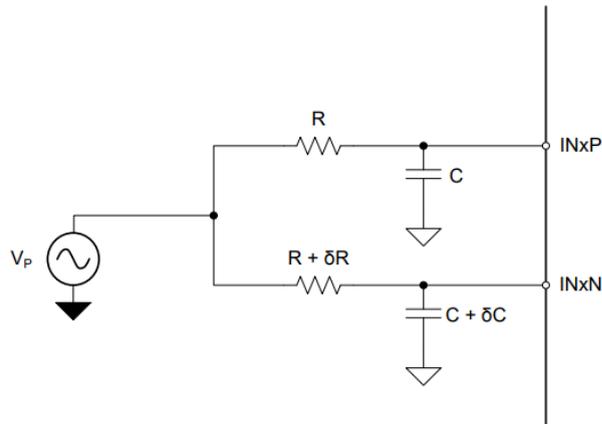


Figure 96. Typical front-end configuration

V_P represents the common-mode signal of the system. If the values of R and C modeled in the differential signal are exactly the same, the system exhibits a very high CMR. If the δR and δC in the resistors R and capacitors C are not matched respectively, the CMR of the entire system is approximately equal to Equation 8.

$$\text{CMR} = 20 \log \left(\frac{\delta R}{R} + \frac{\delta C}{C} \right) + 20 \log \left(\frac{f}{f_c} \right)$$

where

- f_c is the -3 -dB frequency of the RC filter. (8)

If 1% precision external components are used and the bandwidth of the RC filter is approximately 6kHz, then the system has only 74dB of CMR at 60Hz. In the real world, the front end of ECG not only includes a first-order RC filter, but also electrodes, cables, and second-order or third-order RC filters. Considering all these components, mismatches can easily accumulate and thus contribute up to 20% or more of the signal.

At a frequency of 60Hz, this degree of mismatch will cause the system's CMR to drop below 60dB. Therefore, different techniques must be considered to improve CMR. There is a trade-off in choosing the bandwidth of the anti-aliasing filter placed in front of the modulator. Considering the mismatches between discrete components, it is best to choose a larger bandwidth; the upper limit of the bandwidth is determined by the sampling frequency of the modulator.

Power Supply Recommendations

The DADS129x has three power supplies: AVDD, AVDD1 and DVDD. To achieve the best performance, the noise of AVDD and AVDD1 must be as low as possible. AVDD1 supplies power to the charge pump module and has a transient with a frequency of f_{CLK} . Therefore,

DADS1294/1296/1298 Low-Power, 4/6/8-Channel, Low-Noise, 24-Bit ADC for Physiological Signal Measurement

AVDD1 and AVSS1 should be connected to AVDD and AVSS in a star configuration. Eliminating the noise from AVDD and AVDD1 (which are out of sync with the operation of DADS129x) is very important. Use 1 μ F and 0.1 μ F solid-state ceramic capacitors as bypass capacitors for each DADS129x power supply. To achieve the best performance, place digital circuits (DSP, microcontrollers, FPGA, etc.) in the system so that the return current on these devices does not pass through the analog return path of DADS129x. Use single-pole or bipolar power supplies to power DADS129x. Use surface mount, low-cost, thin, multi-layer ceramic type capacitors for decoupling. In most cases, the VCAP1 capacitor is also multi-layer ceramic; however, in systems where the circuit board is subjected to high-frequency or low-frequency vibrations, non-ferroelectric capacitors such as tantalum capacitors or Class 1 capacitors (C0G or NPO) should be installed.

EIA 2 and 3 class dielectrics (such as X7R, X5R, X8R, etc.) are ferroelectric types. The piezoelectric properties of these capacitors can manifest as electrical noise from the capacitor. When using an internal reference, the noise at the VCAP1 node can lead to performance degradation.

Power-On Sequencing

Before powering on the device, all digital and analog inputs must be at a low level. When powering on, keep all these signals at a low level until the power supply stabilizes, as shown in Figure 105.

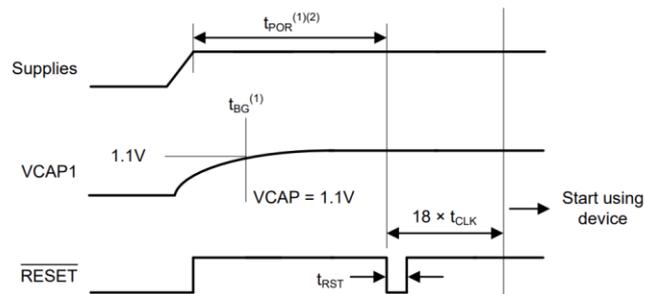
Allow time for the power voltage to reach its final value, then start providing the main clock signal to the CLK pin. Wait for the time t_{POR} , then use the RESET pin or the RESET command to send a reset pulse to initialize the digital part of the chip. Issue the reset command after t_{POR} or when the VCAP1 voltage is greater than 1.1V (depending on the longer time).

Note:

- Table 38 describes t_{POR} .
- The charging time of the VCAP1 pin is set by the RC time constant; see Figure 31.

After releasing the RESET pin, program the configuration register; for details, see the CONFIG1: Configuration Register 1 (Address = 01h) (Reset = 06h) section.

Table 38 shows the power-on sequence timing.



- (1) Timing to reset pulse is t_{POR} or after t_{BG} , whichever is longer.
- (2) When using an external clock, t_{POR} timing does not start until CLK is valid.

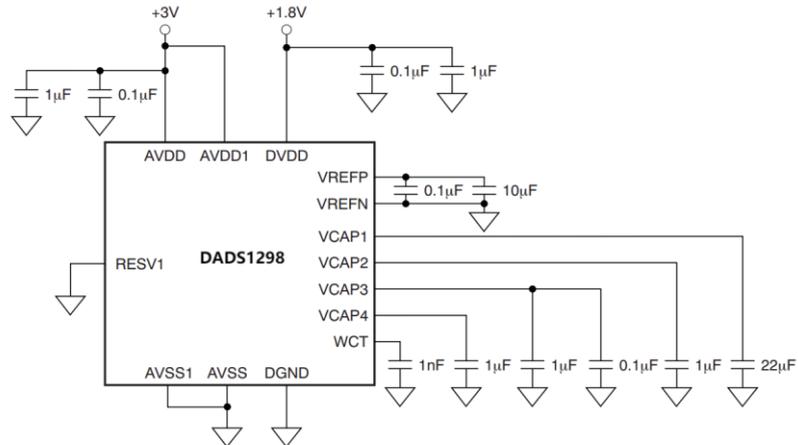
Figure 105. Power-on timing diagram

Table 38. Timing requirements of Figure 105

| | | Min | Max | Unit |
|-----------|---------------------------------|----------|-----|-----------|
| t_{POR} | Wait after power up until reset | 2^{18} | | t_{CLK} |
| t_{RST} | Reset low duration | 2 | | t_{CLK} |

Connect to a single-pole (3V or 1.8V) power supply

Figure 106 illustrates the DADS129x connected to a single-pole power supply. In this example, the analog power supply (AVDD) is referenced to the analog ground (AVSS), and the digital power supply (DVDD) is referenced to the digital ground (DGND).

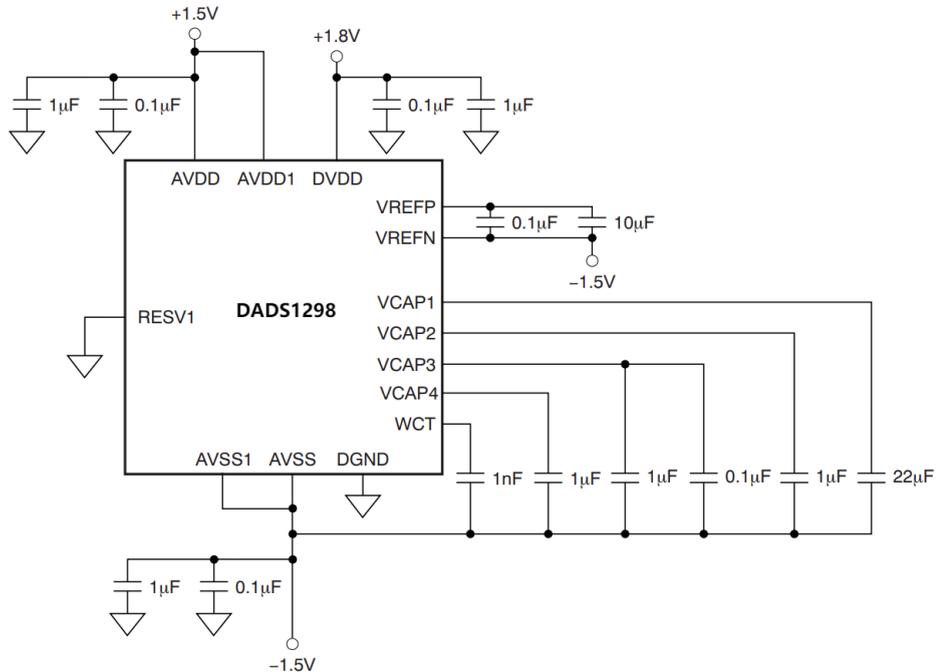


NOTE: Place the capacitors for supply, reference, WCT, and VCAP1 to VCAP4 as close to the package as possible.

Figure 106. Single power supply

Connect to a bipolar ($\pm 1.5V$ or $\pm 1.8V$) power supply.

Figure 107 illustrates the DADS129x connected to a bipolar supply. In this example, the analog supplies connect to the device analog supply (AVDD). This supply is referenced to the device analog return (AVSS), and the digital supply (DVDD) is referenced to the device digital ground return (DGND).



NOTE: Place the capacitors for supply, reference, WCT, and VCAP1 to VCAP4 as close to the package as possible.

Figure 107. Bipolar power supply

Layout Guide

For grounding, use a low-impedance connection to allow the returning current to flow back to its respective source without interference. To achieve the best performance, dedicate a complete PCB layer to the grounding plane, and do not route any other signal traces on this layer. Keep the connection to the grounding plane as short and straight as possible. When using through-hole connections to the grounding layer, use multiple parallel through-holes to reduce the grounding impedance.

The mixed-signal layout sometimes includes separate analog and digital ground planes connected together in one location; however, when the analog, digital, and power components are properly placed, separate ground planes are not necessary. Properly placing components can divide the analog, digital, and power circuits into different PCB areas to prevent digital return current from coupling to sensitive analog circuits. If grounding plane separation is required, connect at the ADC. Connecting each grounding layer at multiple locations creates grounding loops, so this is not recommended. A single grounding plane for analog and digital can avoid grounding loops. Use low ESR ceramic capacitors to bypass power pins. Short and straight traces must be used to place the bypass capacitors as close as possible to the power pins. For optimal performance, the grounding side of the bypass capacitor must also be a low-impedance connection. Power current should flow through the bypass capacitor pin first and then to the power pin, making the bypass most effective (also known as Kelvin connection). If multiple ADCs are located on the same PCB, use a wide power trace or a dedicated power plane to minimize the possibility of crosstalk between ADCs.

If external filtering is used for analog input, use C0G type ceramic capacitors as much as possible. C0G capacitors have stable characteristics and low noise. Ideally, route differential signals into multiple pairs to minimize the loop area between traces. Route digital circuit traces (such as clock signals) away from all analog pins. Note that the internal reference output loop shares the same pins as the AVSS power supply. To minimize coupling between power traces and reference loop traces, route two traces separately; ideally, use a star connection at the AVSS pin. Short and straight interconnections must be made between analog input lines and avoid stray distributed capacitance, especially between the analog input pin and AVSS. These analog input pins have high impedance and are very sensitive to external noise. Consider the AVSS pin as a sensitive analog signal and directly connect it to the power ground through appropriate shielding.

If no shielding is implemented, leakage current between PCB traces may exceed the input bias current of DADS129x. Try to keep digital signals away from analog input signals on the PCB.

The SCLK input of the serial interface should have no noise and interference, which is very important. Even with a relatively slow SCLK frequency, short digital signal rise and fall times may cause excessive ringing and noise.

For optimal performance, use termination resistors as needed to keep digital signal traces short and ensure that all digital signals are routed directly above the grounding plane, using the minimum through-hole connections.

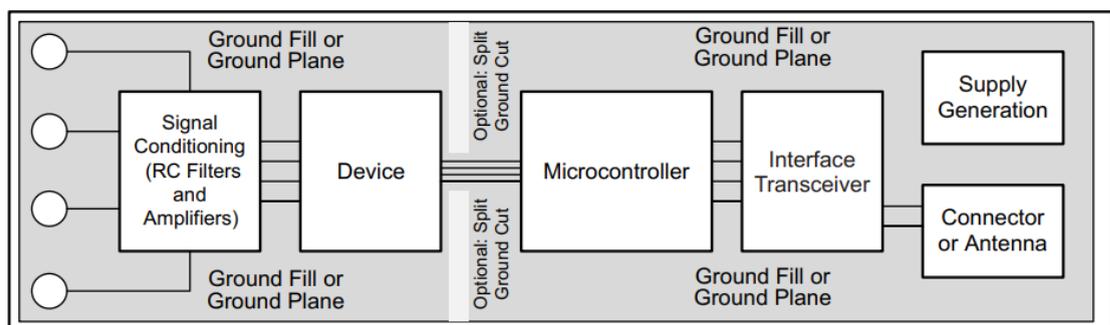


Figure 108. System Component Placement

Layout Example

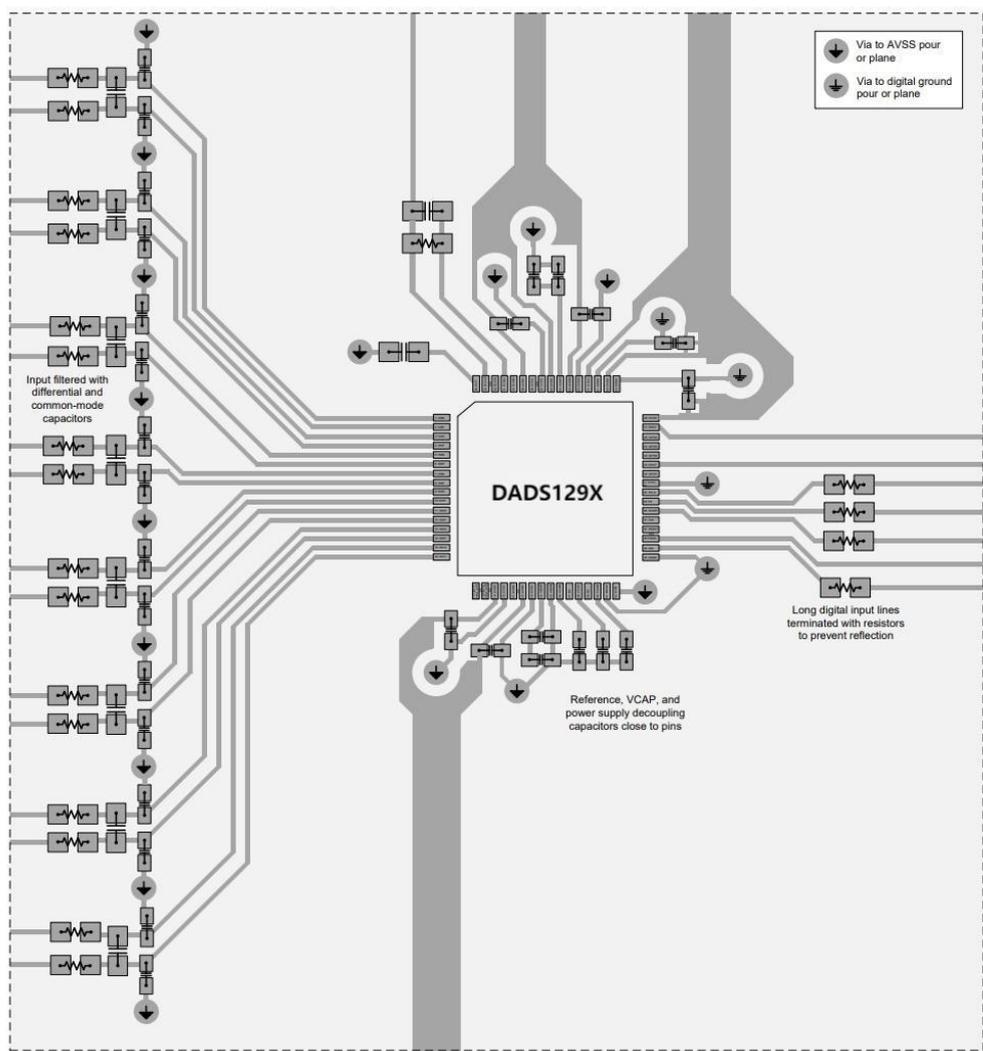
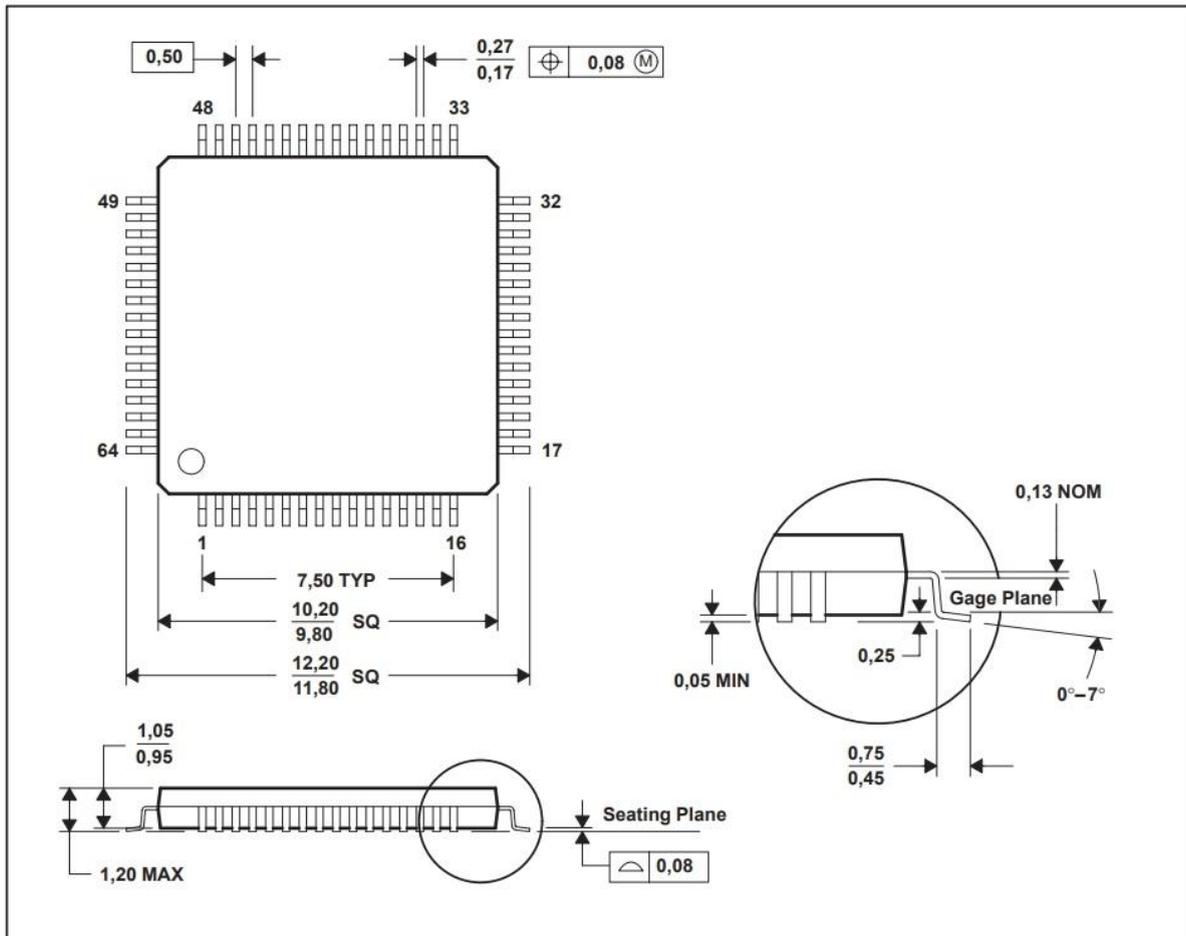


Figure 109. DADS129x layout example

Package Size

PAG (S-PQFP-G64)
PLASTIC QUAD FLATPACK


Device Ordering Information List

| Product Model | Temperature Range | Package Type | Packaging Quantity | RoHS |
|---------------|-------------------|--------------|--------------------|------|
| DADS1294 | -40 °C to +85 °C | 64-TQFP | 168/tray | Y |
| DADS1296 | -40 °C to +85 °C | 64-TQFP | 168/tray | Y |
| DADS1298 | -40 °C to +85 °C | 64-TQFP | 168/tray | Y |