DADS1292 Dual-Channel, 24-Bit, Low-Noise, Synchronous Sampling ADC

1. Characteristics

- Two low-noise programmable gain amplifiers (PGAs) and two high-resolution synchronous sampling analog-to-digital converters (ADCs).
- Input reference noise: 1.2 uVpp (bandwidth 70Hz)
- Input bias current: 300pA
- Data rate: 250 ~ 16000 samples per second (SPS)
- Common-mode rejection ratio (CMRR): -120dB
- Programmable gain: 1, 2, 4, 6, 8, 12 or 24
- Single-pole or bipolar power supply:
  - Analog: 4.75V to 5.25V
  - Digital: 1.8V to 3.6V
- Built-in human bio-electrical signal measurement functions:
  - Human body bias amplifier
  - Lead-Off Detection
  - Internal test signal
- Built-in oscillator is optional
- Built-in benchmark selectable
- Flexible power-saving and standby modes
- SPI interface
- Operating temperature: -40°C to +85°C

2. Applications

- Medical devices for measuring human bioelectrical signals:
  - ✧ Electroencephalography (EEG) research
  - ✧ Fetal ECG monitoring
  - ✧ Sleep research monitoring
  - ✧ Bispectral Index (BIS)
  - ✧ Evoked audio potential (EAP)

3. Overview

The DADS1292 is a 2- channel, low-noise, 24-bit synchronous sampling ΔΣ analog-to-digital converter (ADC). It integrates a programmable gain amplifier (PGA), an internal reference, and a clock oscillator. The DADS1292 provides the functionality required for extracranial electroencephalography (EEG) and electrocardiography (ECG) applications. With its high integration and excellent performance, the DADS1292 enables users to build wearable brain-computer interface systems in a significantly reduced size. The DADS1292 features a flexible input multiplexer in each channel. This multiplexer can be independently connected to the internally generated signal to perform tests, temperature, and lead disconnection detection. Furthermore, any configuration of the input channel can be selected to generate a human bias output signal. Optional SRB 1/2 pins are also provided , which can be used as the other end (N/P) input for single-ended (P/N) sampling. Channel 1 can be configured for respiratory detection mode if needed. The DADS1292 operates at data transfer rates from 250 SPS to 16 kSPS. Lead-off detection can be achieved internally via an excitation current source. Multiple DADS1292 devices can be daisy-chained in multi-channel systems. The DADS1292 is packaged in a QFN32 (5mm x 5mm) package.

4. Device Packaging Information

Product Model	Packaging	Package size
DADS1292	Q FN32	5.0mm × 5.0mm

5. Functional Block Diagram

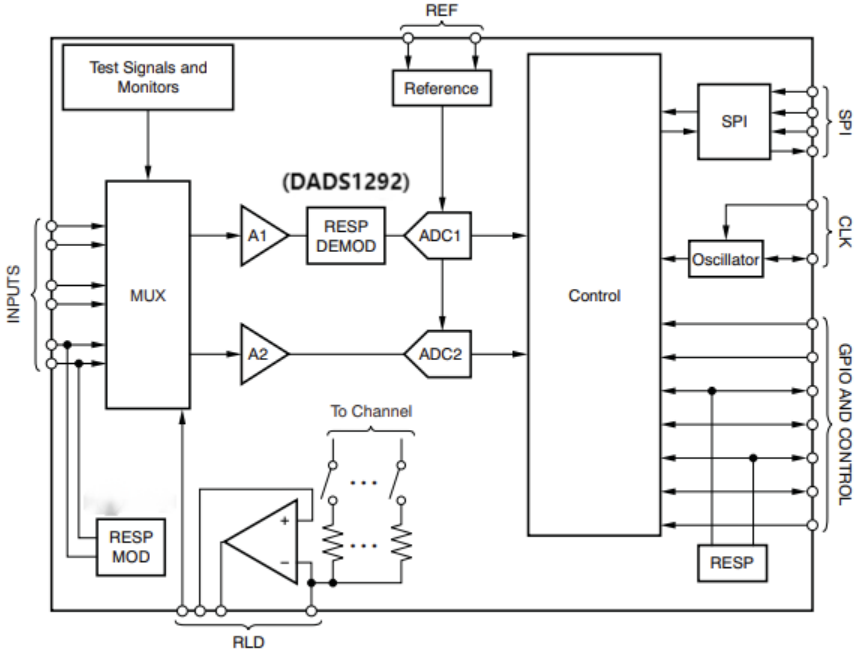

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Figure 1. Functional Block Diagram

6. Specifications

- **Absolute Maximum Ratings**

		Min	Max	Unit
Voltage	AVDD to AVSS	-0.3	5.5	V
	DVDD to DGND	-0.3	3.9	
	AVSS to DGND	-3	0.2	
	VREFP to AVSS	-0.3	AVDD + 0.3	
	VREFN to AVSS	-0.3	AVDD + 0.3	
	Analog Input	AVSS - 0.3	AVDD + 0.3	
	Numeric input	DGND - 0.3	DVDD + 0.3	
Current	Input current to any pin other than the power supply pin	-10	10	mA
Temperature	Maximum junction temperature (T_J)		150	°C
	Storage temperature (T_{stg})	-60	150	

- **ESD Ratings**

		Value	Unit
V(ESD) electrostatic discharge	Human Model (HBM)	±2,000	V
	Model of live equipment (CDM) according to JEDEC specification JESD22-C101	±500	

- **Recommended working conditions**

		Min	Typ	Max	Unit
Power supply range					
Analogd power supply	AVDD to AVSS	4.75	5	5.25	V
Digital power supply	DVDD to DGND	1.8	3.3	3.6	V
Analog -to- digital voltage differential	AVDD to DVDD	-2.1		3.6	V
Analog signal input range					
Full-amplitude differential input voltage	V_{INxP} - V_{INxN}		±V_{REF} / gain		V
V_{CM} Input signal common-mode voltage range	(V_{INxP} + V_{INxN}) / 2	Refer to the Analog Input Signals section for description			V
Reference voltage input range					
V_{REF} Reference input voltage	V_{REF} = (V_{VREFP} - V_{VREFN})		4.5		V
VREFN negative input			AVSS		V
VREFP Positive Input			AVSS + 4.5		V
Clock input					
f_{CLK} External clock input frequency	CLKSEL pin = 0	1.5	2.048	2.25	MHz
Digital input					
Input voltage range		DGND - 0.1		DVDD + 0.1	V
Temperature range					
T_A Operating temperature range		-40		85	°C

- **Thermal performance parameters**

Symbol	Name	Value	Unit
$R_{\theta JA}$	Connection with ambient thermal resistance	46.2	°C/W
$R_{\theta JC(top)}$	Thermal resistance connected to the housing (top)	5.8	
$R_{\theta JC(bot)}$	Thermal resistance connected to the housing (bottom)	--	
$R_{\theta JB}$	Connecting plate thermal resistance	19.6	

ψ_{JT}	Connection top feature parameters	0.2	
ψ_{JB}	Connecting plate characteristic parameters	19.2	

8. Electrical Characteristics

Unless otherwise specified, typical conditions are T_A = 25°C, and maximum and minimum values apply to T_A = -40°C to 85°C. Unless otherwise specified, all electrical parameters are measured under the following conditions: AVDD-AVSS = 5V, DVDD = 3.3V, V_{REF} = 4.6V, using an external clock of f_{CLK} = 2.048MHz, sampling rate = 250SPS, and gain = 12.

Parameter	Test conditions	Min	Typ	Max	Unit
Analog Input					
Input capacitor			20		pF
Input bias current	T_A = 25°CINxP =INxN=2.5V			±300	pA
	T_A = -40°C ~ + 85°CINxP = INxN = 2.5V		±300		
DC input resistance	Not enabled lead-off	1,000			MΩ
	$I_{LEADOFF}$ = 6nA		500		
PGA performance					
Gain settings					
Bandwidth					
ADC performance					
Resolution					
Sampling rate					
Common-mode input voltage					
Common-mode input voltage					
ADC DC performance					
Equivalent input noise (0.01Hz ~ 70Hz)	1000 points, 4 seconds of data, gain=24, T_A = 25°C, input short circuit		1.2		uVpp
Integral nonlinearity	V_{IN} = -3dBFs, gain = 12		14		ppm
Offset error	gain=12, 250SPS		14		uV
Offset error temperature drift			80		nV/°C
Gain error	gain=12 , 250SPS		1.5		% of FS
Gain temperature drift			3		ppm/°C
Inter-channel Gain Matching Degree			0.2		% of FS
ADC AC performance					
Common-mode rejection ratio	f_{CM} = 50Hz and 60Hz		-120		dB
PSRR	f_{PS} = 50Hz and 60Hz		112		dB
Crosstalk	f_{IN} =50Hz and 60Hz, gain=12		-110		dB
SNR	V_{IN} =-6dBFs, f_{IN} =10Hz, gain=12		113		dB
THD	V_{IN} =-6dBFs, f_{IN} =60Hz, gain=12		-98		dB
Human body BIAS amplifier					
Noise	BW=150Hz		2		uVrms
Gain-bandwidth product	50-kΩ || 10-pF load, gain=1		100		KHz
Slew rate	50-kΩ || 10-pF load, gain=1		0.07		V/us
THD	f_{IN} = 10Hz, gain = 1		-80		dB
Output short-circuit current			1.1		mA
Static power consumption			20		uA
Electrode drop detection					
AC detection selectable frequency	Continuous detection		fDR/4		Hz
	Periodic detection		DR/4, 7.8, 31.2		
Constant current source current	ILEAD_OFF[1:0]=00		10		nA
	ILEAD_OFF[1:0]=01		40		
	ILEAD_OFF[1:0]=10		8.5		uA
	ILEAD_OFF[1:0]=11		34		
Constant current source accuracy			20%		
Comparator threshold accuracy			±30		mV

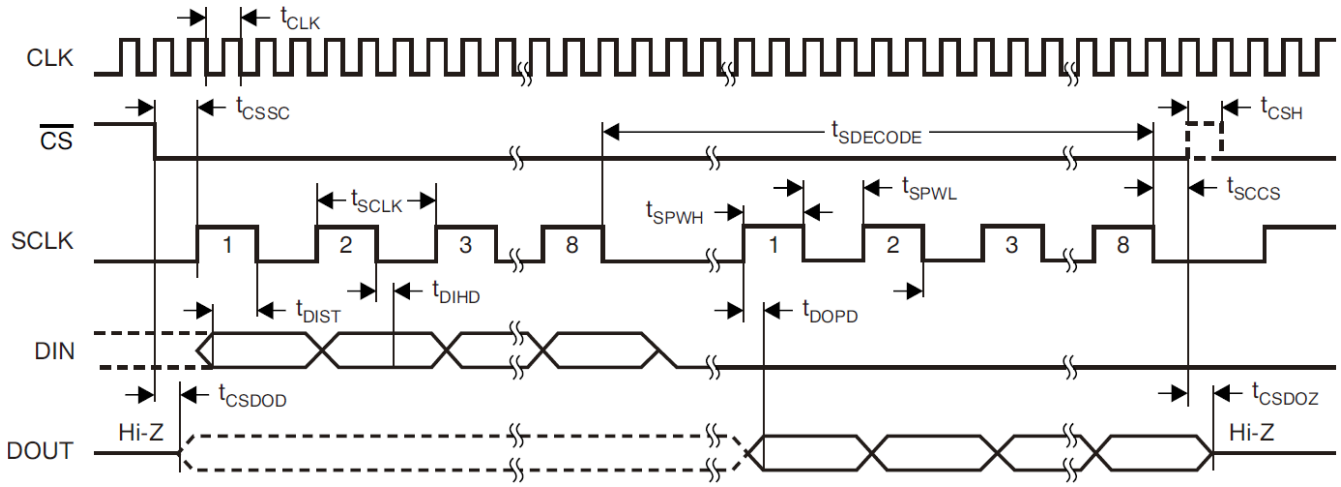
9. Electrical Characteristics (continued)

Parameter		Test conditions	Min	Typ	Max	Unit
External reference						
Input resistance				6.9k		Ω
Internal benchmark						
Internal reference voltage				4.6		V
V_{REF} accuracy				±0.4%		
V_{REF} Temperature Drift		T_A = -40°C ~ +85°C		35		ppm/°C
V_{REF} startup time				2 5		ms
System monitoring						
Power supply measure error	Analog power supply measurement			2%		
	Digital power supply measurement			2%		
Device wake-up		From power-up to DRDY low		150		ms
		STANDBY mode		31.25		µs
Temperature measurement	Voltage	T_A = 25°C		145		mV
	Conversion factor			490		uV/°C
Test signal	frequency			$f_{CLK}/2^{21}$, $f_{CLK}/2^{20}$		Hz
	Voltage			1*V_{REF}/2400 2*V_{REF}/2400		V
	voltage accuracy			±2%		
clock						
Internal clock frequency		Typical value		2.048M		Hz
Internal clock accuracy		TA=25°C			0.5%	
		TA = -40°C ~ +85°C			2.5%	
Internal clock startup time				20		us
Internal clock power consumption				1 20		uW
Digital signal levels (DVDD = 1.8V to 3.3V)						
High-level input			0.8*DVDD		DVDD+0.1	V
low-level input			-0.1		0.2*DVDD	
High-level output			0.9*DVDD			V
Low-level output					0.1*DVDD	V
Input current			-10		1 0	uA
Power consumption (AVDD-AVSS=5V, DVDD=3.3V)						
AVDD current		Internal reference enabled, 5V, HDR_EN=0		2.3		mA
AVDD current		Internal reference enabled, 5V, HDR_EN=1		3.0		mA
DVDD current		Normal mode, DVDD=3.3V		0.7		mA
Power consumption		Normal mode (with HDR_EN=0 set)		13.8		mW
		Normal mode (with HDR_EN=1 set)		17.3		mW
		Standby mode, internal reference enabled		3.63		mW
		P WDN_=0 Mode		14		uW

10. Serial Communication Timing

Unless otherwise specified, T_A = 25℃.

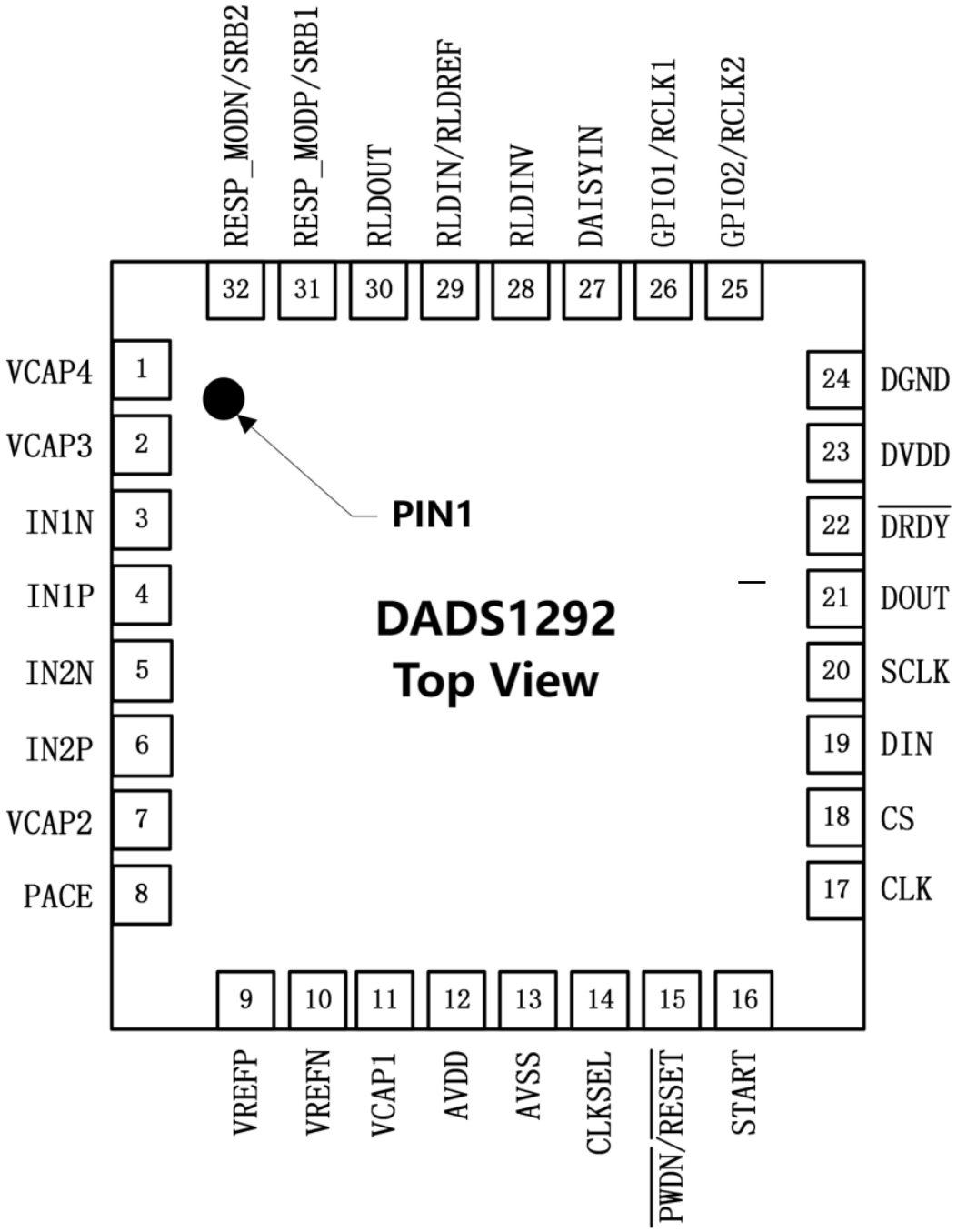
Symbol	Parameter	2.7V≤DVDD≤3.6V		1.65V≤DVDD≤2V		Unit
		Min	Max	Min	Max	
t_{CLK}	Master clock cycle	414	514	414	514	ns
t_{CSSC}	$\overline{CS}$ low level until the first SCLK, set time	6		17		ns
t_{SCLK}	SCLK cycle	50		66.6		ns
$t_{SPWH,L}$	SCLK pulse width, high level and low level	15		25		ns
t_{DIST}	DIN valid to SCLK falling edge: Setup time	10		10		ns
t_{DIHD}	IN after the falling edge of SCLK: Hold time	10		11		ns
t_{CSH}	$\overline{CS}$ high-level pulse	2		2		t_{CLK}
t_{SCCS}	The eighth falling edge of S CLK leads to the high level of $\overline{CS}$	4		4		t_{CLK}
$t_{SDECODE}$	Command decoding time	4		4		t_{CLK}
$t_{DISCK2ST}$	DAISY_IN valid until SCLK rising edge: Setup time	10		10		ns
$t_{DISCK2HT}$	DAISY_IN is valid after the rising edge of SCLK: Hold time	10		10		ns
t_{DOHD}	DAISY_IN is valid after the rising edge of SCLK: Hold time	10		10		ns
t_{DOPD}	SCLK rises to DOUT valid: Setup time		17		32	ns
t_{CSDOD}	$\overline{CS}$ low level to DOUT drive	10		20		ns
t_{CSDOZ}	$\overline{CS}$ high level to DOUT Hi-Z		10		20	ns



Note: SPI is set to CPOL=0 and CPHA=1.

Figure 2. Serial Communication Timing Diagram

11. Pin Configuration and Pin Functions



Pin Functions

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	VCAP4	Analog capacitor pin; connect a 1μF capacitor to AVSS	17	CLK	Master clock input
2	VCAP3	Analog capacitor pin; connects a parallel combination of 1μF and 0.1μF capacitors to the AVSS	18	$\overline{CS}$ or CS_	SPI chip select, active low
3	IN1N	1- channel differential analog negative input N	19	DIN	SPI serial data input
4	IN1P	1- channel differential analog positive input P	20	SCLK	SPI serial clock input
5	IN2N	2- channel differential analog negative input N	21	DOUT	SPI serial data output
6	IN2P	2- channel differential analog positive input P	22	$\overline{DRDY}$ or DRDY_	Data ready, active low
7	VCAP2	Analog capacitor pin; connect a 1μF capacitor to AVSS	23	DVDD	Digital power supply. Connect a 1 μF capacitor to DGND
8	PACE	Pacemaker signal detection analog output	24	DGND	Digital
9	VREFP	Positive analog reference voltage; connect a minimum 10μF capacitor to VREFN	25	GPIO2	General Purpose Input/Output Pin 2
10	VREFN	Negative analog reference voltage	26	GPIO1	General Purpose Input / Output Pin 1
11	VCAP1	Analog capacitor pin; connect a 10μF capacitor to AVSS	27	DAISYIN	Daisy chain input
12	AVDD	Analog power supply; connect a 1μF capacitor to the AVSS	28	BIASINV or RLDINV	Human body bias or right leg drive op amplifier inverting input
13	AVSS	Analog ground	29	BIASIN/BIASREF or RLDIN/RLDRE	Human body bias or right leg drive reference input
14	CLKSEL	Internal or external master clock selection	30	BIASOUT or RLDOUT	Human body bias or right leg drive op amplifier output
15	$\overline{RESET}$ / $\overline{PWDN}$ Or RESET _ /PWDN _	System reset, active low	31	RESP_MODEP/SRB 1	Reference and bias signal 1 or respiratory modulation signal P
16	START	Synchronization signal for starting or restarting the conversion	32	RESP_MODEN/SRB2	Reference and bias signal 2 or respiratory modulation signal N

12. Noise Measurement

There are two methods to optimize the noise performance of the DADS1292 : using a low sampling rate can reduce the noise of the ADC , and increasing the gain of the PGA can improve the system's input equivalent noise. The table below lists the input equivalent noise obtained at different sampling rates and gain values when the input is shorted, internally shorted to (VREFP+ VREFN)/2 or externally shorted to (AVDD+AVSS)/2 at TA = 25°C.

uVrms and uVpp are measurements from at least 1000 points, and the other three parameters are calculated using the following formula:

$$\text{Dynamic Range} = 20 \times \log\left(\frac{\text{VREF}}{\sqrt{2} \times \text{Gain} \times V_{RMS}}\right)$$

$$\text{Noise-Free Bits} = \log_2 \frac{2 * \text{VREF}}{\text{Gain} * \text{uVpp}}$$

$$\text{ENOB} = \log_2\left(\frac{\text{VREF}}{\sqrt{2} \times \text{Gain} \times V_{RMS}}\right)$$

Under a 5V power supply and a 4.605V reference:

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	PGA Gain=1					PGA Gain=2				
		µVrms	µVpp	DYNAMIC RANGE (dB)	NOISE -FREE BITS	ENOB	µVrms	µVpp	DYNAMIC RANGE (dB)	NOISE -FREE BITS	ENOB
000	16000	17.94	165.79	105.16	15.76	17.47	10.49	119.28	103.81	15.24	17.24
001	8000	9.91	68.28	110.32	17.04	18.32	4.88	34.82	110.46	17.01	18.35
010	4000	6.91	49.05	113.45	17.52	18.84	3.41	22.62	113.57	17.63	18.86
011	2000	5.05	33.43	116.17	18.07	19.3	2.45	15.48	116.44	18.18	19.34
100	1000	3.48	22.48	119.41	18.64	19.83	1.76	11.37	119.31	18.63	19.82
101	500	2.48	15.63	122.36	19.17	20.32	1.27	8.5	122.14	19.04	20.29
110	250	1.75	10.41	125.38	19.75	20.83	0.87	5.89	125.43	19.57	20.83

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	PGA Gain=4					PGA Gain=6				
		µVrms	µVpp	DYNAMIC RANGE (dB)	NOISE -FREE BITS	ENOB	µVrms	µVpp	DYNAMIC RANGE (dB)	NOISE -FREE BITS	ENOB
000	16000	5.18	61.01	103.92	15.2	17.26	3.62	36.31	103.5	15.37	17.19
001	8000	2.6	19.95	109.9	16.81	18.25	1.84	13.53	109.39	16.79	18.17
010	4000	1.78	11.04	113.2	17.67	18.8	1.35	7.86	112.07	17.57	18.61
011	2000	1.33	8.56	115.72	18.03	19.22	0.95	6.22	115.13	17.91	19.12
100	1000	0.94	6.24	118.74	18.49	19.72	0.69	4.57	117.9	18.36	19.58
101	500	0.66	4.46	121.81	18.98	20.23	0.46	2.88	121.43	19.02	20.17
110	250	0.45	2.88	125.14	19.61	20.79	0.34	2.06	124.05	19.51	20.6

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	PGA Gain=8					PGA Gain=12				
		µVrms	µVpp	DYNAMIC RANGE (dB)	NOISE -FREE BITS	ENOB	µVrms	µVpp	DYNAMIC RANGE (dB)	NOISE -FREE BITS	ENOB
000	16000	2.7	19.7	103.55	15.83	17.2	2.16	15.19	101.97	15.62	16.94
001	8000	1.56	10.17	108.32	16.79	17.99	1.22	7.88	106.93	16.57	17.76
010	4000	1.09	7.47	111.43	17.23	18.51	0.86	5.5	109.97	17.09	18.27
011	2000	0.77	4.8	114.45	17.87	19.01	0.62	3.68	112.81	17.67	18.74
100	1000	0.56	3.73	117.21	18.23	19.47	0.42	2.63	116.2	18.15	19.3
101	500	0.38	2.47	120.59	18.83	20.03	0.31	1.96	118.83	18.58	19.74
110	250	0.27	1.61	123.55	19.45	20.52	0.21	1.37	122.22	19.09	20.3

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	PGA Gain=24				
		µVrms	µVpp	DYNAMIC RANGE (dB)	NOISE -FREE BITS	ENOB
000	16000	1.43	8.79	99.53	15.41	16.53
001	8000	0.99	6.44	102.72	15.86	17.06
010	4000	0.69	4.31	105.86	16.44	17.58
011	2000	0.5	2.91	108.66	17.01	18.05
100	1000	0.35	2.32	111.76	17.33	18.56
101	500	0.24	1.49	115.04	17.97	19.11
110	250	0.17	1.08	118.03	18.44	19.6

13. Functional Description

- **Overview**

The DADS1292's analog input channels offer flexible path allocation for measuring temperature, supply voltage, internal short circuit, and bias voltage. The DADS1292's two analog input channels can be flexibly configured as human body bias electrodes, allowing for the selection and combination of human body bias signals. Lead-off detection uses a current source and can be configured for DC or AC detection modes. In addition to using external references and clocks, the DADS1292 can utilize an internal low-noise reference and internal oscillator. The PGA offers configurable gains of 1 , 2 , 4 , 6 , 8 , 12 , and 24, and the ADC sampling rate is selectable between 250 SPS and 16 kSPS. It features an SPI interface, two GPIOs, and can use the START pin to achieve synchronous operation of multiple devices.

- **Feature Description**

This section describes some of the circuit characteristics of the DADS1292, including its analog, digital, and EEG (ECG) circuitry. In the following description, f_{CLK} is the frequency of the CLK pin, t_{CLK} is the period of f_{CLK}, f_{DR} is the sampling rate of the ADC output data, t_{DR} is the period of f_{DR}, and f_{MOD} is the rate of the ADC modulator output data, t_{MOD} is the period of f_{MOD}.

1) Analog section

The analog section includes: analog switches, PGA, reference, and ADC.

■ Analog input switch

Each analog channel in front of the PGA has a configurable analog switch, providing flexible input channel selection for the PGA input.

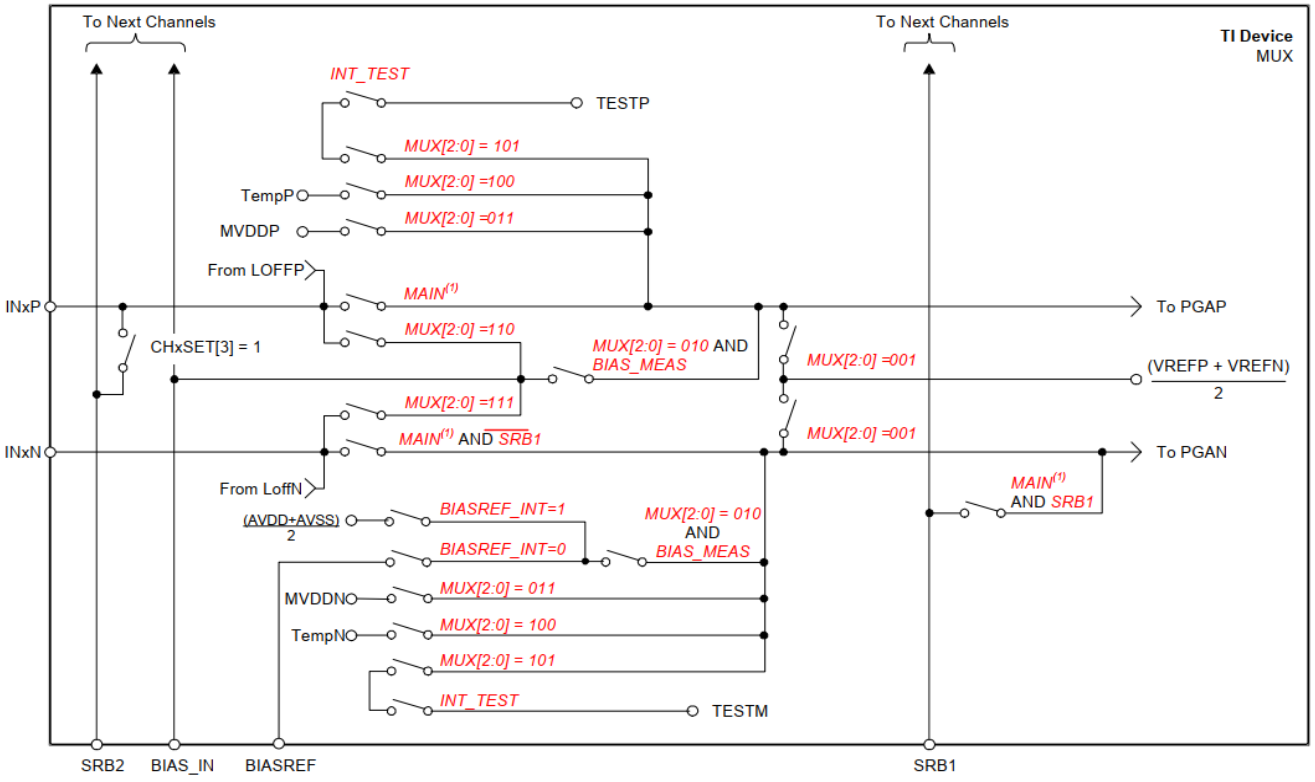


Figure 3. Channel Analog Switch

The analog input switches of the DADS1292 can achieve the following signal distribution and other specifications:

1. The external electrode signal Normal Electrode (INxP,INxN) is set to CHnSET[2:0]=000, which connects the input of the PGA channel to INxP and INxN to measure the external differential input signal.
2. Internally shorting INT_SHORT and setting CHnSET[2:0]=001 can internally short the input of the channel PGA to (VREFP+VREFN)/2, which can measure the noise of the channel.
3. For BIASIN measurement, set CHnSET[2:0]=010 and BIAS_MEAS=1, and connect the input of channel PGA to BIASIN and BIASREF respectively to measure the (BIASIN-BIASREF) differential signal. BIASREF can be internal or external.
4. To measure the power supply voltage (MVDDP, MVDDN), set CHnSET[2:0]=011. You can connect the input of channel PGA to (AVDD+AVSS)/2 to measure the power supply voltage.
5. Temperature measurement signals (TempP, TempN), set CHnSET[2:0]=100, can connect the input of channel PGA to the internal temperature sensor to measure the internal temperature of the device. The temperature measurement formula is:

T= (Treading(uV)-145300uV) /490uV+25, the unit is degrees Celsius.

6. The internal test signal INT_TEST(TESTP, TESTN) can be connected to the internal test signal by setting CHnSET[2:0]=101. The internal test signal can be configured as DC and AC (frequency-configurable square wave) in CONFIG2.
7. To assign the BIASIN signal to the INxP or INxN electrode, set CHnSET[2:0]=110 or 111. For details, refer to the EEG or ECG characteristics.
8. The constant current source and comparator with lead-off function are connected to INxP or INxN. There are also DC and AC options. Please refer to the EEG or ECG characteristics for details.

■PGA and benchmark

The DADS1292's internal PGA is a fully differential input/output. The PGA output can be selectively fed into the inverting input of a BIAS AMP to flexibly generate human body BIAS signals. The DADS1292 integrates a low-noise reference circuit, with the reference voltage reference point being AVSS, typically 4.6V. The reference voltage is amplified by a bandgap, requiring a 10uF~100uF filter capacitor to be reserved for the bandgap. In addition to the internal reference, the internal reference amplification circuit can be disabled, and the reference voltage can be provided externally via VREFP and VREFN pins.

■ΔΣ ADC

After the PGA of each channel, the DADS1292 has two 24-bit ΔΣ ADCs that can work in parallel. The sampling rate of the input analog signal by the low-noise second-order modulator of the ADC is $f_{MOD} = f_{CLK} / 2$. The bandwidth of the digital signal after quantization by the modulator is $f_{MOD} / 2$, and then it is sent out after passing through a third-order digital filter.

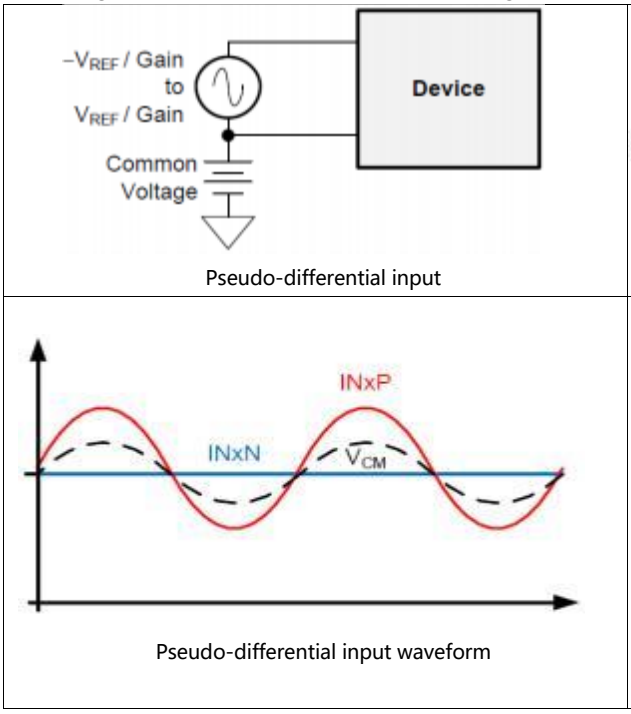
The digital filter is a third-order Sinc filter with infinitesimal gain at integer multiples of f_{DR}. Its -3dB bandwidth is shown in the table below:

DR (Hz)	16000	8000	4000	2000	1000	500	250
-3dB bandwidth (Hz)	4193	2096	1048	524	262	131	65

After receiving the Start signal, the digital filter will only have the first set of data after tSETTLE = $4*t_{DR}$ time. After that, it can output data at the DR rate. If there is a jump in the analog signal during the data output process, it will take $3*t_{DR}$ time to obtain a stable ADC result.

■Analog signal input

The analog input of the DADS1292 is a differential signal, and the differential input voltage (VINxP-VINxN) ranges from -VREF/gain to +VREF/gain.



Pseudo-differential input | Differential input

Pseudo-differential input waveform | Differential input waveform

Note : Pseudo-differential input is equivalent to superimposing a common-mode signal on the differential signal. The amplitude of this common-mode signal is half that of the original differential signal. Pseudo-differential input will cause the dynamic range of the input signal to be halved. Regardless of the type of input, the linear operating range of the analog circuitry must be considered, which is from AVDD-1.3V to AVSS+0.3V. This limitation must apply to the entire signal chain of the analog input. The applied differential signal, common-mode point, PGA gain, etc., all need to take this limitation into account.

2) Digital part

■ **Clock**

The DSD1292 integrates an internal oscillator to generate a 2.048MHz clock, but an external clock source can also be used.

CLKSEL pin input level	Register CONFIG1.CLK_EN bit	Clock source	CLK pin function
0	X	External	Input external clock
1	0	Internal	Three states
1	1	Internal	Output internal clock

■ **GPIO**

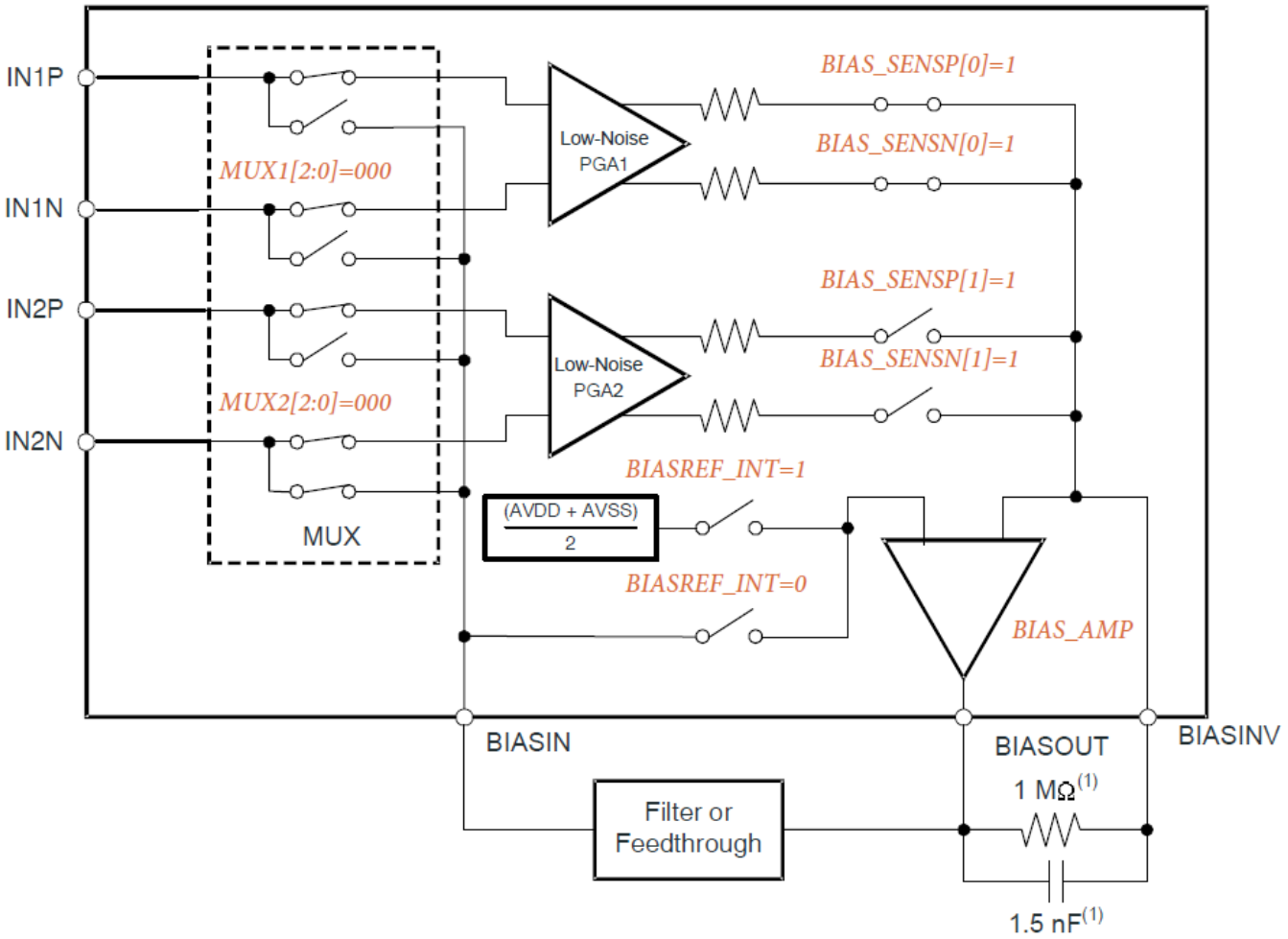
The DSD1292 has two general-purpose I/O ports that can be used when not powered down:

GPIOC is configured	Write GPIOD Operation	Read GPIOD Operation
Input	Invalid	Read back to the currentpin value
Output	GPIOD 's data is output topin	

3) ECG and EEG functions

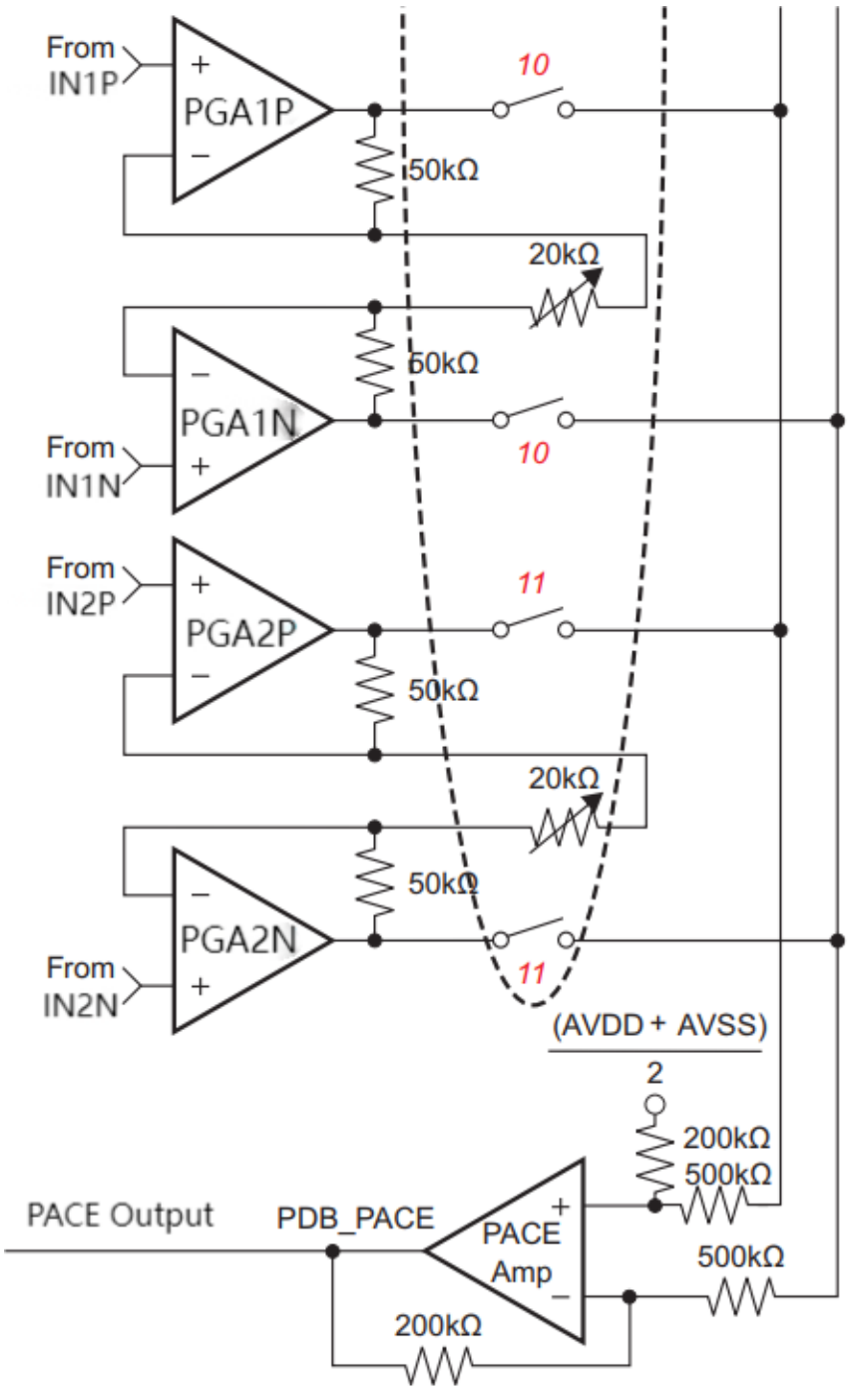
■ **BIAS /RLD and PACE drive circuits**

When measuring human body electrical signals, the human body needs to be driven to a suitable voltage by the BIAS /RLD. The DSD1292 can arbitrarily select the outputs of two PGAs to generate the BIAS voltage for the human body, as shown in the example diagram below: IN1P, IN2P, IN1N, and IN2N are the measured human body electrical signals. After passing through the PGAs, they are selected and sent to BIAS_AMP. The resulting adder circuit amplifies the common-mode point Vcm of multiple signals by inverting the reference BIASREF. BIASOUT can then be sent to drive the human body. This loop can improve the measured CMRR . In application, the stability of the loop needs to be considered; a capacitor can be reserved as a potential pole.



(1) Typical values are only used as examples.

The chip's PACE pin outputs a signal for pacemaker detection, with selectable channel 1 or 2 for PACE detection (see the PACE register). As shown in the figure, the PACE output is the corresponding channel signal amplified by the PGA and then attenuated by 0.4 times. External hardware or software methods are required to detect the pacemaker signal.

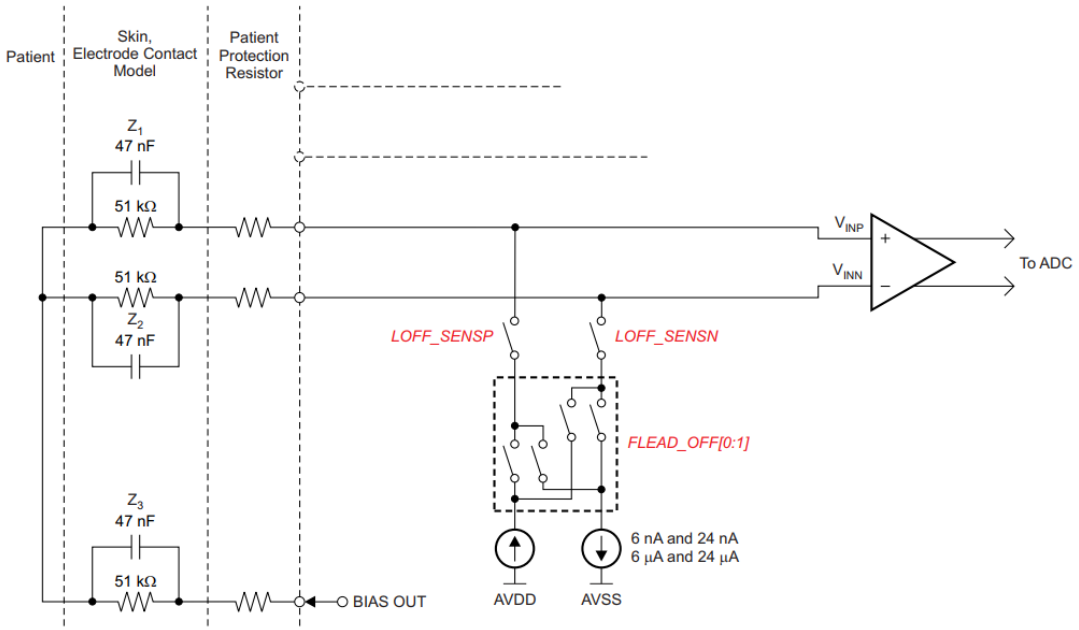


PACE Generation Circuit

■ Channel Lead-Off Detection

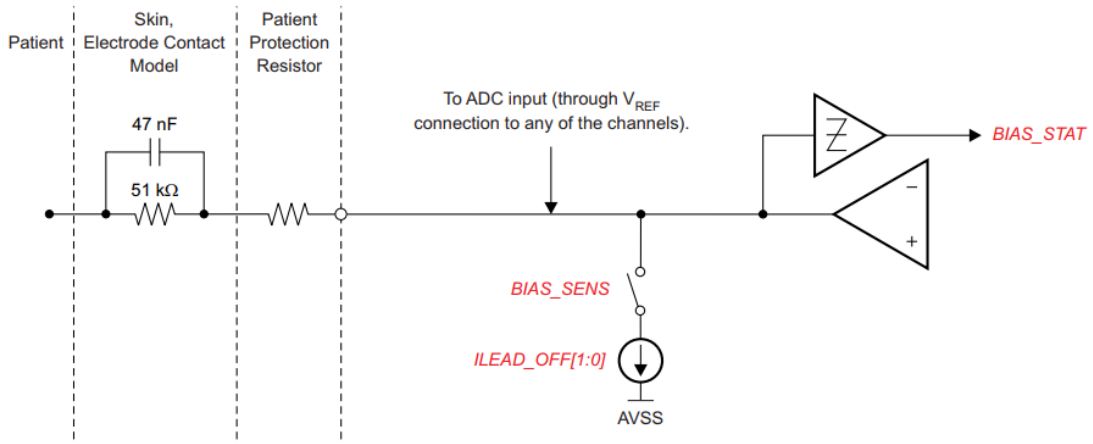
The DADS1292 uses a constant current source/sink to detect electrode drop. The constant current source has four selectable levels. During DC-LEAD-Off detection, a lead-off comparator can be used to locate the dropped probe. The comparator has multiple configuration levels, and the comparator results are displayed in the LOFFPx and LOFFNx registers. AC-Lead-off involves configuring the constant current source to output pulses (7.8Hz or 3.2Hz pulses) to form an in-band AC constant current source that drives the impedance between INxP and INxN. The algorithm analyzes the ADC code results and measures the amplitude at these two frequencies (7.8Hz/3.2Hz) to determine the impedance change between INxP and INxN, thus determining whether a lead-off has occurred. AC-lead-off cannot be applied simultaneously with the acquisition of human body electrical signals.

The source and sink are applied to INxP and INxN by default, respectively, and can also be used after FLIP. The detection principle is shown in the following figure:



■ BIAS / RLD Lead-Off Detection

The BIAS/RLD Lead-Off mechanism works differently when BIAS-AMP is off/on, as shown in the following diagram:



When BIAS-AMP is off	When BIAS-AMP is enabled
The constant current source of the sink enables the state BIAS_STAT, which is obtained together with the comparator and represents the lead-off condition.	The constant current source has been shut down, and only a comparator is used to obtain BIAS_STAT

■ Respiratory impedance testing

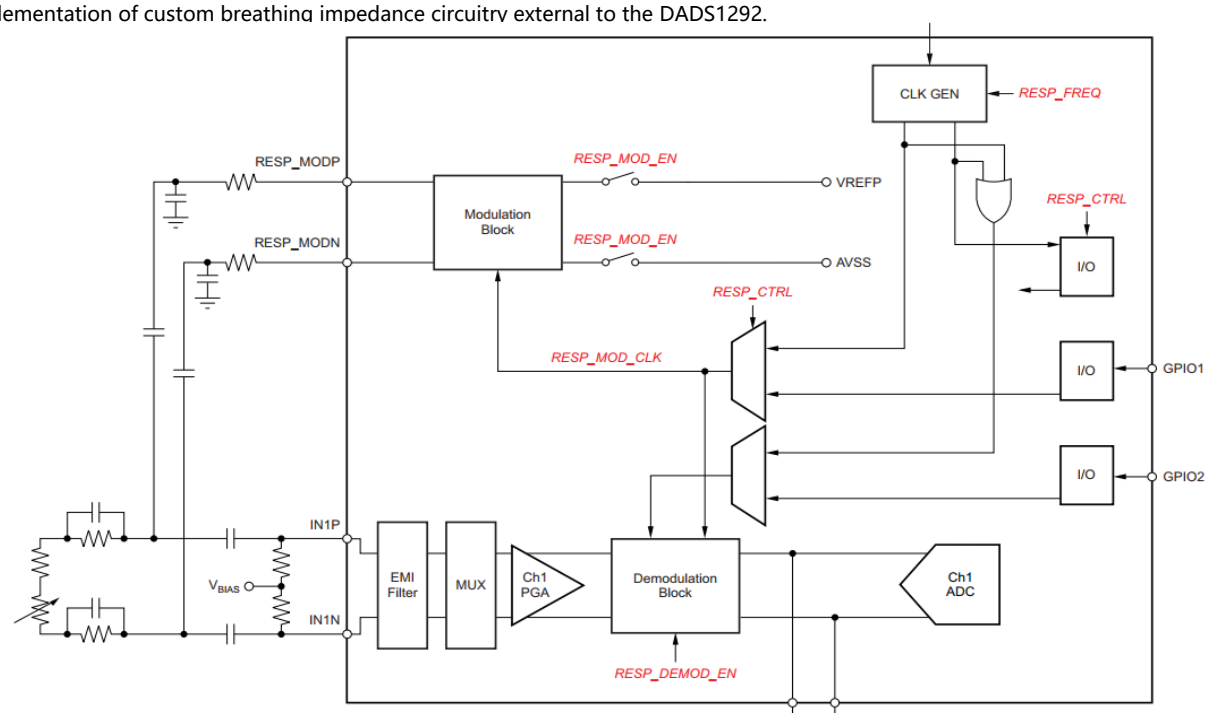
As shown in the table below, DADS1292 offers three options for respiratory impedance measurement: external breathing, internal breathing using the chip modulation signal, and internal breathing using a modulation signal generated by the user.

RESP_CTRL[1]	RESP_CTRL[0]	Description
0	0	Disable breathing mode
0	1	Generate modulation and demodulation signals for the external breathing circuit. The RESP_CLK signals on GPIO1 and GPIO2.
1	0	Respiratory measurements were performed using an internally generated RESP_MOD signal.
1	1	Respiratory measurements were performed using user-generated modulation and occlusion signals.

Note: If CLKSEL=1 (internal master clock),do not set RESP_CTRL[1:0]=11.

1. External breathing mode (RESP_CTRL=01b)

Using this option, GPIO 1 and GPIO 2 can be automatically configured as outputs, as shown in the figure below. GPIO 1 is the modulation signal, and GPIO 2 is the demodulation signal. When using this option, the general-purpose pin functions of GPIO 1 and GPIO 2 are unavailable. The modulation frequency can be set to 64kHz or 32kHz using the RESP_FREQ[2:0] bits in the CONFIG4 register. The remaining bits of RESP_FREQ[2:0] can generate square waves on GPIO 1 and GPIO 2. XOR on GPIO 2 is only available at 64kHz or 32kHz frequencies. This option allows for the implementation of custom breathing impedance circuitry external to the DADS1292.



2. mode with an internal clock (RESP_CTRL=10b)

The modulation block is controlled by the RESP_MOD_EN bit, and the demodulation block is controlled by the RESP_DEMOD_EN bit. The modulation signal is a square wave with an amplitude of VREFP–AVSS. Using this option, the output of the modulation circuit can be obtained on the RESP_MODP and RESP_MODN pins of the device. This availability allows for the addition of custom filters to the square wave modulation signal. Using this option, GPIO 1 and GPIO 2 can be used for other purposes. The modulation frequency is 64kHz or 32kHz and can be set via the RESP_FREQ[2:0] bits in the CONFIG4 register. The phase of the internal demodulated signal can be set via the RESP_PH[2:0] bits in the RESP register. With this breathing option enabled, DADS1292 channel 1 cannot be used to acquire EEG/ ECG signals.

3. Internal breathing circuit with user-generated signals (RESP_CTRL=11b)

In this mode, GPIO 1 and GPIO 2 are automatically configured as inputs and cannot be used for other purposes. Signals must be provided as shown in the diagram above . Do not use the internal master clock in this mode.

- **Work mode**

1) Power consumption mode

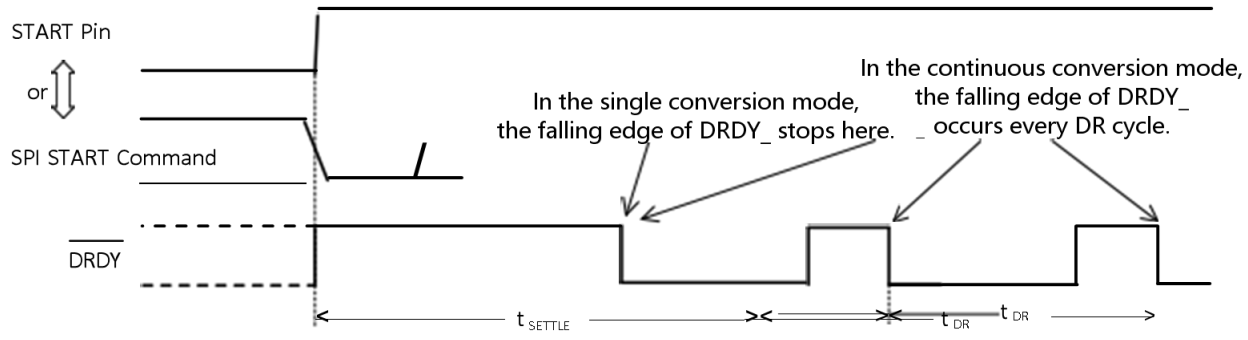
Power consumption mode	Description
Normal mode	PWDN_ = 1, and no Standby command has been received. All functions are running. The BIAS-AMP, REF-BUFFER, internal CLK and other modules are enabled/disabled according to the configuration.
Standby mode	PWDN_ = 1. Enters in Normal mode upon receiving the Standby command. Except for the reference source, the source of CLK and the SPI port, all other modules are shut down, and only the Wakeup command is received.
Shutdown mode	PWDN_ = 0, all functional modules are turned off, the configuration of the registers is retained. To exit this state, PWDN_ must be set to 1.

2) START state

In Normal mode, pulling the START pin high for more than two t_{CLK} cycles, or sending a START command via the SPI port (the falling edge of the 7 SCK cycles of the SPI command), will cause the DADS1292 to enter the START state. Immediately after entering START mode, the DADS1292 sets DRDY_ = 1. After t_{SETTLE} , the first falling edge of DRDY_ indicates that the conversion data is ready. If you only want to control START using SPI commands, you need to keep the START pin low. Without entering the START state, the DADS1292 will not output the falling edge signal of DRDY_. The falling edge of DRDY_ indicates that the DADS1292 has completed one parallel ADC data conversion; the DRDY signal is unaffected by the CS signal. In multi-chip operation, the START pin is used to synchronize all DADS1292 ADCs, ensuring that all ADCs sample at the same time. In the following description, the "START signal" is defined as: pulling the START pin high for more than 2 t_{CLK} , or sending a START command via the SPI port (the command is recognized on the falling edge of the 7th SCK). The t_{SETTLE} time after START is 4 t_{DR} times.

3) Continuous/Single Conversion Mode

The value of SINGLE_SHOT in the CONFIG4 register, whether 0 or 1, determines whether the DADS1292 operates in continuous conversion mode or single-shot conversion mode. In continuous conversion mode (SINGLE_SHOT=0), after the first falling edge of DRDY_ , DRDY_ will continuously appear with falling edges at sampling intervals determined by DR. If the DADS1292 operates in single-shot conversion mode (SINGLE_SHOT=1), only one falling edge of DRDY_ will appear.



The difference between continuous conversion and single conversion

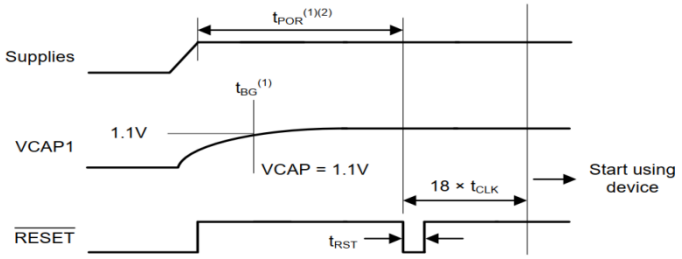
Two commands can be used to retrieve data in both modes: the RDATAC command and the RDATA command (see subsequent command descriptions). In continuous/single conversion mode, DRDY_ = 0 after a falling edge, and then DRDY_ = 1 on the falling edge of the SCK of the first SPI command (CS=0) . Without an SPI command, in single conversion mode, DRDY_ remains 0 after the first DRDY_ = 0 ; in continuous conversion mode, DRDY_ = 1 for four tCLK times before the next falling edge of DRDY_ (interval t_{DR}). The DADS1292 defaults to continuous conversion mode and is in RDATAC mode upon power-up.

4) Data reading

Data format: The data length containing the ADC result is 72 bits , [(24 status bits + 24 bits × 2 channels) = 72 bits] , where the 24 status bits are: (1100 + LOFF_STATP + LOFF_STATN + bits[4:7] of the GPIO register).

5) RESET and power-on reset

The DADS1292 can be reset using the RESET pin or the RESET command. When using the RESET pin, the low-level hold time must be greater than t_{RESET}. The RESET command takes effect on the falling edge of the 8th SCLK. After the reset, it takes 18 t_{CLK} cycles to complete initialization. Each write to CONFIG1 triggers the reset of the ΔΣ ADC digital filter. After the chip powers on, the voltage of VCAP1 rises slowly (the rate of rise depends on the size of the external capacitor connected to VCAP1). When VCAP1 exceeds 1.1V, resetting again using the RESET pin ensures that the chip enters the normal initialization mode. Without this reset, and if the external capacitor of VCAP1 is large, causing the voltage to rise slowly, the chip may enter an incorrect state and fail to operate.



Power-on reset

- **Programming**

1) Data format

The ideal DADS1292 stores the ADC result in a 24-bit two's complement format, as shown in the table below:

Input signal, V_{IN} (INxP-INxN)	Ideal Output Code
>=FS	7FFFFFh
+FS/(2^23–1)	000001h
0	0 000000h
–FS/(2^23–1)	FFFFFFh
<=–FS	800000h

1LSB=(2×VREF/Gain)/2^24=+FS/2^23

2) SPI interface

The SPI interface includes four signals: CS, SCLK, DIN , and DOUT.

3) SPI commands

Order	Description	First byte	Second byte
System commands			
WAKEUP	Standby wake-up	0000 0010 (02h)	
STANDBY	Enter Standby	0000 0100 (04h)	
RESET	Reset	0000 0110 (06h)	
START	Start synchronous conversion	0000 1000 (08h)	
STOP	Stop synchronous conversion	0000 1010 (0Ah)	
Data read and write commands			
RDATAC	Enter continuous conversion mode (default upon power-on)	0001 0000 (10h)	
SDATAC	Stop continuous conversion mode	0001 0001 (11h)	
RDATA	The data read command supports continuous reading.	0001 0010 (12h)	
Register read/write commands			
RREG	Read register	001r rrrr (2xh)	000n nnnn
WREG	Write register	010r rrrr (4xh)	000n nnnn

- **Register definition**

1. Register allocation table

Address	Registration	Default settings	Register bits							
			7	6	5	4	3	2	1	0
Read-only ID register										
00h	ID	xxh	REV_ID[2:0]							
Global settings across channels										
01h	CONFIG1	96h	1	DAISY_EN_	CLK_EN	1	HDR_EN	D R[2:0]		
02h	CONFIG2	C0h	1	1	0	INT_CAL	0	CAL_AMP0	CAL_FREQ[1:0]	
03h	CONFIG3	60h	PD_REF BUF_	1	VREF_4V	BIAS_MEAS	BIASREF_ INT	PD_BIAS_	BIAS_LOFF_ SENS	PD_BIAS_
04h	LOFF	00h	COMP_TH[2:0]			0	ILEAD_OFF[1:0]		FLEAD_OFF[1:0]	
Channel-specific settings										
05h	CH1SET	61h	PD1	GAIN1 [2:0]			SRB2	MUX1[2:0]		
06h	CH2SET	61h	PD2	GAIN2 [2:0]			SRB2	MUX2[2:0]		
0Dh	BIAS_SENSP	00h							BIASP2	BIASP1
0Eh	BIAS_SENSN	00h							BIASN2	BIASN1
0Fh	LOFF_SENSP	00h							LOFFP2	LOFFP1
10h	LOFF_SENSN	00h							LOFFN2	LOFFN1
11h	LOFF_FLIP	00h							LOFF_FLIP2	LOFF_FLIP1
Lead-off status register (read-only register)										
12h	LOFF_STATP	00h							IN2P_OFF	IN1P_OFF
13h	LOFF_STATN	00h							IN2N_OFF	IN1N_OFF
GPIO and other registers										
14h	GPIO	0Fh	GPIOD[4:1]				GPIOC[4:1]			
15h	PACE	00h	0	0	SRB1	0	0	PACE_SEL		PD_PACE_b
16h	RESP	00h	RESP_DE MOD_EN	RESP_MO D_EN	0	RES_PH			RESP_CTRL	
17h	CONFIG4	00h	0	0	0	0	SINGLE_S HOT	0	PD_LOFF_C OMP_	0

ID: ID control register (address = 00h) (reset = xxh)

7	6	5	4	3	2	1	0
REV_ID[7:0]							
R-xh			R- xh	R-3h		R-xh	

Note: R/W = Read/Write; R = Read Only; -n = Reset value

2. ID Control Register Field Description

Bit	Fields	Type	Reset	Description
1:0	REV _ ID [7 : 0]	R	xh	0xAC : Version A chip 0xBC : Version B chip

CONFIG1: Configuration Register 1 (Address = 01h) (Reset = 96h / 06h)

This register configures the DAISY_EN bit , clock, and data rate.

7	6	5	4	3	2	1	0
1	DAISY_EN_	C LK_EN	1	0	DR [2:0]		
R/ W -1h	R/ W -0h	R/ W -0h	R/ W -1h	R/ W -0h	R/ W -6h		

Note : R/W = Read/Write; R = Read-only; -n = Reset value

3. Description of Field 1 in Configuration Register

Bit	Fields	Type	Reset	Description
7	Reserved	R/W	1h	Reserved
6	D AISY_EN_	R/W	0h	Daisy chain or multiple readback mode 0 : Enable daisy chain mode; 1 : Turn off daisy chain mode
5	CLK_EN	R/W	0h	Clock connection When the CLKSEL pin is 1, this bit determines whether the internal oscillator signal is connected to the CLK pin. 0 : Oscillator clock output disabled; 1 : Oscillator clock output enabled
4	Reserved	R/W	1h	Reserved
3	HDR_EN	R/W	0h	High dynamic range enabled: 0: Disabled. This configuration requires external connections to AVDD and VCAP3 for the A version chip (ID=0xAC) to function; for the B version chip (ID=0xBC), it does not require connections to AVDD and VCAP3 to function. 1: Enable. This configuration is only valid for version A (ID=0xAC) chips, and AVDD and VCAP3 cannot be connected externally; version B chips (ID=0xBC) do not support this configuration.
2:0	DR[2:0]	R/W	6h	Output data rate. These bits determine the chip's output data rate: $f_{MOD} = f_{CLK}/2$. 000 : $f_{MOD}/64$ (16kSPS) 001 : $f_{MOD}/128$ (8kSPS) 010 : $f_{MOD}/256$ (4kSPS) 011 : $f_{MOD}/512$ (2kSPS) 100 : $f_{MOD}/1024$ (1kSPS) 101 : $f_{MOD}/2048$ (500SPS) 110 : $f_{MOD}/4096$ (250SPS) 111 : Reserved (not used)

CONFIG2: Configuration Register 2 (Address = 02h) (Reset = C0h / 40h)

This register is primarily configured to generate test signals.

CONFIG2: Configuration Register 2

7	6	5	4	3	2	1	0
1	1	0	INT_CAL	0	CAL_AMP	CAL_FREQ[1:0]	
R/W- xh	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Note : R/W = Read/Write; R = Read Only; -n = Reset value

4. Description of field 2 in configuration register

Bit	Fields	Type	Reset	Description
7:5	Reserved	R/W	6 h/2h	Reserved
4	INT_CAL	R/W	0 h	Test source. This bit determines the source of the test signal. 0 : The test signal is driven externally; 1 : Internally generated test signal
3	Reserved	R/W	0 h	Reserved. Always write 0h.
2	Calibration amplifier	R/W	0 h	Test signal amplitude 0 : 1× (VREF P- VREFN)/2400 1 : 2×(VREFP-VREFN)/2400
1:0	CAL_FREQ[1:0]	R/W	0 h	Test signal frequency 00 : In the $f_{CLK}/221$ pulse; 01 : In $f_{CLK}/220$ pulse 10 : Not used 11 : DC

CONFIG3: Configuration register 3 (address = 03h) (reset = 60h / 40h)

This register configures internal or external references and BIAS operations.

CONFIG3: Configuration Register 3 Table

7	6	5	4	3	2	1	0
PD_REFBUF_	1	VREF_4V	BIAS_MEAS	BIASREF_INT	PD_BIAS_	BIAS_LOFF_SENS	BIAS_STAT
R/W-0h	R/W-1h	R/W- 0/1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

5. Description of the 3 fields in the configuration register

Bit	Fields	Type	Reset	Description
7	PD_REFBUF_	R/W	0h	The reference buffer is de-energized . This bit determines the de-energized state of the reference buffer. 0 : Power-off internal reference buffer 1 : Enable internal reference buffer
6	Reserved	R/W	1h	Reserved
5	VREF_4V	R/W	0/1h	Reference voltage. This bit determines the internal reference voltage VREFP. 0=VREFP is set to 2.4 60 V 1=VREFP is set to 4.605 V (for use with a 5V analog power supply only).
4	BIAS_MEAS	R/W	0h	The BIAS measurement bit enables BIAS measurement. The BIAS signal can be measured using any channel. 0 : Open; 1 : The BIAS_IN signal is routed to the channel with MUX_Setting = 010.
3	BIASREF_INT	R/W	0h	The BIASREF signal . This bit determines the source of the BIASREF signal. 0 : BIASREF signal external feed; 1 : The BIASREF signal (AVDD+AVSS)/2 is generated internally.
2	PD_BIAS_	R/W	0h	BIAS buffer power . This bit determines the power state of the BIAS buffer. 0 : BIAS buffer de-energized; 1 : BIAS buffer enabled
1	BIAS_LOFF_SENS	R/W	0h	BIAS detection function . This bit enables the BIAS detection function. 0 : BIAS detection is disabled; 1 : BIAS detection enabled
0	BIAS_STAT	Read-only	0h	BIAS lead status . This bit displays the BIAS lead status. 0 : BIAS is connected; 1 : BIAS not connected

LOFF: Lead Detection Control Register (Address = 04h) (Reset = 00h)

This register is configured for lead detachment detection.

LOFF: Lead Detection Control Register

7	6	5	4	3	2	1	0
COMP_TH2[2:0]			0	ILEAD_OFF[1:0]		FLEAD_OFF[1:0]	
R/W-0h			R/W - 0h	R/W-0h		R/W - 0h	

Note : R/W = Read/Write; R = Read Only; -n = Reset value

6. Explanation of Lead Detection Control Register Fields

Bit	Fields	Type	Reset	Description
7:5	COMP_TH[2:0]	R/W	0h	Lead detection comparator threshold 000 : Comparator positive electrode 95%; Comparator negative electrode 5% 001 : Comparator positive electrode 92.5%; Comparator negative electrode 7.5% 010 : Comparator positive electrode 90% ; Comparator negative electrode 10% 011 : Comparator positive electrode 87.5%; Comparator negative electrode 12.5% 100 : Comparator positive electrode 85%; Comparator negative electrode 15% 101 : Comparator positive electrode 80%; Comparator negative electrode 20 % 110 : Comparator positive electrode 75%; Comparator negative electrode 25% 111 : Comparator positive electrode 70%; Comparator negative electrode 30%
4	Reserved	R/W	0h	Reserved. Always write 0h.
3:2	ILEAD_OFF[1:0]	R/W	0h	Magnitude of the continuity detection current . These bits determine the magnitude of the current being detected in the current lead . 00 : 10nA 01 : 40nA 10 : 8.5μA 11 : 34μA
1:0	FLEAD_OFF[1:0]	R/W	0h	Continuity detection frequency. These bits determine the lead detachment detection frequency for the channel. 00 : DC lead detection 01 : AC lead detachment detection at 7.8Hz ($f_{CLK}/2^{18}$) 10 : Joint shedding detection at 31.2Hz ($f_{CLK}/2^{16}$) 11 : AC lead dropout detection in fDR / 4

CHnSET: Channel settings (n=1 to 2) (address=05h to 06h) (reset=61h)

This control register configures the channel's power consumption mode, PGA gain, and multiplexer settings.

CHnSET: Channel Setting Register

7	6	5	4	3	2	1	0
PDn	Gain [2:0]			SRB2	Multiplexer [2: 0]		
R/W-0h	R/W-6h			R/W-0h	R/W-0h		

Note : R/W = Read/Write; R = Read Only; -n = Reset value

7. Channel Settings (n=1 to 8) Register Field Description

Bit	Fields	Type	Reset	Description
7	PDn	R/W	0h	Power off. This bit determines the power off mode for the corresponding channel. 0 : Normal operation. 1 : Power outage in the channel. When closing a channel, it is recommended to set the channel to input short circuit by setting CHnSET register MUXn[2:0] = 001.
6:4	Gain [2:0]	R/W	6h	PGA gain. These bits determine the PGA gain setting. 000 : 1 001 : 2 010 : 4 011 : 6 100 : 8 101 : 12 110 : 24 111 : Do not use
3	SRB2	R/W	0h	SRB2 connection. This bit controls the connection between the P stage of the corresponding channel and SRB2. 0 : Disable SRB2 function 1 : Enable SRB2 function
2:0	Multiplexer [2: 0]	R/W	1h	Channel input. These bits determine the channel input selection. 000 : Normal electrode input 001 : Input short circuit (used for offset or noise measurement) 010 : Used in conjunction with the BIAS_MEAS bit used for BIAS measurements. 011 : MVDD for power supply measurement 100 : Temperature sensor 101 : Test signal 110 : BIAS_DRP (BIAS_IN and P-level connections) 111 : BIAS_DRN (BIAS_IN and N-level join)

BIAS_SENSP: BIAS positive terminal signal sensing register (address=0Dh) (reset=00h)

This register controls the connection of the positive terminal signal of the control channel to the bias circuit (BIAS).

BIAS_SENSP: BIAS positive terminal signal sensing register

7	6	5	4	3	2	1	0
BIASP8	BIASP7	BIASP6	BIASP5	BIASP4	BIASP3	BIASP2	BIASP1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

8. Description of BIAS Positive Terminal Signal Sensing Register Fields

Bit	Fields	Type	Reset	Description
1	BIASN2	R/W	0h	from IN2N to BIAS bias circuit 0: Disable 1: Enable
0	BIASN1	R/W	0h	from IN1N to BIAS bias circuit 0: Disable 1: Enable

BIAS_SENSN: BIAS negative terminal signal sensing register (address=0Eh) (reset=00h)

This register controls the connection of the negative terminal signal of the control channel to the bias circuit (BIAS).

BIAS_SENSN: BIAS negative terminal signal sensing register

7	6	5	4	3	2	1	0
BIASN8	BIASN7	BIASN6	BIASN5	BIASN4	BIASN3	BIASN2	BIASN1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

9. Description of the fields in the BIAS negative terminal signal sensing register

Bit	Fields	Type	Reset	Description
1	BIASN2	R/W	0h	from IN2N to BIAS bias circuit 0: Disable 1: Enable
0	BIASN1	R/W	0h	from IN1N to BIAS bias circuit 0: Disable 1: Enable

LOFF_SENSP: Positive lead detachment detection register (address=0Fh) (reset=00h)

This register controls the detection of disconnection of the positive lead of the channel.

LOFF_SENSP: Positive Lead Dropout Detection Register

7	6	5	4	3	2	1	0
RES						LOFFP2	LOFFP1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

10. Description of the positive lead detachment detection register fields

Bit	Fields	Type	Reset	Description
1	LOFFP2	R/W	0h	IN2P lead-off detection 0: Disable 1: Enable
0	LOFFP1	R/W	0h	IN1P lead-off detection 0: Disable 1: Enable

LOFF_SENSN: Negative lead disconnection detection register (address=10h) (reset=00h)

This register controls the detection of disconnection of the negative lead of the channel.

LOFF_SENSN: Negative lead detachment detection register

7	6	5	4	3	2	1	0
LOFFN8	LOFFN7	LOFFN6	LOFFN5	LOFFN4	LOFFN3	LOFFN2	LOFFN1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

11. Description of the negative lead detection register fields

Bit	Fields	Type	Reset	Description
1	LOFFN2	R/W	0h	IN2N lead-off detection 0 : Disabled 1 : Enable
0	LOFFN1	R/W	0h	IN1N lead-off detection 0 : Disabled 1 : Enable

LOFF_FLIP: Lead detection current toggle register (address=11h) (reset=00h)

This register controls the direction of the current for lead detachment detection .

LOFF_FLIP: Lead Sense Current Flip Register

7	6	5	4	3	2	1	0
						LOFF_FLIP2	LOFF_FLIP1
R/W0h	R/W0h	R/W0h	R/W0h	R/W0h	R/W0h	R/W0h	R/W0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

12. Explanation of the Lead Detection Current Toggle Register Fields

Bit	Fields	Type	Reset	Description
1	LOFF_FLIP2	R/W	0h	Channel 2LOFF polarity reversal Flip the pull-up or pull-down polarity of the current source on channel 2 to perform lead disconnection detection. 0 : No flip = IN2P is pulled to AVDD and IN2N is pulled to AVSS 1 : Flip = IN2P is pulled to AVSS and IN2N is pulled to AVDD
0	LOFF_FLIP1	R/W	0h	Channel 1LOFF polarity reversal Flip the pull-up or pull-down polarity of the current source on channel 1 to detect lead disconnection. 0 : No flip = IN1P is pulled to AVDD and IN1N is pulled to AVSS 1 : Flip = IN1P is pulled to AVSS and IN1N is pulled to AVDD

LOFF_STATP: Lead positive terminal status register (address=12h) (reset=00h)

This register stores the status of whether the positive terminal of each channel has detached. See the Lead Detection section for details. The LOFF_STATP value is ignored if the corresponding LOFF_SENSP bit is not set to 1.

LOFF_STATP: Lead positive terminal status register (read-only)

7	6	5	4	3	2	1	0
IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

13. Description of the fields in the positive lead status register

Bit	Fields	Type	Reset	Description
1	IN2P_OFF	R	0h	Channel 2 positive terminal lead status, IN2P electrode conduction or disconnection status 0 : Electrode conduction 1 : Electrode detachment
0	IN1P_OFF	R	0h	Channel 1 positive terminal lead status, IN1P electrode conduction or disconnection status 0 : Electrode conduction 1 : Electrode detachment

LOFF_STATN: Negative lead status register (address=13h) (reset=00h)

This register stores the status of whether the negative terminal of each channel has detached. See the Lead Detection section for details. The LOFF_STATP value is ignored if the corresponding LOFF_SENSP bit is not set to 1.

LOFF_STATN: Lead negative terminal status register (read-only)

7	6	5	4	3	2	1	0
IN8N_OFF	IN7N_OFF	IN6N_OFF	IN5N_OFF	IN4N_OFF	IN3N_OFF	IN2N_OFF	IN1N_OFF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

14. Description of the fields in the negative lead status register

Bit	Fields	Type	Reset	Description
1	IN2N_OFF	R	0h	Channel 2 Negative Terminal Lead Status IN2N Electrode On/ Off Status 0 : Electrode conduction 1 : Electrode detachment
0	IN1N_OFF	R	0h	Channel 1 Negative terminal lead status IN1N Electrode conduction or disconnection status 0 : Electrode conduction 1 : Electrode detachment

GPIO: General Purpose I/O Register (Address = 14h) (Reset = 0Fh)

This register controls the behavior of the GPIO pins.

GPIO: General Purpose I/O Registers

7	6	5	4	3	2	1	0
		GPIOD[2 :1]				GPIOC [2 :1]	
R/W-0h				R/W-Fh			

Note : R/W = Read/Write; R = Read Only; -n = Reset value

15. Description of General - Purpose I/O Register Fields

Bit	Fields	Type	Reset	Description
7:6	Reserved	R/W	0h	Reserved
5 :4	GPIOD[2:1]	R/W	0h	GPIO Data . These bits are used to read and write data to the GPIO port. When reading the register, the returned data corresponds to the state of the external GPIO pin, regardless of whether it is programmed as an input or output. As an output, writing to GPIOD sets the output value. As an input, writing to GPIOD has no effect.
3:2	Reserved	R/W	3h	Reserved
1 :0	GPIOC[2:1]	R/W	3h	GPIO control (corresponding) These bits determine whether the corresponding GPIOD pin is an input or an output. 0 : Output 1 : Input

PACE : PACE Select Register (address=15h) (reset=00h)

This register selects the channel driving the PACE pin.

PACE : PACE selection register

7	6	5	4	3	2	1	0
0	0	SRB1	00		PACE_SEL		PD_PACE_b
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

16. Miscellaneous 1.Register Field Description

	Fields	Type	Reset	Description
7:6	Reserved	R/W	0h	Reserved. Always write 0h
5	SRB1	R/W	0h	Enable SRB1. This bit controls the connection between SRB1 and channel N. 0: Disable SRB1 function 1: Enable SRB1 function
4:3	Reserved	R/W	0h	Reserved.
2:1	PACE_SEL	R/W	0h	PACE Channel Selection. Controls the selection of the channel driving the PACE. x0: Select channel 1 x1: Select Channel 2
0	PD_PACE_b	R/W	0h	PACE circuit switch. 0: PACE circuit is not working 1: PACE circuit operation

RESP: Respiratory Control Register (Address =16h) (Reset =00h)

This register is the respiratory control register.

RESP : Respiratory Control Register

7	6	5	4	3	2	1	0
RESP_DEMOD_EN	RESP_MOD_EN	0	RESP_PH			RESP_CTRL	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

17. Miscellaneous 2 Register Field Description

Bit	Fields	Type	Reset	Description
7	RESP_DEMOD_EN	R/W	0h	Enables the breathing demodulation circuitry . This bit enables and disables the demodulation circuitry on channel 1. 0 = RESP demodulation circuit off 1 = RESP demodulation circuit enabled
6	RESP_ MOD_EN	R/W	0h	Enable breathing modulation circuitry. This bit enables and disables the modulation circuitry on channel 1. 0 = RESP modulation circuit off 1 = RESP modulation circuit enabled
5	Reserved	R/W	0h	Reserved.
4:2	RESP_PH[2:0]	R/W	0h	respiratory phase 000 = 22.5° 001 = 45° 010 = 67.5° 011 = 90° 100 = 112.5° 101 = 135° 110 = 157.5° 111 = Not applicable
1:0	RESP_CTRL[1:0]	R/W	0h	Breathing control ; these bits set the mode of the breathing circuit. 00 = No breathing 01 = External breathing 10 = Internal breathing with internal signals 11 = Internal breathing with user-generated signals

CONFIG4 : Configuration Register 4 (Address =17h) (Reset =00h)

This register configures the conversion mode and enables the lead detection comparator.

CONFIG4: Configuration Register 4

7	6	5	4	3	2	1	0
RESP_FREQ			0	SINGLE_SHOT	0	PD_LOFF_COMP_	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Note : R/W = Read/Write; R = Read Only; -n = Reset value

18. Description of the 4 fields of the configuration register

Bit	Fields	Type	Reset	Description
7: 5	RESP_FREQ	R/W	0h	When RESP_CTRL[1:0]=10 or RESP_CTRL[1:0]=0 or 1, these bits control the breathing control frequency. 000 = 64kHz modulation clock 001 = 32kHz modulation clock 010 = 16kHz square wave on GPIO 1 011 = 8kHz square wave on GPIO 1 4kHz square wave on GPIO 1 101 = 2kHz square wave on GPIO 1 110 = 1kHz square wave on GPIO 1 111 = 500Hz square wave on GPIO 1 Modes 000 and 001 are the modulation frequencies for internal and external breathing modes, respectively. In internal breathing mode, control signals appear on the RESP_MODP and RESP_MODN terminals. All other bit settings generate a square wave on GPIO 1 as described above.
4	Reserved	R/W	0h	Reserved.
3	SINGLE_SHOT	R/W	0h	Single -shot conversion selection. This bit sets the conversion mode. 0 : Continuous conversion mode 1 : Single-shot mode
2	Reserved	R/W	0h	Reserved.
1	PD_LOFF_COMP_	R/W	0h	The lead detection comparator is powered off . This bit turns off the power to the lead detection comparator. 0 : Lead detection comparator disabled 1 : Lead detection comparator enabled
0	Reserved	R/W	0h	Reserved.

14. Application Description and Packaging

- **Breathing Measurement Instructions**

The DADS1292 uses out-of-band amplitude modulation and demodulation to measure changes in chest impedance corresponding to respiration. When respiratory mode is enabled, channel 1 cannot be used to acquire physiological signals because the internal demodulation circuitry is occupied. Physiological signals can still be acquired using the same electrode used for respiratory measurements, simply by connecting that electrode to another channel simultaneously, as shown in Figure 4. Note the configuration shown in the figure.

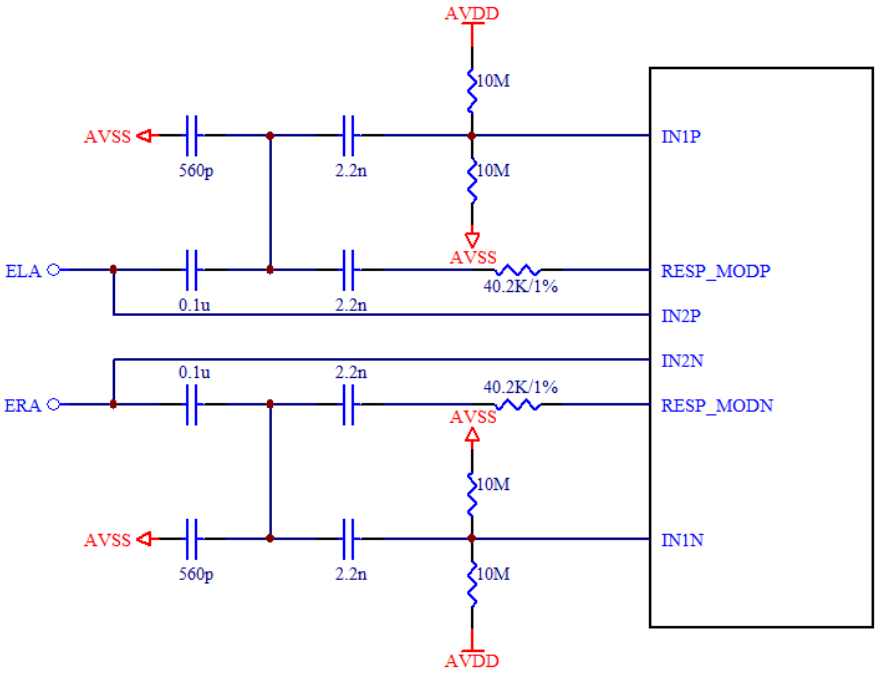


Figure 4. Typical breathing circuit

- **Chip power connection**

The DADS1292 chip can be connected to a single-pole or bipolar power supply for analog power, and supports 1.8V~3.6V for digital power.

1) Connect to a single-pole (3~5V) power supply

Figure 5 illustrates the DADS1292 connected to a single-pole power supply. In this example, the analog power supply (AVDD) is referenced to analog ground (AVSS), and the digital power supply (DVDD) is referenced to digital ground (DGND). (Note: The power supply, reference, and capacitors VCAP1 through VCAP4 should be placed as close to the package as possible.)

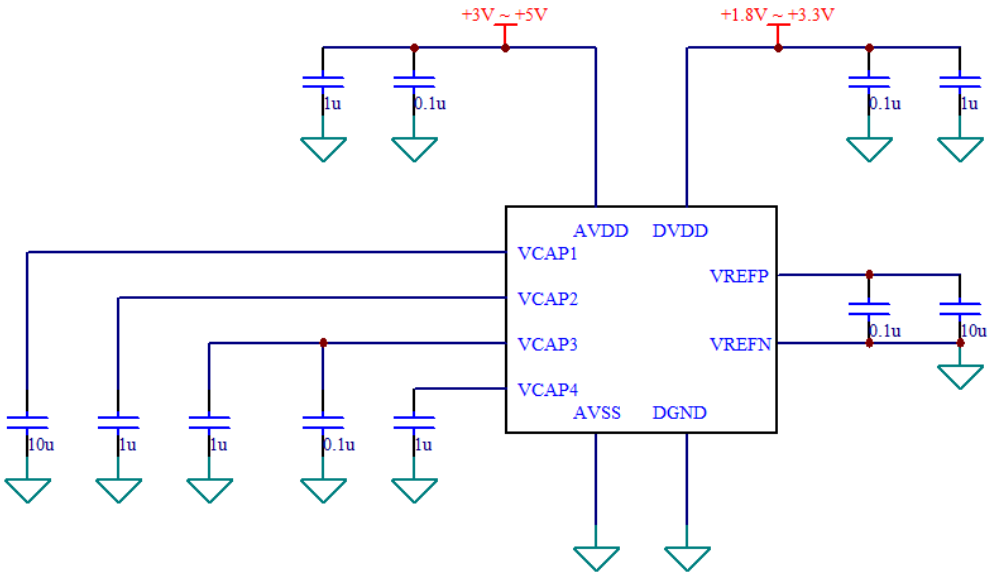


Figure 5. Single power supply

2) Connect to a bipolar (±1.5~±2.5) power supply

Figure 6 illustrates the DADS1292 connected to a bipolar power supply . In this example, the analog power supply is connected to the device analog power supply (AVDD). This power supply is referenced to the device analog loop (AVSS), and the digital power supply (DVDD) is referenced to the device digital ground loop (DGND). (Note: The power supply, reference, and capacitors VCAP1 through VCAP4 should be placed as close to the package as possible.)

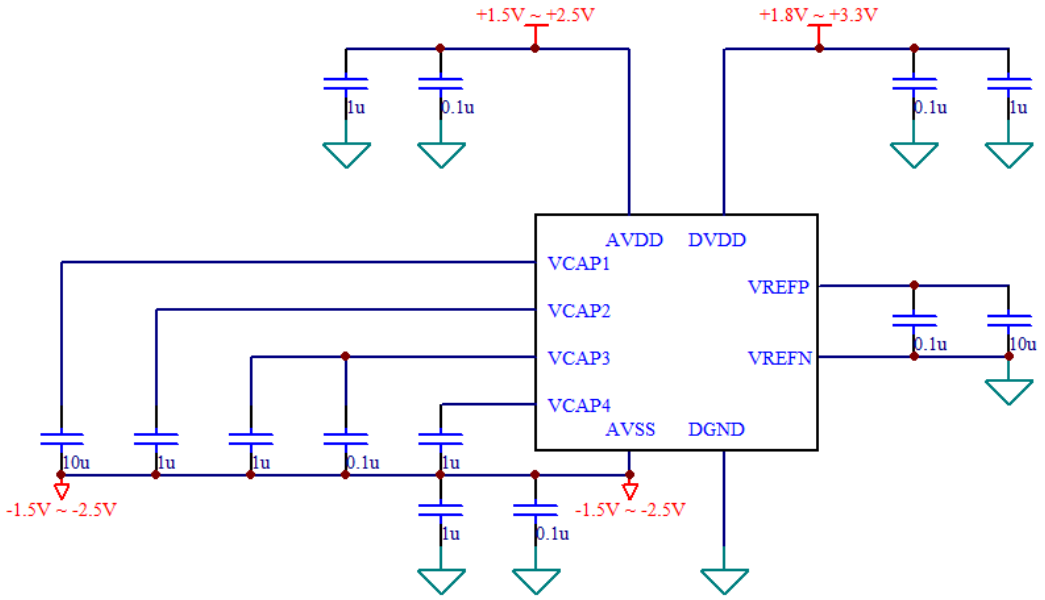


Figure 6. Bipolar power supply

15. Package Dimensions

External dimensions

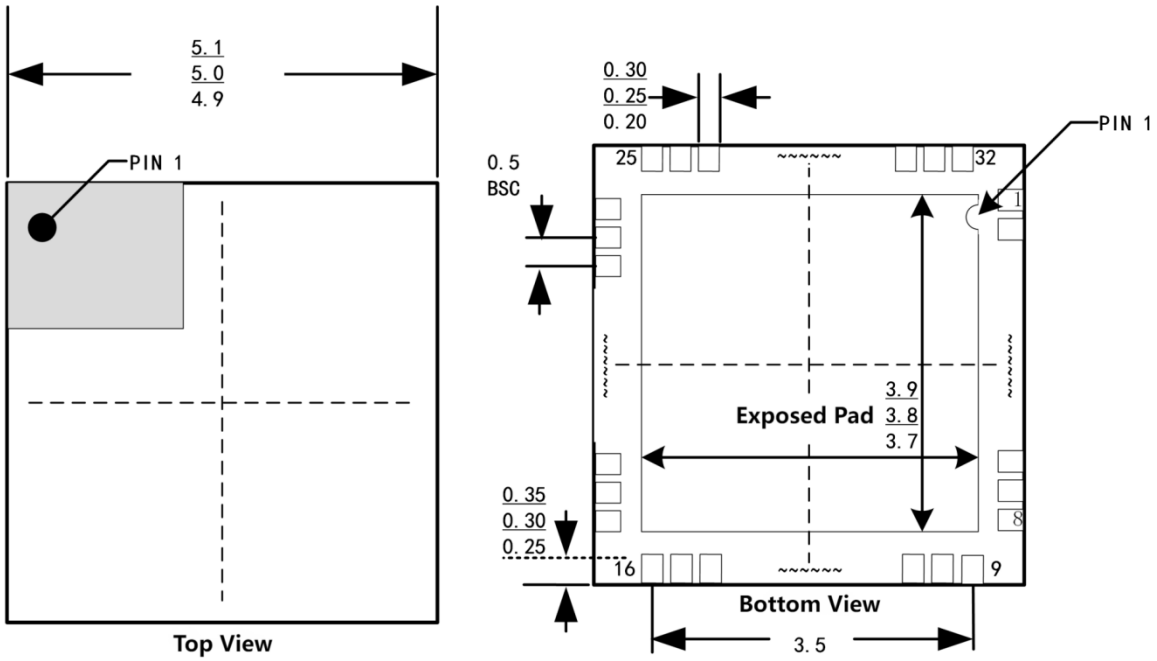


Figure 7. QFN32 package dimensions

16. Ordering Guide

Model	Temperature Range	Packaging Type	Package Quantity
DADS1292	-40 °C to +85°C	QFN32	490/Reel