FEATURES

- Simultaneously Measure Four/Eight Channels
- Up to 144kSPS Data Rate
- AC Performance:
  - 70kHz Bandwidth
  - 111dB SNR (High-Resolution Mode)
  - –108dB THD
- DC Accuracy:
  - 0.8μV/°C Offset Drift
  - 1.3ppm/°C Gain Drift
- Selectable Operating Modes:
  - High-Speed: 144kSPS, 106dB SNR
  - High-Resolution: 52kSPS, 111dB SNR
  - Low-Power: 52kSPS, 31mW/ch
  - Low-Speed: 10kSPS, 7mW/ch
- Linear Phase Digital Filter
- SPI™ or Frame-Sync Serial Interface
- Low Sampling Aperture Error
- Modulator Output Option (digital filter bypass)
- Analog Supply: 5V
- Digital Core: 1.8V
- I/O Supply: 1.8V to 3.3V

APPLICATIONS

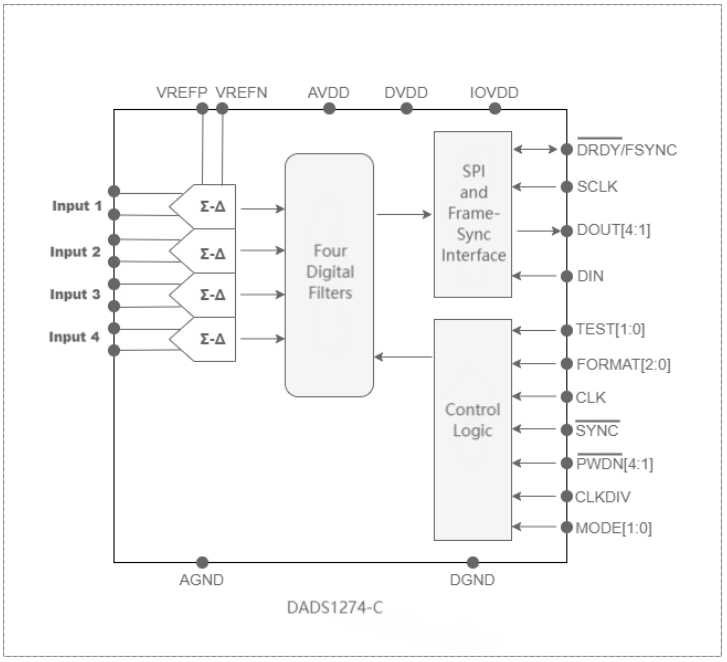
- Vibration/Modal Analysis
- Multi-Channel Data Acquisition
- Acoustics/Dynamic Strain Gauges
- Pressure Sensors

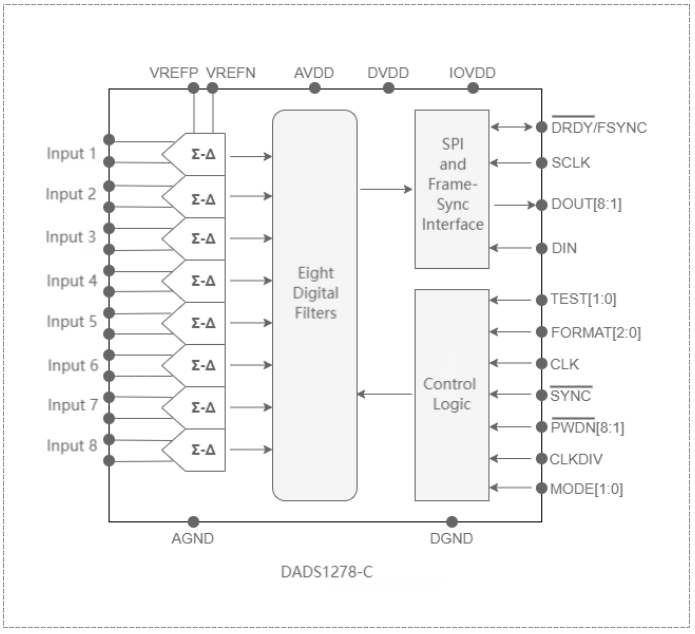
DESCRIPTION

The DADS1274-C (4-channel) and DADS1278-C (8-channel) are 24-bit, delta-sigma (Δ-Σ) analog-to-digital converters (ADCs) capable of up to 144k samples per second (SPS), allowing for simultaneous sampling of 4 or 8 channels. The chips are housed in the same package and are scale-down compatible. These high-resolution ADCs offer large usable bandwidth for audio applications, but with significantly lower offset and drift than comparable industrial products. The DADS1274-C and DADS1278-C are suitable for high-precision industrial measurements requiring stringent DC and AC specifications.

A high-order steady-state chopper regulator achieves very low drift and in-band noise. An on-chip decimation filter suppresses out-of-band noise. The ADC provides up to 90% of the Nyquist rate of usable signal bandwidth with in-band ripple less than 0.005dB.

Four operating modes allow users to balance speed, resolution, and power consumption. All operations are directly controlled by the pins, eliminating the need for programming registers. The chips are suitable for the entire industrial temperature range (-40°C to +85°C). The chip uses a TQFP-64 package.





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Absolute Maximum Rating

Unless otherwise stated, operate within the room temperature range [1].

		DADS1274-C, DADS1278-C	unit
AVDD to AGND		-0.3 to +6.0	V
DVDD, IOVDD to DGND		-0.3 to +3.6	V
AGND to DGND		-0.3 to +0.3	V
Input current	Momentary	100	mA
	Continuous	10	mA
Analog input to AGND		-0.3 to AVDD + 0.3	V
Digital input or output to DGND		-0.3 to IOVDD + 0.3	V
Maximum welding temperature		+150	°C
Operating temperature range	DADS1274-C	-40 to +125	°C
	DADS1278-C	-40 to +105	°C
Storage temperature range		-60 to +150	°C

Stress exceeding these ratings may cause permanent damage. Prolonged exposure to absolute maximum conditions may reduce the reliability of the equipment. These are only stress ratings and do not imply functional operation of the equipment under these conditions or any other conditions exceeding the specified limits.

Electrical Characteristics

All specifications at T_A= -40 °C to +105°C, AVDD=+5V, DVDD=+1.8V, IOVDD=+3.3V, f_{CLK} = 27MHz, VREFP=2.5V, VREFN=0V, and all channels are active unless otherwise specified.

Parameter		Test conditions	DADS1274-C, DADS1278-C			Unit
			MIN	TYP	MAX	
Analog Inputs						
Full-scale input voltage (FSR (1))		V_{IN} = (AINP – AINN)		±V_{REF}		V
Maximum input voltage		AINP or AINN to AGND	AGND – 0.1		AVDD + 0.1	V
Common-mode input voltage (V_{CM})		VCM = (AINP + AINN)/2		2.5		V
Differential input impedance	High-speed mode (2)			14		kΩ
	High resolution mode			14		kΩ
	Low power mode			28		kΩ
	Low speed mode			140		kΩ
DC characteristics						
		Data resolution	24			Bits
Data rate (f_{DATA})	High-speed mode	f_{CLK} = 37MHz		144,531		SPS (3)
		f_{CLK} = 32.768MHz		128,000		SPS
		f_{CLK} = 27MHz		105,469		SPS
	High resolution mode			52,734		SPS
	Low power mode			52,734		SPS
	Low speed mode			10,547		SPS
Integral nonlinearity (INL) (4)		Differential input V_{CM} =2.5V		±0.0003	±0.0012	% FSR (1)
DC error				0.25	2	mV
DC deviation temperature drift				0.8		μV/°C
Gain error				0.1	0.5	% FSR
Gain Temperature Drift				1.3		ppm/°C
noise	High-speed mode	Input shorting		8.5	16	μV, rms
	High resolution mode	Input shorting		5.5	12	μV, rms
	Low power mode	Input shorting		8.5	16	μV, rms
	Low speed mode	Input shorting		8.0	16	μV, rms
Common-mode suppression		f CM = 60Hz	90	108		dB
Power supply suppression	AVDD	f PS = 60Hz		80		dB
	DVDD			85		dB
	IOVDD			105		dB
V_{COM} output voltage		Unloaded		AVDD/2		V

(1) FSR = Full amplitude range = 2V_{REF}
(2) For the high-speed mode, the maximum value f_{CLK} = 37MHz , and for other modes, the maximum value is 27MHz.
(3) SPS = sampling rate per second.
(4) Best-fit algorithm.

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Electrical Characteristics (continued)

All specifications at T_A= -40 °C to +105°C, AVDD=+5V, DVDD=+1.8V, IOVDD=+3.3V, f_{CLK} = 27MHz, VREFP=2.5V, VREFN=0V, and all channels are active unless otherwise specified.

Parameter		Test conditions	DADS1274-C, DADS1278-C			Unit
			MIN	TYP	MAX	
Communication characteristics						
		f=1kHz, -0.5dBFs (5)		-107		dB
Signal-to-noise ratio (SNR) (6)	High-speed mode		101	106		dB
	High resolution mode	V_{REF} = 2.5V	103	110		dB
		V_{REF} = 3V		111		dB
	Low power mode		101	106		dB
	Low speed mode		101	107		dB
Total Harmonic Distortion (THD) (7)		V_{IN} = 1kHz, –0.5dBFS		-108	-96	dB
Stray dynamic range				109		dB
Passband ripple				±0.005		dB
Passband				0.453f_{DATA}		Hz
-3dB bandwidth				0.49f_{DATA}		Hz
With external mourning reduction	High resolution mode		95			dB
	Other modes		100			
Cutoff frequency	High resolution mode		0.547 f_{DATA}		127.453f_{DATA}	Hz
	Other modes		0.547 f_{DATA}		63.453 f_{DATA}	Hz
Group delay	High resolution mode			39/f_{DATA}		s
	Other modes			38/f_{DATA}		s
Establishment time (lag time)	High resolution mode	Completed		78-C/f_{DATA}		s
	Other modes	Completed		76/f_{DATA}		s
Reference Input						
Negative Reference Input (VREFN)			AGND – 0.1		AGND + 0.1	V
Reference input voltage (V_{REF}) (8) (V_{REF} = VREFP - VREFN)		0.1 ≤ f_{CLK} ≤ 27MHz	0.5	2.5	3.1	V
		27 < f_{CLK} ≤ 32.768MHz	0.5	2.5	2.6	V
		32.768MHz < f_{CLK} ≤ 37MHz	0.5	2.048	2.1	V
DADS1274-C Reference Input Impedance	High-speed mode			1.3		kΩ
	High resolution mode			1.3		kΩ
	Low power mode			2.6		kΩ
	Low speed mode			13		kΩ
DADS1278-C Reference Input Impedance	High-speed mode			0.65		kΩ
	High resolution mode			0.65		kΩ
	Low power mode			1.3		kΩ
	Low speed mode			6.5		kΩ
Digital input/output (IOVOO = 1.8V to 3.6V)						
V_{IH}			0.7 IOVDD		IOVDD	V
V_{IL}			DGND		0.3 IOVDD	V
V_{OH}		I_{OH} = 4mA	0.8 IOVDD		IOVDD	V
VOL		I_{OL} = 4mA	DGND		0.2 IOVDD	V
Digital port input leakage		0 < $V_{IN\ DIGITAL}$ < IOVDD			±10	μA
Master clock rate (f_{CLK})		High-speed mode(8)	0.1		37	MHz
		Other modes	0.1		27	MHz

(5) Worst-case channel crosstalk between one or more channels.
(6) The minimum signal-to-noise ratio is guaranteed by the limitation of DC noise characteristics.
(7) THD includes the first 9 harmonics of the input signal; low speed mode includes the first 5 harmonics.
(8) f_{CLK} is a maximum of 37MHz for high-speed mode and a maximum of 27 MHz for all other modes.

Electrical Characteristics (continued)

All specifications at T_A= -40 °C to +105°C, AVDD=+5V, DVDD=+1.8V, IOVDD=+3.3V, f_{CLK} = 27MHz, VREFP=2.5V, VREFN=0V, and all channels are active unless otherwise specified.

Parameter		Test conditions	DADS1274-C, DADS1278-C			Unit
			MIN	TYP	MAX	
Power supply						
AVDD			4.75	5	5.25	V
DVDD (9)		0.1 ≤ f_{CLK} ≤ 32.768MHz	1.65	1.8	1.95	V
		32.768MHz < f_{CLK} ≤37MHz	2.0	2.1	2.2	V
IOVDD			1.65		3.6	V
Cut off current	AVDD			1	10	μA
	DVDD			1	15	μA
	IOVDD			1	10	μA
DADS1274-C						
DADS1274-C AVDD current	High-speed mode			50	75	mA
	High resolution mode			50	75	mA
	Low power mode			23	35	mA
	Low speed mode			5	9	mA
DADS1274-C DVDD current	High-speed mode			18	24	mA
	High resolution mode			12	17	mA
	Low power mode			10	15	mA
	Low speed mode			2.5	4.5	mA
DADS1274-C IOVDD current	High-speed mode			0.15	0.5	mA
	High resolution mode			0.075	0.3	mA
	Low power mode			0.075	0.3	mA
	Low speed mode			0.02	0.15	mA
DADS1274-C Power consumption	High-speed mode			285	420	mW
	High resolution mode			275	410	mW
	Low power mode			135	210	mW
	Low speed mode			30	55	mW
DADS1278-C						
DADS1278-C AVDD current	High-speed mode			121.25	181.25	mA
	High resolution mode			121.25	181.25	mA
	Low power mode			55	80	mA
	Low speed mode			11.25	17.5	mA
DADS1278-C DVDD current	High-speed mode			23	30	mA
	High resolution mode			16	20	mA
	Low power mode			12	17	mA
	Low speed mode			2.5	4.5	mA
DADS1278-C IOVDD current	High-speed mode			0.25	1	mA
	High resolution mode			0.125	0.5	mA
	Low power mode			0.125	0.5	mA
	Low speed mode			0.035	0.2	mA
DADS1278-C Power consumption	High-speed mode			636	942	mW
	High resolution mode			618	918	mW
	Low power mode			294	426	mW
	Low speed mode			60	96	mW

(9) For high-speed mode, the maximum value fCLK <= 37MHz, and for other modes, the maximum value is 27MHz.

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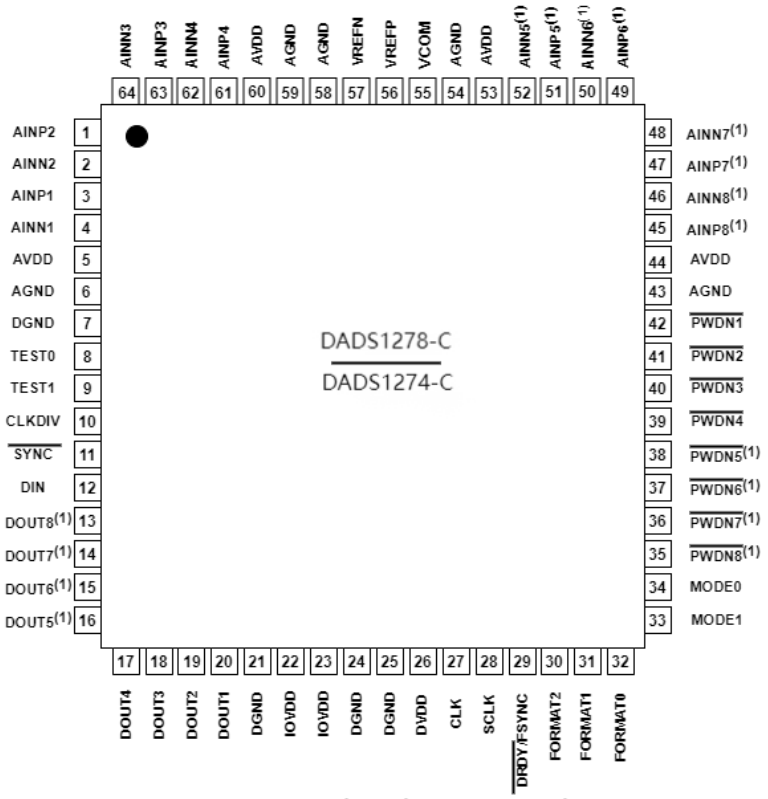


DADS1278-C/DADS1274-C Pin Assignments(Top View)-TQFP64

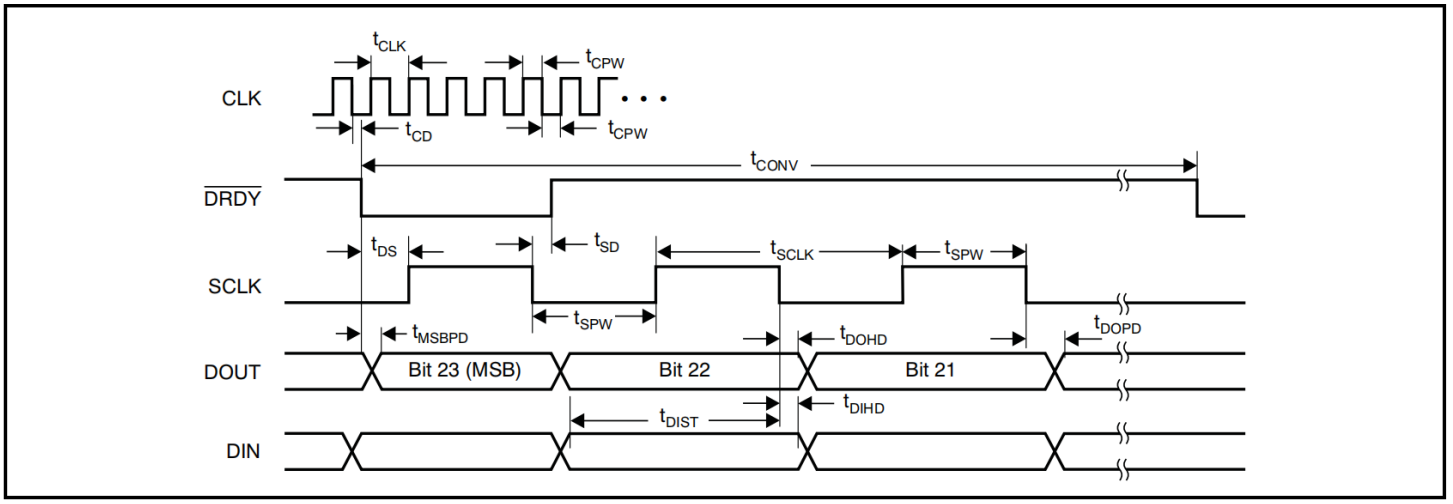
DADS1274-C/DADS1278-C Pin Definitions

Pin		Function	Description
Name	No.		
AGND	6, 43, 54, 58, 59	Analog ground	Analog ground; using a single plane connected to DGND
AINP1	3	Analog Input	DADS1278-C: AINP[B:1] Positive analog input, channels 1 to 8. DADS1274-C: AINP[B:5] is connected to the internal ESD conductor and must be left floating. AINP[4:1] is the negative terminal of the analog input, channels 1 to 4.
AINP2	1	Analog Input	
AINP3	63	Analog Input	
AINP4	61	Analog Input	
AINP5	51	Analog Input	
AINP6	49	Analog Input	
AINP7	47	Analog Input	
AINP8	45	Analog Input	
AINN1	4	Analog Input	DADS1278-C: AINP[B:1] Negative terminal of analog input, channels 1 to 8 DADS1274-C: AINP[8:5] is connected to the internal ESD conductor and must be floating. AINP[4:1] is the negative terminal of the analog input, channels 1 to 4.
AINN2	2	Analog Input	
AINN3	64	Analog Input	
AINN4	62	Analog Input	
AINN5	52	Analog Input	
AINN6	50	Analog Input	
AINN7	48	Analog Input	
AINN8	46	Analog Input	

DADS1274-C/DADS1278-C Pin Definitions (Continued)

AVDD	5, 44, 53, 60	Analog power supply	Analog power supply (4.75V to 5.25V)
VCOM	55	Analog output	AVDD/2 Unbuffered Voltage Output
VREFN	57	Analog Input	Reference power input negative terminal
VREFP	56	Analog Input	Reference power input positive terminal
CLK	27	Digital input	Master clock input (f_{CLK})
CLKDIV	10	Digital input	CLK input drive control: 1 = 37MHz (high-speed mode) / others 27MHz 0 = 13.5MHz (low power) / 5.4MHz (low speed)
DGND	7,21,24, 25	Digital ground	Digital ground power supply
DIN	12	Digital input	Daisy chain Digital input
DOUT1	20	Digital output	DOUT1 is the TDM data output (TDM mode) DADS1278-C: DOUT[8:1] Data output from channel 8 to 1 DADS1274-C: DOUT[8:5] is internally connected to an active circuit DOUT[4:1] Channel 4 to 1 data output
DOUT2	19	Digital output	
DOUT3	18	Digital output	
DOUT4	17	Digital output	
DOUTS	16	Digital output	
DOUT6	15	Digital output	
DOUT7	14	Digital output	
DOUT8	13	Digital output	
$\overline{\text{DRDY}}$/FSYNC	29	Digital Input/Output	Frame synchronization protocol: frame clock input; SPI protocol: data ready output.
DVDD	26	Digital power supply	Digital Core Power
FORMAT0	32	Digital input	FORMAT[2:0] selects frame synchronization/SPI protocol, TDM/discrete data output, fixed/dynamic position TDM data, and modulator mode/normal operation mode.
FORMAT1	31	Digital input	
FORMAT2	30	Digital input	
IOVDD	22,23	Digital power supply	I/O power supply (+1.65V to +3.6V)
MODE0	34	Digital input	MODE[1:0] selects high-speed, high-resolution, low-power, or low-speed operating modes.
MODE1	33	Digital input	
$\overline{\text{PWDN1}}$	42	Digital input	DADS1278-C:PWDN[8:1] Power-off control for channels 1 to 8. DADS1274-C: PWDN[8:5] must be 0V, PWDN[4:1] channels 1 to 4 are power-off controlled.
$\overline{\text{PWDN2}}$	41	Digital input	
$\overline{\text{PWDN3}}$	40	Digital input	
$\overline{\text{PWDN4}}$	39	Digital input	
$\overline{\text{PWDN5}}$	38	Digital input	
$\overline{\text{PWDN6}}$	37	Digital input	
$\overline{\text{PWDN7}}$	36	Digital input	
$\overline{\text{PWDN8}}$	35	Digital input	
SCLK	28	Digital Input/Output	Serial clock input, modulator clock output
$\overline{\text{SYNC}}$	11	Digital input	Synchronization signal input (all channels).
TEST0	8	Digital input	TEST[1:0] Test mode selection: 00=Normal operation 01=Not used 11=Test mode 10 = Not used
TEST1	9	Digital input	

SPI Format Timing



T_A = –40 °C to +105 °C, IOVDD = 1.65V to 3.6V, and DVDD = 1.65V to 1.95V, unless otherwise specified.

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{CLK}	CLK period ($1/f_{CLK}$) (1)	37		10,000	ns
t_{CPW}	CLK pulse width	15			ns
t_{CONV}	Conversion period ($1/f_{DATA}$) (2)	256		2560	t_{CLK}
t_{CD} (3)	CLK to $\overline{DRDY}$ falling edge time		22		ns
t_{DS} (3)	Data retrieval time from the falling edge of DROY to the rising edge of SCLK	1			t_{CLK}
t_{MSBPD}	$\overline{DRDY}$ Falling edge to DOUT MSB effective time (propagation delay)			16	ns
t_{SD} (3)	SCLK Falling edge to $\overline{DRDY}$ rising edge time		18		ns
t_{SCLK} (4)	SCLK cycle	1			t_{CLK}
t_{SPW}	SCLK pulse width	0.4			t_{CLK}
t_{DOHD} (3)(5)	The SCLK falling edge to the new DOUT is invalid (duration).	10			ns
t_{DOPD} (3)	SCLK falling edge to new DOUT valid (propagation delay)			32	ns
				26	ns (4)
t_{DIST}	The new DIN is valid for the falling edge of SCLK (setup time).	6			ns
t_{DIHD} (5)	The old DIN parameter was effective on the falling edge of SCLK (duration time).	6			ns

(1) f_{CLK} = 27MH maximum value.

(2) Depends on MODE[1:0] and CLKDIV options.

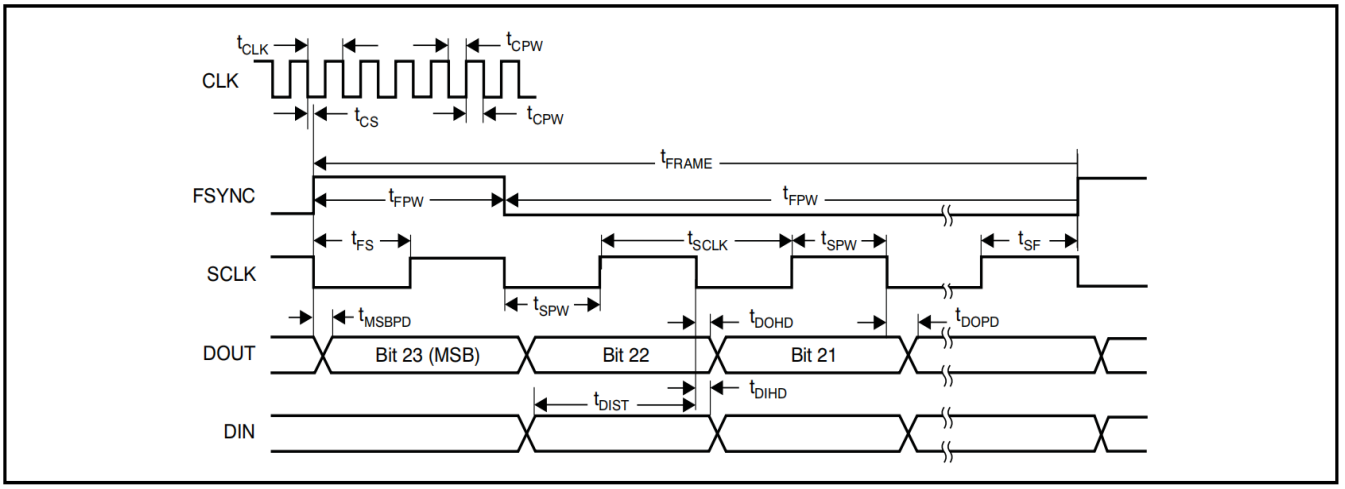
(3) $\overline{DRDY}$ and the load of DOUT = 20pF

(4) For optimal performance, the f_{SCLK} / f_{CLK} ratio is limited to 1, 1/2, 1/4, 1/8, etc.

(5) t_{DOHD} (DOUT duration) and t_{DIHD} (DIN duration) are derived based on worst-case scenarios (digital power supply voltage and environment). Under the same conditions, with DOUT directly connected to DIN, the time edge is >4ns.

(6) DOUT1, TDM mode, IOVDD=3.15V to 3.45V, while DVDD=1.7V to 1.9V.

Frame-Sync Format Timing



T_A = –40 °C to +105 °C, IOVDD = 1.65V to 3.6V, and DVDD = 1.65V to 2.2V, unless otherwise specified .

Symbol	Parameter		MIN	TYP	MAX	Unit
t_{CLK}	CLK period ($1/f_{CLK}$)	High-speed mode	27		10,000	ns
		Other modes	37		10,000	ns
t_{CPW}	CLK pulse width		11			ns
t_{CS}	Time from CLK falling edge to SCLK falling edge		-0.25		0.25	t_{CLK}
t_{FRAME}	Frame period ($1/f_{DATA}$) (1)		256		2560	t_{CLK}
t_{FPW}	FSYNC Pulse Width		1			t_{SCLK}
t_{FS}	Time from FSYNC rising edge to SCLK rising edge		5			ns
t_{SF}	Time from SCLK rising edge to FSYNC rising edge		5			ns
t_{SCLK}	SCLK cycle (2)		1			t_{CLK}
t_{SPW}	SCLK Pulse Width		0.4			t_{CLK}
t_{DOHD} (3)(4)	SCLK falling edge to previous DOUT failure time (duration time)		10			ns
t_{DOPD} (4)	The effective time from the falling edge of SCLK to the next DOUT (propagation delay)				31	ns
					21	ns (5)
					25	ns (6)
t_{MSBPD}	The effective time (propagation delay) from the rising edge of FSYNC to DOUT MSB.				31	ns
					21	ns (5)
					25	ns (6)
t_{DIST}	The new DIN is valid for the falling edge of SCLK (setup time).		6			ns
t_{DIHD} (3)	The old DIN parameter was effective on the falling edge of SCLK (duration time).		6			ns

(1) Depends on MODE[1:0] and CLKDIV options.

(2) SCLK must run continuously and the ratio of SCLK to fcU< is limited to 1, 1/2, 1/4, and 1/8.

(3) t_{DOHD} (DOUT duration) and t_{DIHD} (DIN duration) are derived based on worst-case scenarios (digital power supply voltage and environment). Under the same conditions, when DOUT is directly connected to DIN, the time edge is >4ns.

(4) Load on DOUT = 20pF.

(5) DOUT1, TDM mode, IOVDD=3.15V to 3.45V, while DVDD=2V to 2.2V.

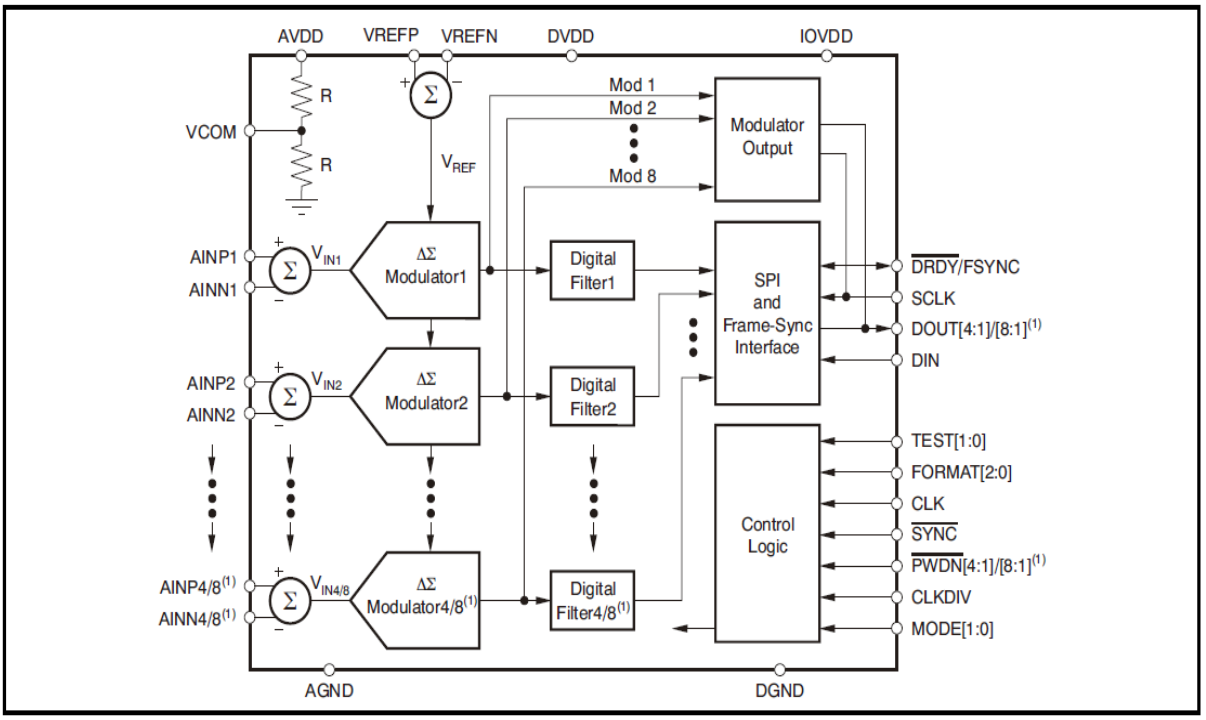
(6) DOUT1, TDM mode, IOVDD=3.15V to 3.45V, while DVDD=1.7V to 1.9V.

Overview

The DADS1274-C (quad-channel) and DADS1278-C (eight-channel) are 24-bit ADCs based on a delta-sigma (Δ-Σ) architecture. They offer a superior combination of DC and AC performance. The block diagram of the chip is shown below. Note that the two devices are functionally identical, except that the DADS1274-C has four ADCs and the DADS1278-C has eight. The packages are identical, and the DADS1274-C is pin-compatible with the DADS1278-C, allowing for hardware compatibility. The converter consists of four (DADS1274-C) or eight (DADS1278-C) sixth-order (Δ-Σ) and low-ripple linear-phase FIR filters. The modulator measures the differential input signal V_{IN} = (AINP – AINN) and the differential reference V_{REF} = (VREFP – VREFN). The digital filters receive the modulator signal and provide a low-noise digital output. To balance speed, resolution, and power, four operating modes are supported: high speed, high resolution, low power, and low speed. The table below summarizes the performance of each mode. In high-speed mode, the maximum data rate is 144kSPS. In high-resolution mode, SNR=111dB (V_{REF} =3.0V); in low-power mode, power consumption is only 31mW/channel; in low-speed mode, power consumption at 10.5kSPS is only 7mW/channel. Users can also bypass the digital filter and directly access the modulator output.

The DADS1274-C/78-C is configured by simply setting the appropriate I/O pins, without the need for register programming. It supports SPI and serial port data retrieval in synchronous frame formats. With daisy-chain outputs and external synchronization capabilities, the DADS1274-C/78-C can be easily used in systems requiring eight or more channels.

DADS1274-C/DADS1278-C Block Diagram (reference)



(1) DADS1274-C has four channels; DADS1278-C has eight channels.

Table 2. Summary of Operating Mode Characteristics

Model	Max data rate (SPS)	Bandwidth (kHz)	SNR (dB)	Noise (μV_{RMS})	Power/channel (mW)
High-speed mode	144,531	65,472	106	8.5	70 (1)
High resolution mode	52,734	23,889	110	5.5	64
Low power mode	52,734	23,889	106	8.5	31
Low speed mode	10,547	4,798	107	8.0	7

(1) The value is specified as 105 kSPS.

Function Description

The DADS1274-C/78-C is a (Δ-Σ) ADC consisting of four or eight independent converters that acquire the input signal in parallel. The converter comprises two main functional blocks for performing the ADC conversion: a modulator and a digital filter. The modulator samples the input signal and a reference voltage simultaneously to produce a digital output signal. The density of digital code flips is proportional to the analog input level relative to the reference voltage. The pulse stream is filtered by an internal digital filter, which produces the output conversion result. In operation, the modulator samples the input signal at a high rate (typically 64x higher than the final output data rate). The modulator's quantization noise is shifted to a higher frequency range, which is removed by the internal digital filter. Oversampling results in very low noise levels within the signal passband. Because the input signal is sampled at a very high rate, input signal aliasing does not occur until the input signal frequency is at the modulator's sampling rate. Due to the high modulator sampling rate, this architecture greatly relaxes the requirements for external anti-aliasing filters.

Sampling Aperture Matching

The DADS1274-C/78-C converter operates from the same CLK input. The CLK input controls the timing of the modulator sampling instant. The converter is designed to control the sampling skew or modulator sampling aperture matching between channels. Furthermore, the digital filters are synchronized to begin the convolution phase at the same modulator clock cycle. This design ensures good phase matching between DADS1274-C/78-C channels. The phase matching of one 4-channel DADS1274-C may not have the same degree of sampling matching as another DADS1274-C (eight or more channels in total). Due to manufacturing variations, the resulting differences in internal clock signal coupling and the external CLK signal with each chip can cause significant sampling matching errors. Using a CLK tracker of the same length or an external clock distribution chip can be used to reduce inter-chip sampling matching errors.

Frequency Response

The digital filter establishes the overall frequency response. The filter employs a multi-stage FIR topology to provide minimal passband ripple and a linear phase with high cutoff frequency attenuation. The oversampling rate of the digital filter (i.e., the ratio of the modulator sample rate to the output data rate, or fMOD / fDATA) is an optional mode function.

Table 3. Oversampling rate comparison

Model	Oversampling ratio (f_{MOD} / f_{DATA})
high speed	64
High resolution	128
Low power consumption	64
low speed	64

Table 4. High -speed mode f_{CLK} case

f_{CLK} (MHz)	V_{REF} (V)	DVDD (V)	interface
$0.1 \le f_{CLK} \le 27$	0.5 to 3.1	1.65 to 1.95	Synchronization frame or SPI
$27 < f_{CLK} \le 32.768$	0.5 to 2.6	1.65 to 1.95	Synchronization Frame
$32.768 < f_{CLK} \le 37$	0.5 to 2.1	Versions 2.0 to 2.2	Synchronization Frame

Clock Input (CLK)

The DADS1274-C/78-C requires a clock input to operate. Each converter in the DADS1274-C/78-C operates on the same clock input. For maximum data rates, the clock input is 27MHz or 13.5MHz in low-power mode, and 27MHz or 5.4MHz in low-speed mode, depending on the CLKDIV input setting. For high-speed mode, the maximum CLK input frequency is 37MHz. For high-resolution mode, the maximum CLK input frequency is 27MHz. Operation in high-speed mode is limited by the clock input frequency.

external clock frequency (fCLK) does not affect the resolution of the DADS1274-C/78-C. Using a low fCLK reduces the power consumption of the external clock buffer. The output data rate is proportional to the clock frequency; the minimum clock frequency can be fCLK = 100kHz. The table below summarizes the ratio of clock frequency (fCLK) to data rate (fDATA), the maximum data rate, and the corresponding maximum clock input in the four operating modes. For any high-speed data converter, a high-quality, low-jitter clock ensures optimal performance. Ensuring that the clock input does not overload, keeping the clock trace as short as possible, and using a 50Ω series resistor close to the source typically improves overall system performance.

Table 5. Clock Input Options

Mode Selection	MAX f_{CLK} (MHz)	CLKDIV	f_{CLK} / f_{DATA}	Data rate (SPS)
High speed	37	1	256	144,531
High resolution	27	1	512	52,734
Low power consumption	27	1	512	52,734
	13.5	0	256	
Low speed	27	1	2,560	10,547
	5.4	0	512	

Mode Selection (MODE)

The DADS1274-C/78-C supports four operating modes: high speed, high resolution, low power, and low speed. These modes provide optimized speed, resolution, and power consumption, selected by the status of the digital input pins MODE[1:0]. The DADS1274-C/78-C continuously monitors the status of the MODE pins during operation.

Table 6. Mode Selection

MODE[1:0]	Mode Selection	MAX f_{DATA} (1)
00	High speed	144,531
01	High resolution	52,734
10	Low power consumption	52,734
11	Low speed	10,547

(1) **fCLK = 27MHz maximum (37MHz maximum in high-speed mode)**

When using the SPI protocol, the $\overline{DRDY}$ pin remains high after a mode change occurs until data setup (or validity) is complete. In the synchronous frame protocol, the DOUT pin remains low after a mode change occurs until data setup (or validity) is complete, as shown in Figure 2 and Table 7. When DOUT changes to logic 1, it indicates that data is valid, and data can be read and detected from the chip.

Figure 2. Mode Selection

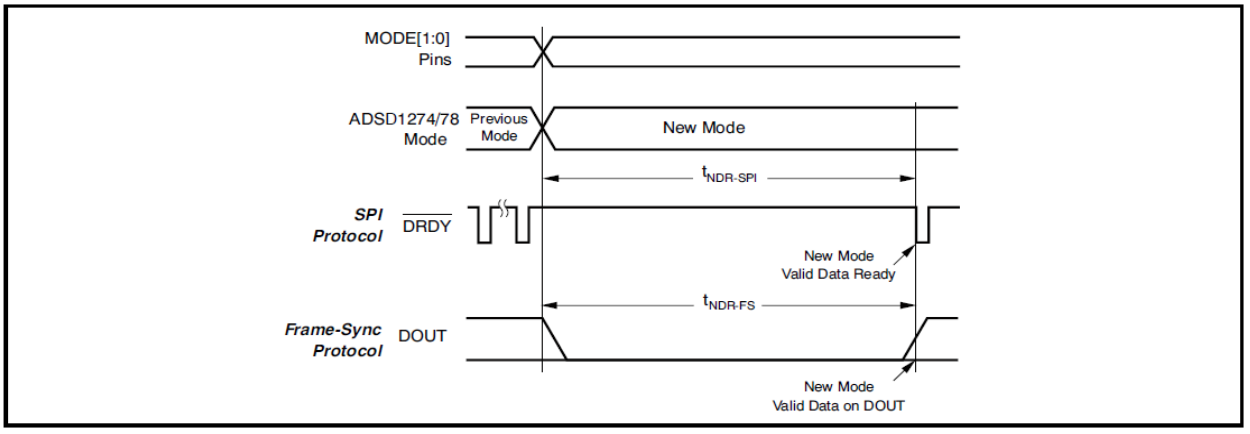


Table 7. New data after the pattern change

Symbol	Description	MIN	TYP	MAX	Unit
$t_{NDR-SPI}$	New Data Preparation Time (SPI)			129	Transform ($1/f_{DATA}$)
t_{NDR-FS}	New data preparation time (Frame-Sync) (1)	127		128	Transform ($1/f_{DATA}$)

(1) If the mode change is out of sync with the FSYNC clock, t_{NDR-FS} will vary between transitions 127 and 128. If the mode change is synchronized with FSYNC, T_{NDR-FS} will remain stable .

Synchronization (SYNC)

The DADS1274-C/78-C can be synchronized by pulsing the SYNC pin low and then returning it high. When the pin goes low, the conversion process stops, and the internal counter used by the digital filter is reset. When the SYNC pin returns to high, the conversion process restarts. Synchronization allows the conversion to be aligned with external events, such as changes in the external multiplexer on the analog input, or by referencing timing pulses. Because the DADS1274-C/78-C converters operate in parallel from the same master clock and use the same SYNC input for control, they are always synchronized with each other. Aperture matching between internal channels is typically less than 500 ps. However, synchronization of multiple devices is somewhat different. Changes in the internal reset threshold between devices when they are powered on can cause uncertainty in the conversion timing. The SYNC pin can be used to synchronize multiple devices to the same CLK cycle. Figure 3 shows the timing requirements for SYNC and CLK in SPI format. The timing requirements for frame synchronization format are shown in Figure 4. After synchronization, the indication of valid data depends on whether SPI or frame synchronization format is used. In SPI format, DRDY goes high once SYNC goes low; see Figure 3 . After SYNC returns high, DRDY remains high while the digital filter stabilizes. DRDY goes low once valid data is ready to be retrieved. In the frame synchronization format, DOUT goes low once Sync goes low; see Figure 4. After SYNC returns high, DOUT remains low while the digital filter stabilizes. DOUT begins outputting valid data once valid data is ready to be retrieved. For proper synchronization, FSYNC, SCLK, and CLK must be established before setting SYNC high, and then kept running. If the clock inputs (CLK, FSYNC, or SCLK) are subsequently interrupted or reset, the SYNC pin must be re-asserted. For consistent performance, re-asserte SYNC after the device is powered on when data first appears.

Figure 3. Synchronization Timing (SPI Protocol)

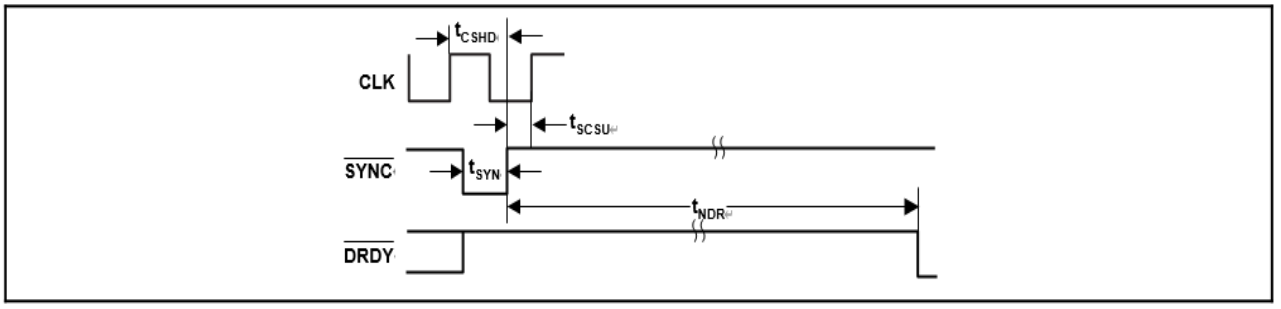
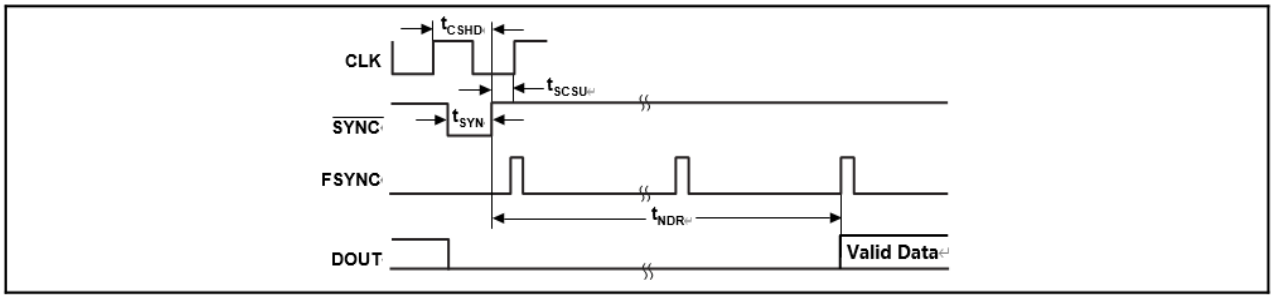


Figure 4. Synchronization Timing (Synchronization Frame Protocol)



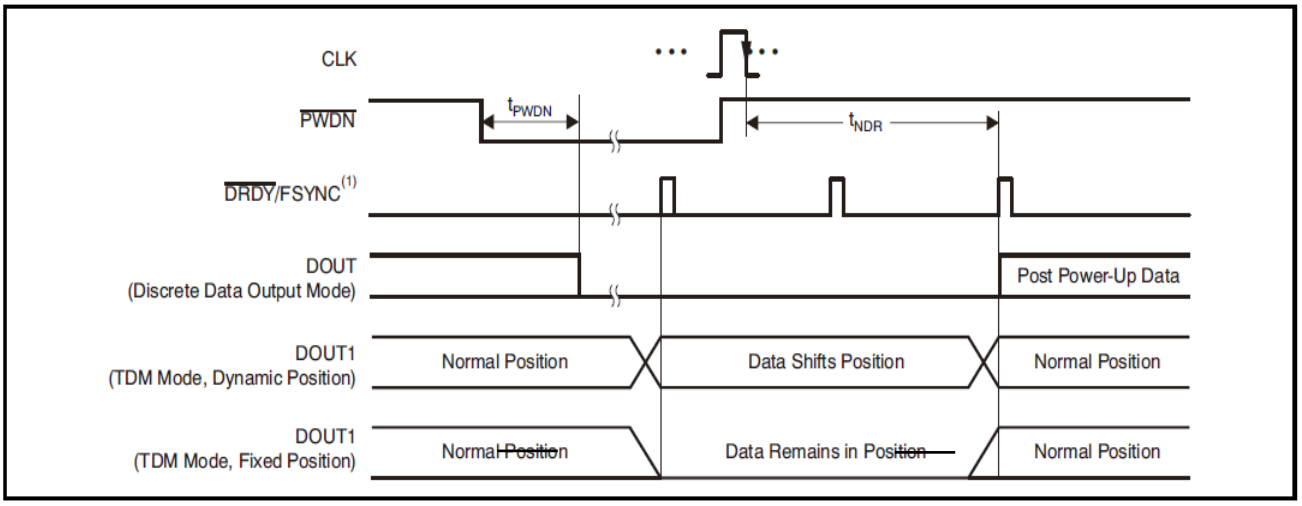
Power-Down (PWDN)

The DADS1274-C/78-C channels can be independently powered down using the PWDN input. To enter power-down mode, hold the corresponding PWDN pin low for at least two CLK cycles. To exit power-down, return the corresponding PWDN pin high. Note that when all channels are powered down, the DADS1274-C/78-C enters a microwatt (μW) power state, and all internal biases are disabled. In this state, the TEST[1:0] input pins must be driven; all other input pins can float. The DADS1274-C/78-C outputs remain driven. As shown in Figure 5 and Table 8 , the SPI interface must undergo a maximum of 130 conversion cycles before reading data after power-down, and frame synchronization must undergo 129 conversion cycles. Data from running channels is unaffected. User software can implement the required delay time in any of the following ways:

1. Count the number of data transitions after the PWDN pin goes high.
2. After the PWDN pin goes high, delay for 129/f_{DATA} or 130/f_{DATA}, then read the data.
3. Detect non-zero data in the power-on channel.

After one or more channels are powered on, these channels synchronize with each other. A SYNC pin is not required for synchronization. When a channel is powered off in TDM data format, the data on that channel is either forced to zero (fixed-position TDM data mode) or replaced by transferring the data from the next channel to an idle data location (dynamic-position TDM digital mode). In discrete data format, the data is always forced to zero. When a channel is powered on in dynamic-position TDM data format mode, the channel data remains packed until the data is ready, at which point the data frame is expanded to include the channel data that was just powered on.

Figure 5. Power-down Timing



(1) For the SPI protocol, this occurs on the falling edge of DRDY/FSYNC. Closing all channels forces DRDY/FSYNC high.

Table 8. Power-down Timing

Symbol	Description	MIN	TYP	MAX	Unit
t_{PWDN}	PWDN pulse width for entering power-off mode	2			CLK periods
t_{NDR}	New Data Ready Time (SPI)	129		130	Transform (1/f_{DATA})
t_{NDR}	New data readiness time (Frame-Sync) (1)	128		129	Transform (1/f_{DATA})

(1) The FSYNC clock runs before the rising edge of PWDN. If PWDN is asynchronous with the FSYNC clock, t_{NDR-FS} transitions between 127 and 128. If PWDN is synchronous with FSYNC, t_{NDR-FS} is stable.

FORMAT[2:0]

Data can be read from the DADS1274-C/78-C via two interface protocols (SPI or Frame Synchronization) and several data format options (TDM/Discrete and Fixed/Dynamic Data Location). The FORMAT[2:0] inputs are used to select from the options. Table 9 lists the available options. For details on DOUT modes and data locations, please refer to the DOUT Modes section.

Table 9. Data Output Format

FORMAT [2:0]	Interface Protocol	DOUT Mode	Data
000	SPI	TDM	dynamic
001	SPI	TDM	fixed
010	SPI	Discrete	
011	Frame synchronization	TDM	dynamic
100	Frame synchronization	TDM	fixed
101	Frame synchronization	Discrete	
110	Modulator mode		

Serial interface protocol

The DADS1274-C/78-C uses a serial interface to retrieve data. Two valid protocols are provided: SPI and Frame Synchronization. Both interfaces use the same pins: SCLK, DRDY/FSYNC, DOUT[4:1] (DOUT[8:1] for DADS1278-C), and DIN. The FORMAT[2:0] pins select the desired protocol.

SPI serial interface

The SPI-compatible format is a read-only interface. Data retrieval is indicated by the falling edge of the DRDY output and shifted out on the falling edge of SCLK, with the MSB first. When used in multi-machine mode, this interface can use daisy-chained DIN inputs.

Note: The upper frequency limit for the CLK input in SPI format is 27MHz. When the CLK input operation exceeds 27MHz (high-speed mode only), the frame synchronization format is used.

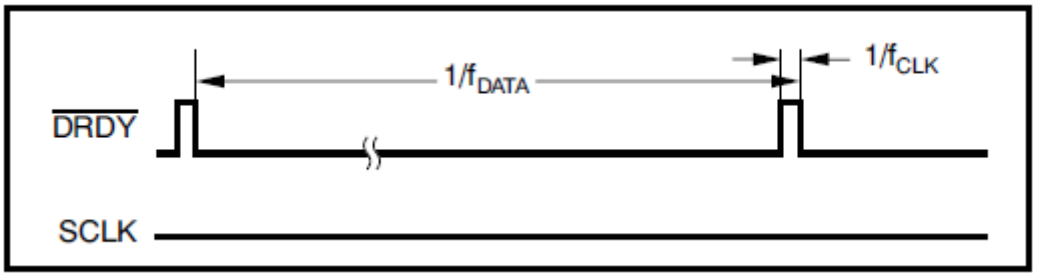
SCLK

The serial clock (SCLK) is a Schmitt input and shifts data out on the falling edge of DOUT. When the DIN pin is used for daisy-chaining, data is also shifted in on the falling edge of DIN. The chip shifts data out on the falling edge and typically shifts in on the rising edge. If there is hysteresis at the SCLK input, it is recommended to keep SCLK as clean as possible to prevent accidental data shifting. SCLK can operate as fast as CLK. During transitions, SCLK can freely run or stop. Note that the time requirement from the falling edge of DRDY to the next rising edge of SCLK is fCLK . For optimal performance, the fSCLK / fCLK ratio is limited to 1, 1/2, 1/4, 1/8, etc. When the chip is configured as a modulator output, SCLK becomes the modulator clock output.

DYDR/FSYNC (SPI format)

In SPI format, this pin is the DRDY output. It goes low when data is ready and returns high on the falling edge of the first SCLK clock cycle. If data cannot be retrieved (e.g., SCLK remains low), DRDY becomes a positive pulse before the next transition data is ready , as shown in Figure 6. New data is loaded one CLK cycle before DRDY goes low. All data must be shifted out before being overwritten.

Figure 6. DRDY Timings Without Readback



DOUT

The converted data is output on DOUT[4:1]/[8:1]. MSB data is valid on DOUT[4:1]/[8:1] when DRDY goes low. Subsequent data bits are shifted out on each falling edge of SCLK. In a daisy-chain configuration, data is shifted in via DIN and out after all channels displayed on DOUT have been shifted out. When the chip is configured as a modulator output, DOUT[4:1]/[8:1] becomes the modulator's data output.

DIN

Use this input when multiple DADS1274-C/78-Cs are to be daisy-chained together. Connect the DOUT1 pin of the first device to the DIN pin of the next device, and so on. It can be used with SPI or frame synchronization formats. Data is shifted in on the falling edge of SCLK. When using only one DADS1274-C/78-C, connect DIN to the low bit.

Frame Synchronization Serial Interface

The frame synchronization format is often used in interfaces such as audio analog-to-digital converters (ADCs). It operates in a slave mode — the user must support the frame signal FSYNC (similar to the left/right clock of a stereo audio ADC) and the serial clock SCLK (similar to the bit clock of an audio ADC). Data is first output at the MSB or left-aligned on the rising edge of FSYNC. When using the frame synchronization format, the FSYNC and SCLK inputs must operate continuously according to the relationship shown in the frame synchronization timing requirements.

SCLK

The serial clock (SCLK) has a Schmitt trigger input and shifts out data on DOUT on the falling edge. When this pin is used in a daisy chain, it also shifts data on the falling edge of DIN. Although SCLK has hysteresis, it is recommended to keep SCLK as clean as possible to prevent failures caused by accidental data shifting. When using the frame synchronization format, SCLK must run continuously. If it is turned off, data readback will be corrupted. The number of SCLK cycles within a frame period (FSYNC clock) can be any power of two of the CLK period (1, 1/2, 1/4, etc.), as long as the number of cycles is sufficient to shift the data output from all channels within a frame. When the device is configured as a modulator output, SCLK becomes the modulator clock output.

DRDY/FSYNC (Frame Synchronization Format)

In frame synchronization format, this pin is used as the FSYNC input. The frame synchronization input (FSYNC) sets the frame period, which must be the same as the data rate. The number of fCLK cycles required per FSYNC cycle depends on the mode selection and the CLKDIV input. Table 5 indicates the number of CLK cycles (fCLK /fDATA) to each frame. If the FSYNC cycle is not the correct value, data readback will be corrupted.

DOUT

The converted data is shifted on DOUT[4:1]/[8:1]. After FSYNC goes high, the MSB data becomes valid on DOUT[4:1]/[8:1]. Subsequent bits are shifted out with each falling edge of SCLK. If daisy-chained, the data shifted in using DIN is displayed on DOUT[4:1]/[8:1] after all channel data has been shifted out. When the device is configured as a modulator output, DOUT becomes the modulator data output.

DIN

Use this input when multiple DADS1274-C/78-Cs are to be daisy-chained together. It can be used with SPI or frame synchronization formats. Data is shifted in on the falling edge of SCLK. When using only one DADS1274-C/78-C, connect DIN to the low bit.

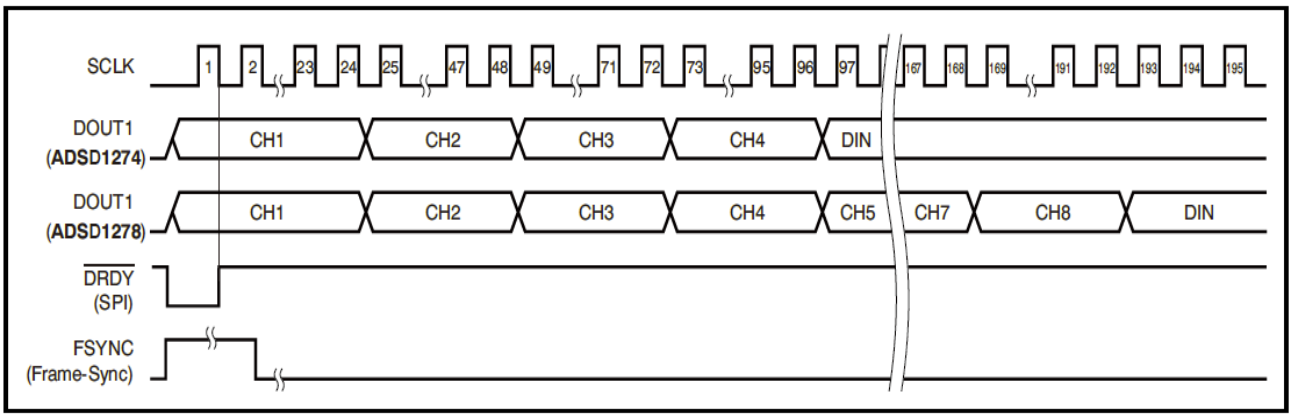
DOUT mode

For SPI and frame synchronization interface protocols, data is shifted out in parallel data format (discrete mode) through a single channel DOUT pin, or in serial format through the common pin DOUT1 (TDM mode) to shift out data from all channels.

TDM mode

In TDM (Time Division Multiplexing) data output mode, data from all channels is shifted out sequentially on a single pin (DOUT1). As shown in Figure 7, data from channel 1 is shifted out first, followed by data from channel 2, and so on. Data from the DIN input follows immediately after the last channel's data is shifted out. DIN is used for daisy-chaining data outputs of additional DADS1274-C/78-C or other compatible devices. Note that when all channels of the DADS1274-C/78-C are disabled, the interface is also disabled, thus disabling the DIN input. The data format in TDM mode can be fixed or dynamic when one or more channels of the device are powered off.

Figure 7. TDM Mode (All Channels Enabled)



TDM mode, fixed location data

In TDM data output mode, the channel data position is fixed regardless of whether the channel is closed. If a channel is closed, the data is forced to zero but still occupies the same position in the data stream. Figure 8 illustrates the data stream when channels 1 and 3 are closed.

Data TDM mode, dynamic location data

In this TDM data output mode, when a channel is closed, a data stream position is moved from the higher channel to fill the empty data slot. Figure 9 illustrates the data flow when channels 1 and 3 are closed.

Discrete data output mode

In discrete data output mode, channel data is shifted out in parallel using separate data output pins DOUT[4:1]/[8:1]. After 24 SCLKs, the channel data is forced to zero. Closed channel data is also forced to zero. Figure 10 illustrates the discrete data output format.

Figure 8. TDM mode, fixed location data (channels 1 and 3 off)

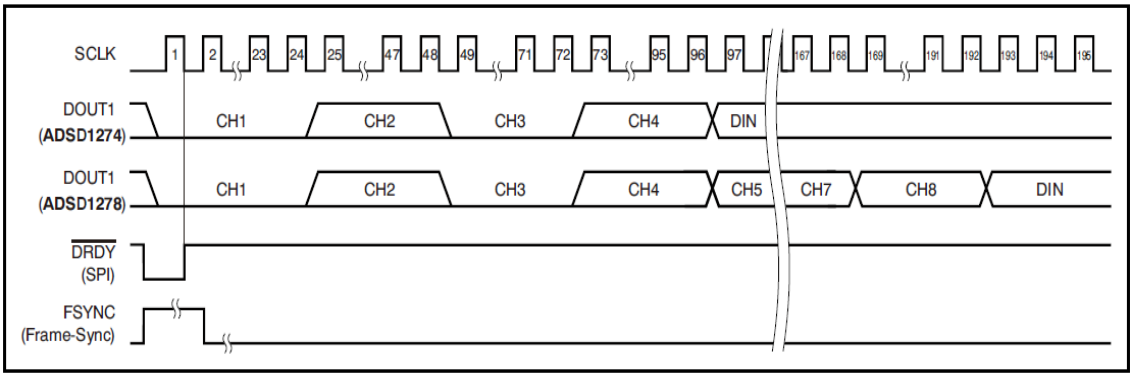


Figure 9. TDM mode, dynamic location data (channels 1 and 3 off)

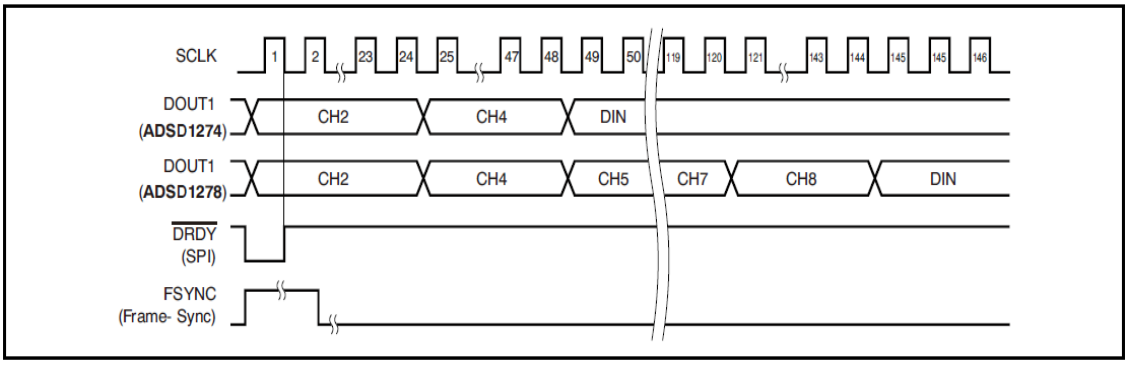
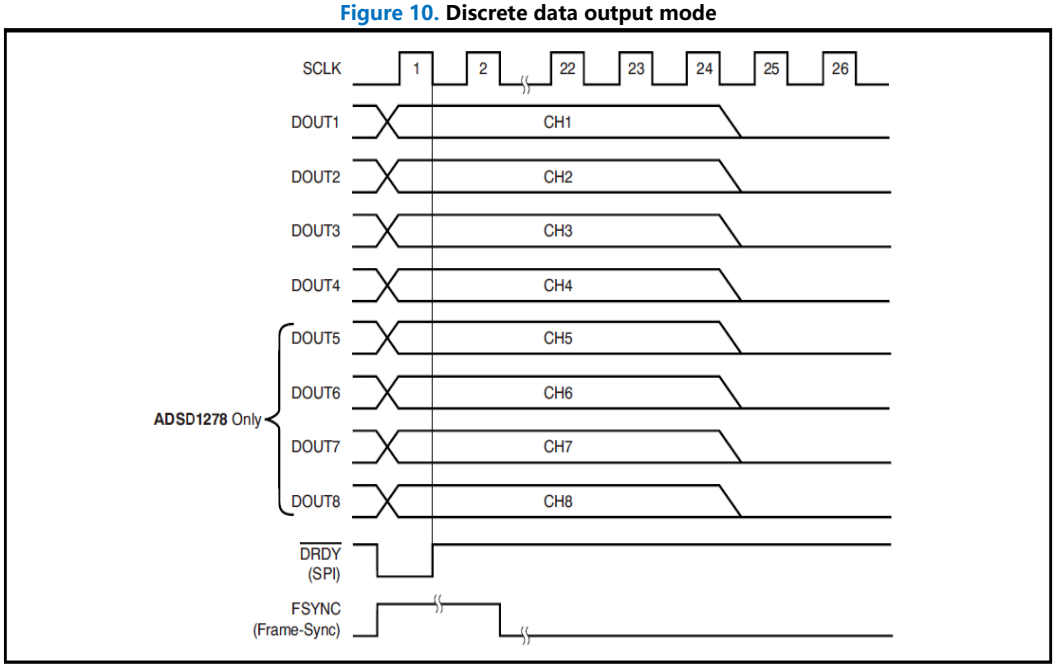


Figure 10. Discrete data output mode



Daisy-chaining

Multiple DADS1274-C/78-Cs can be daisy-chained to output data from a single pin. The DOUT1 data output pin of one chip is connected to the DIN pin of the next chip. As shown in Figure 11, chip 1's DOUT1 pin provides output data to the controller, while chip 2's DIN is grounded. Figure 12 shows the data format when reading back data. The maximum number of channels that can be used in daisy-chaining is limited by the frequency fSCLK , mode selection, and CLKDIV input. f_{SCLK} must be high enough to completely shift data out of all channels within one fDATA cycle. Table 10 lists the maximum number of channels in a daisy chain when $f_{SCLK} = f_{CLK}$. To increase the number of possible data channels in the chain, a segmented DOUT scheme can be used, generating two data streams. Figure 13 shows four DADS1274-C/78-Cs forming an DADS1274-C/78-C daisy-chain pair. The channel data of each daisy-chain pair is shifted out in parallel and received by the processor through an independent data channel. Regardless of whether the interface protocol is SPI or frame synchronization, it is recommended to synchronize all chips by binding the SYNC input together. During SPI protocol synchronization, only the DRDY output of the DADS1274-C/78-C needs to be monitored. In the frame synchronization protocol, data from all chips is ready after the rising edge of FSYNC. Because both DOUT1 and DIN are shifted on the falling edge of SCLK, the propagation delay on DOUT1 is based on the setup time of DIN. Minimize the skew of SCLK to avoid timing conflicts.

Table 10. Number of large channels in a daisy chain ($f_{SCLK} = f_{CLK}$)

Mode Selection	CLKDIV	Maximum number of channels
High speed	1	10
High resolution	1	21
Low power consumption	1	21
	0	10
Low speed	1	106
	0	21

Figure 11. Two -chip daisy chain, SPI protocol (FORMAT[2:0]=000 or 001)

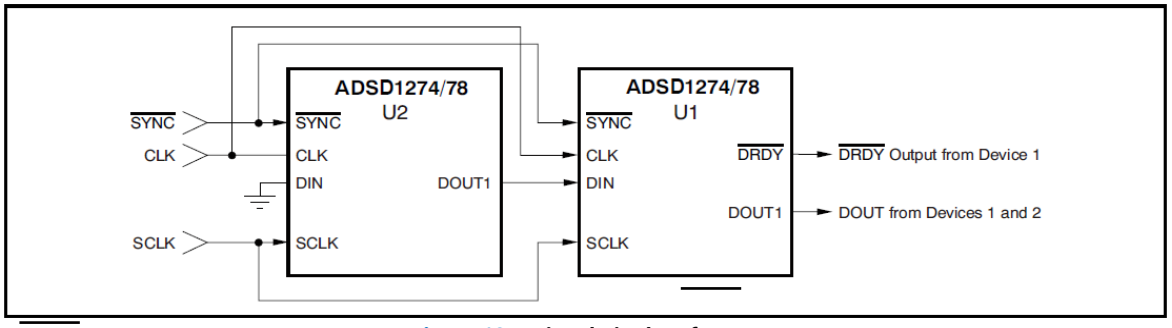


Figure 12. Daisy chain data format

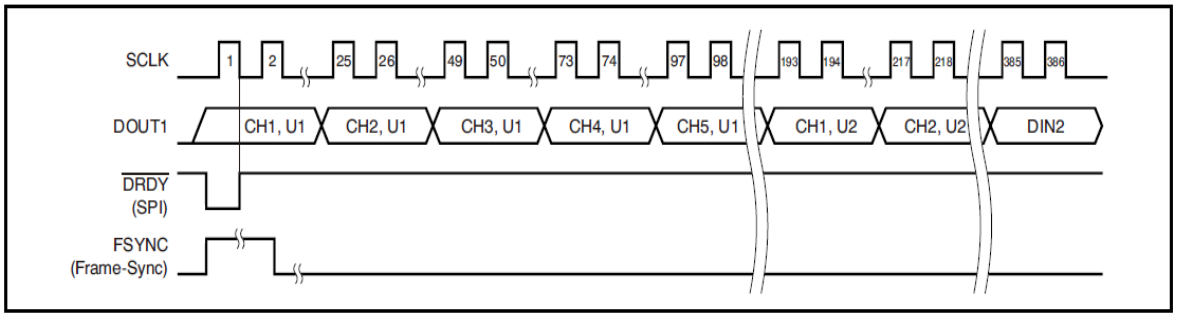
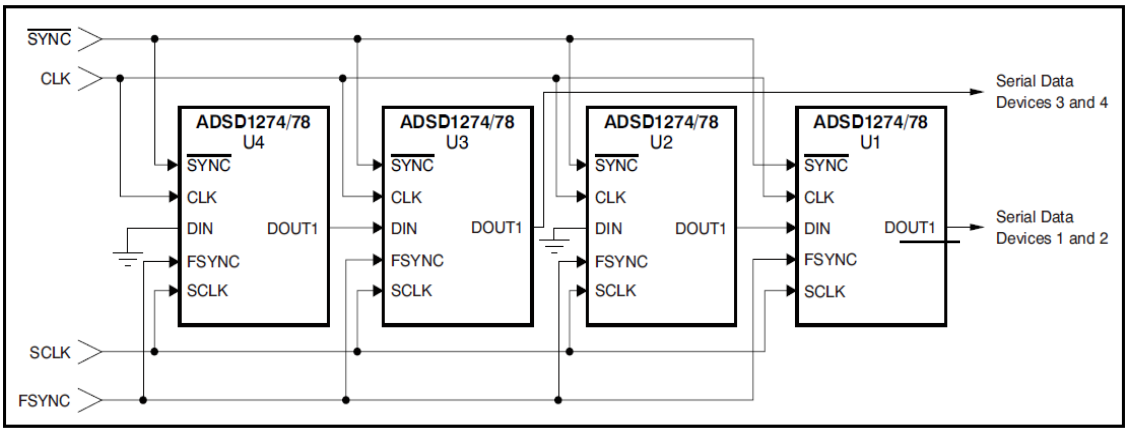


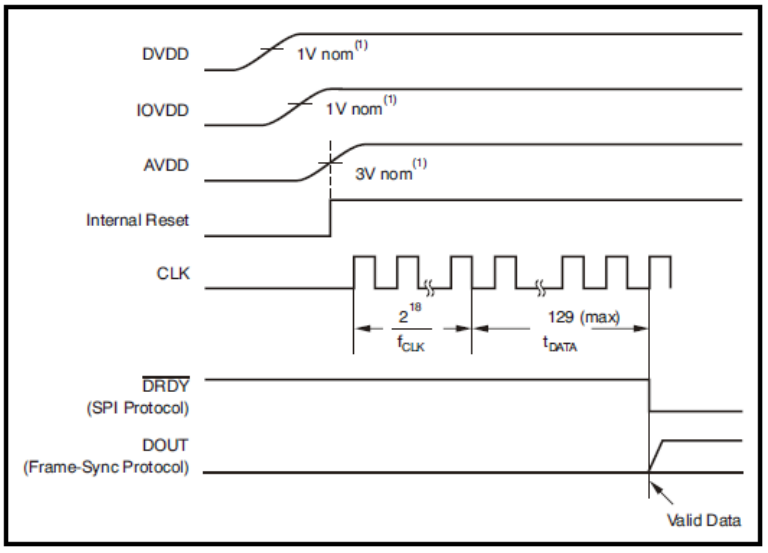
Figure 13. Daisy chain DOUT segmentation, frame synchronization protocol (FORMAT[2:0]=011 or 100)



Powered Supplies

The DADS1274-C/78-C has three power supplies: AVDD, DVDD, and IOVDD. AVDD is the analog power supply for the modulator, DVDD is the digital power supply for the digital core, and IOVDD is the digital I/O power supply. The IOVDD and DVDD power supplies can be connected together (+1.8V) if needed. For rated performance, it is crucial to place the 0.1μF and 10μF capacitors as close as possible to the power supply pins as possible. A single 10μF ceramic capacitor can be used instead of both capacitors. Figure 14 shows the startup sequence of the DADS1274-C/78-C. Upon power-up, turn on the DVDD power supply first, then IOVDD, and finally AVDD. Check that the power supply sequence is correct, including the ramp rate of each power supply. DVDD and IOVDD can be sequenced simultaneously (e.g., if the power supplies are connected together). Each power supply has an internal reset circuit whose outputs are summed to produce a global power-on reset. A count of 2^18 fCLK cycles is performed after the power supply has exceeded the reset threshold and before the converter initiates the conversion process . After the CLK cycle, the DADS1274-C/78-C suppresses the data from the 129 conversion to allow for fully stable output data. In the SPI protocol, DRDY remains high during this interval. In the frame synchronization protocol, DOUT is forced to zero. Power should be applied before driving any analog or digital pins. For consistent performance, assert SYNC after the device is powered on when the data first appears.

Figure 14. Start-up sequence



(1) Approximate power-on reset threshold

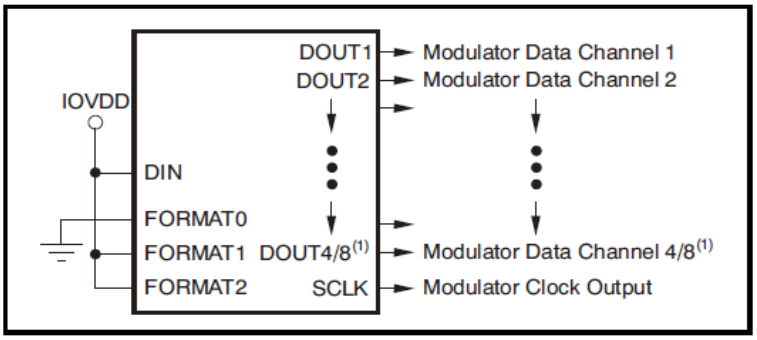
Modulator Output

The DADS1274-C/78-C contains a sixth-order, single-bit, chopper-stabilized modulator followed by a multi-stage digital filter to produce the conversion result. The modulator's data stream output is directly usable, bypassing the internal digital filter. The digital filter is disabled, thus reducing DVDD current, as shown in Table 11. In this mode, an external digital filter needs to be implemented in an ASIC, FPGA, or similar device. To invoke the modulator output, use FORMAT[2:0], as shown in Figure 15. DOUT[4:1]/[8:1] becomes the modulator data stream output for each channel, and SCLK becomes the modulator clock output. The DRDY/FSYNC pins become unused outputs and can be ignored. Frame synchronization and normal operation of the SPI interface are disabled, and SCLK changes from an input to an output, as shown in Figure 15.

Table 11. Modulator Output Clock Frequency

Mode [1:0]	CLKDIV	Modulator clock output (SCLK)	DADS1274-C DVDD (mA)	DADS1278-C DVDD (mA)
00	1	f_{CLK} /4	4.5	8
01	1	f_{CLK} /4	4.0	7
10	1	f_{CLK} /8	2.5	4
	0	f_{CLK} /4	2.5	4
11	1	f_{CLK} /40	1.0	1
	0	f_{CLK} /8	0.5	1

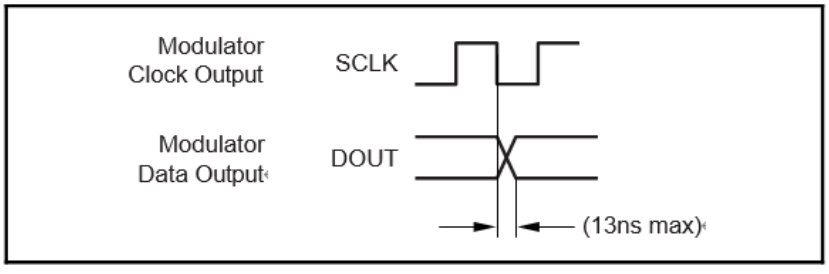
Figure 15. Modulator output



(1) DADS1274-C is a four-channel; DADS1278-C is an eight-channel.

In modulator output mode, the frequency of the modulator clock output (SCLK) depends on the mode selection of the DADS1274-C/78-C. Table 11 lists a comparison of the modulator clock output frequency and DVDD current with the chip mode. Figure 16 illustrates the timing relationship between the modulator and data output. The data output is modulated into a 1s density data stream. When V_{IN} = +V_{REF}, the 1s density is approximately 80%, while when V_{IN} = -V_{REF}, the 1s density is approximately 20%.

Figure 16. Modulator output timing



Pin Testing Using TEST[1:0] Inputs

The DADS1274-C/78-C's test mode feature allows for continuous testing of digital I/O pins. In this mode, the normal function of the digital pins is disabled and routed to other functions (pairs) via internal logic, as shown in Table 12. The pins in the left column drive the output pins in the right column. Note: Some digital input pins become outputs; these outputs must be considered in the design. Analog inputs, power, and ground pins remain connected normally. The test mode is achieved by setting the pins TEST[1:0]=11. For normal converter operation, set TEST[1:0]=00; do not use "01" or "10".

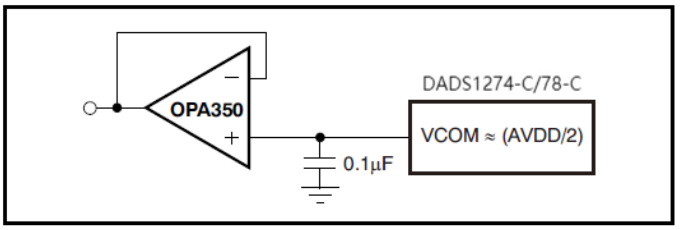
Table 12. Test mode pin mapping (Test[1:0]=11)

Input Pins	Output Pins
$\overline{\text{PWDN1}}$	DOUT1
$\overline{\text{PWDN2}}$	DOUT2
$\overline{\text{PWDN3}}$	DOUT3
$\overline{\text{PWDN4}}$	DOUT4
$\overline{\text{PWDN5}}$	DOUT5
$\overline{\text{PWDN6}}$	DOUT6
$\overline{\text{PWDN7}}$	DOUT7
$\overline{\text{PWDN8}}$	DOUT8
MODE0	DIN
MODE1	$\overline{\text{SYNC}}$
FORMAT0	CLKDIV
FORMAT1	FSYNC/$\overline{\text{DRDY}}$
FORMAT2	SCLK

VCOM Output

The VCOM pin provides an output with a voltage of AVDD/2. This output is used to set the common-mode output level of the analog input device. The drive capability of this output is limited; therefore, it should only be used to drive high-impedance (>1MΩ) nodes. In some cases, external buffering is required. A 0.1 µF bypass capacitor is recommended to reduce noise.

Figure 17. VCOM Output



Application Information

To obtain the specified characteristics from DADS1274-C/78-C, the following layout and component guidelines must be considered.

1. Power Supply: The chip requires three operating power supplies: DVDD, IOVDD, and AVDD. DVDD is permitted from 1.65V to 1.95V (32.768MHz < fCLK ≤ 37MHz: 2.0V to 2.2V); IOVDD is permitted from 1.65V to 3.6V; and AVDD is limited to 4.75V to 5.25V. All power supplies should be supplied using a 10 µF tantalum capacitor and a 0.1 µF bypass ceramic capacitor placed close to the chip pins. Alternatively, a single 10 µF ceramic capacitor can be used . The power supplies should be noise-insensitive and not shared with devices that generate voltage spikes (such as relays, LED display drivers, etc.). If a switching power supply is used, the voltage ripple should be low (less than 2mV) and the switching frequency should be outside the converter's passband.

2. Grounding: A single ground connection can be used to connect the AGND and DGND pins. If separate digital and analog grounds are used, connect them together to the converter.

3. Digital Input: It is recommended to connect a 50Ω resistor in series between the digital input and the chip. This resistor should be placed near the driver terminal of the digital source (oscillator, logic gate, DSP, etc.). This method helps reduce ripple on digital lines (ripple will cause degradation of ADC characteristics).

4. Analog/Digital Circuits: Place analog circuits (input buffers, references) and related wires together, ensuring they are kept away from digital circuits (DSPs, microcontrollers, logic). Avoid direct contact between digital and analog circuits. Crossing between lines reduces noise coupling and crossover.

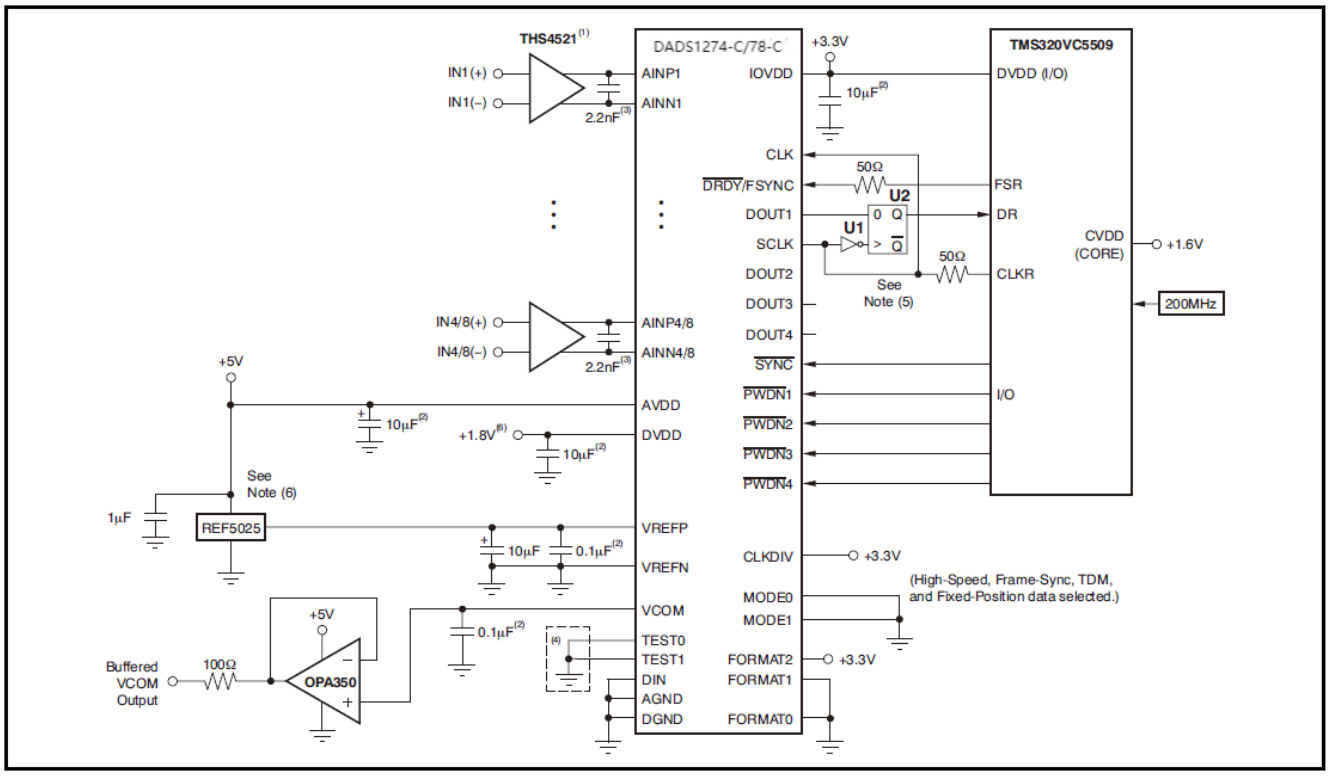
5. Reference Power Input: It is recommended to use a minimum 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor directly connected to the reference inputs VREFP and VREFN. The reference inputs are driven by a low-impedance source. For optimal characteristics, the reference source must have in-band noise of less than 3 µVRMS . If the noise of the reference source exceeds this level, it is necessary to introduce an external reference power supply filter.

6. Analog Inputs: Analog input pins require differential drive to achieve the specified characteristics. A real differential driver or transformer (for AC applications) can be used for this purpose. Connect the analog inputs (AINP, AINN) in pairs from the buffer to the converter using short traces, using straight traces and away from digital wiring. Connect a 1nF to 10nF capacitor directly to the analog input pins AINP and AINN. Use a low-k dielectric (such as COG or chrome film) to maintain a low signal-to-noise ratio. Use a capacitor for each analog input to ground. Their capacitance should not exceed 1/10 of the differential capacitor (typically 100pF) to avoid common-mode effects.

7. Component Placement: Place the bypass capacitors for power supply, analog input, and reference power input as close to the chip pins as possible. This layout is especially important for small-capacity ceramic capacitors. Large-capacity decoupling capacitors can be placed further away from the chip than small ceramic capacitors.

Figures 18 to 20 illustrate the basic connections and interfaces that can be used with the DADS1274-C.

Figure 18. Basic connection diagram of DADS1274-C/78-C



(1) An external Schottky clamping diode or series resistor may be required to prevent overvoltage on the input. Place the THS4521 driver close to the DADS1278-C input.

(2) Indicates ceramic capacitor.

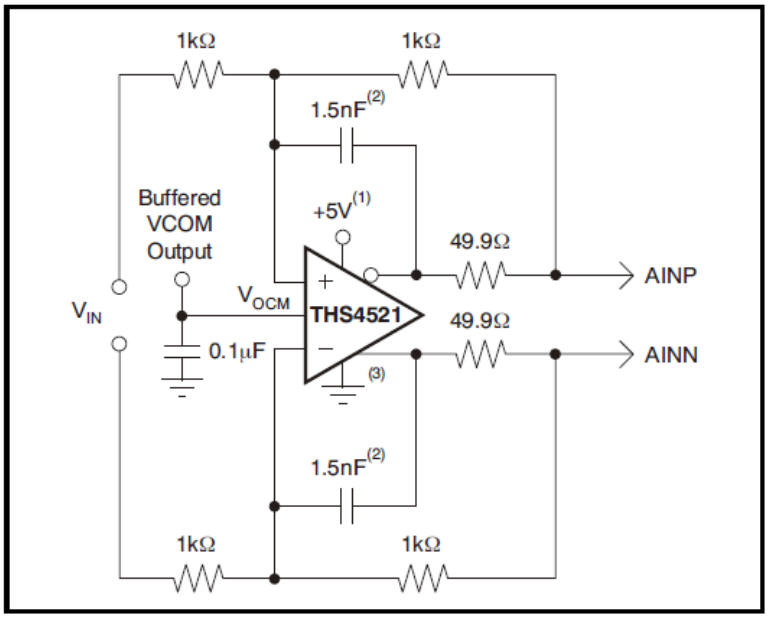
(3) indicates COG ceramic capacitor.

(4) Optional. Needle test mode.

(5) U1:SN74LVC1G04; U2:SN74LVC2G74. These components retime the DADS1274-C/78-C data output for interfacing with the TMS320VC5509.

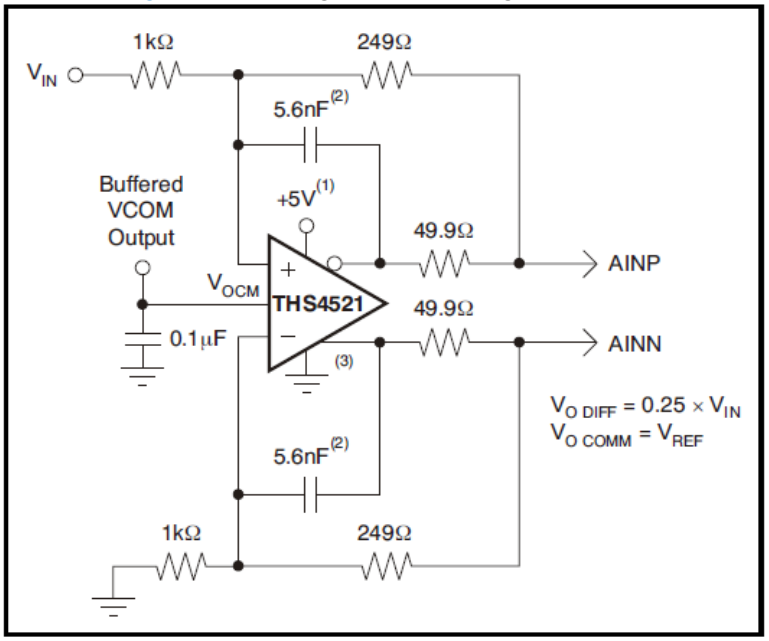
(6) If CLK > 32.768MHz, then use REF5020 and DVDD = 2.1V.

Figure 19. Basic Differential Input Signal Interface



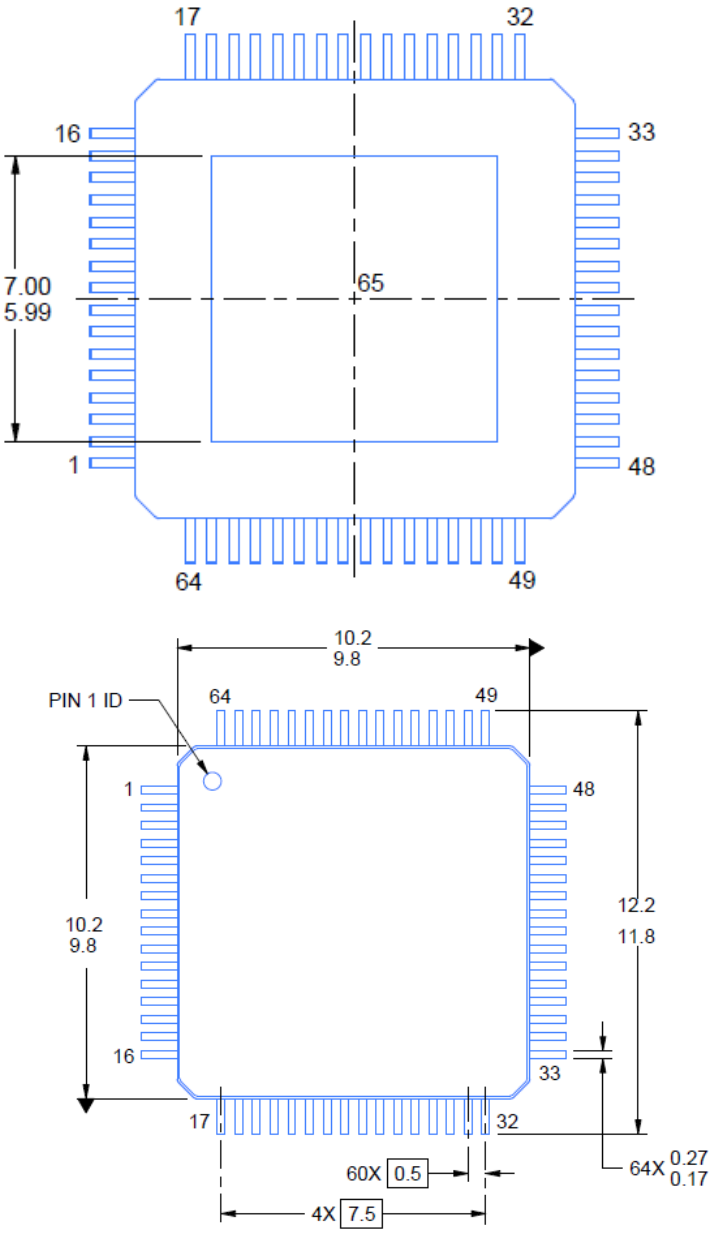
(1) Use 10µF and 0.1µF capacitors for bypassing.
(2) 2.7nF is used for low power mode; 15nF is used for low speed mode.
(3) Backup driver OPA1632 (using ±12V power supply).

Figure 20. Basic single-ended input signal interface



(1) Use 10µF and 0.1µF capacitors for bypassing.
(2) 10nF is used for low power mode; 56nF is used for low speed mode.
(3) Backup driver OPA1632 (using ±12V power supply).

Encapsulation Information



Ordering Information List

Product Model	Temperature Range	Package Type	Packaging	RoHS
DADS1274-C LFP	-40 °C to +85 °C	64-TQFP	168/tray	Y
DADS1278-C LFP	-40 °C to +85 °C	64-TQFP	168/tray	Y