DADS1256 Low Noise 24 Bit Analog-to-Digital Converter

Features

- 24-bit, no missing codes
- Up to 22-bit noise-free resolution
- 0.002% nonlinearity
- Data output rate 16KSPS
- Fast Track Loop
- Single-cycle single conversion
- Flexible input multiplexer
  - 4-channel differential input
  - 8-channel single-ended input
- Low-noise PGA: Noise referred to the input is 30nV
- Chopper-stabilized input buffer
- Supports self-calibration and system calibration of all PGAs
- SPI-compatible serial interface
- Analog supply: 5V, Digital supply: 1.8-3.3V
- Power dissipation
  - As low as 45mW in normal mode
  - 0.45mW in standby mode

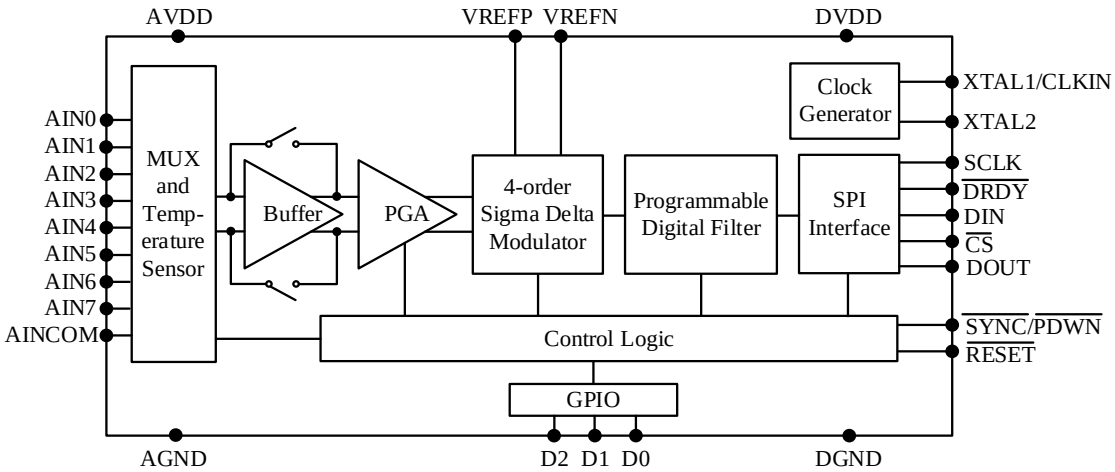
Applications

- Industrial process control
- Scientific instruments
- medical equipment
- Test equipment
- Weighing scale

Description

The DADS1256 is a high-precision data converter chip with an integrated ultra-low noise 24-bit analog-to-digital (A/D) converter. It provides a complete high-resolution measurement solution for the most demanding applications. The A/D converter consists of a 4th-order ΔΣ modulator and a programmable digital filter. Optional input buffers significantly improve input impedance, and a low-noise programmable gain amplifier (PGA) provides gain from 1 to 64 in binary steps. The programmable filter allows users to optimize between noise-free resolution up to 22 bits and data rates up to 16 kSPS. These converters provide fast channel cycling for multiplexed inputs and can also perform single conversions, built up within a single cycle.

Communication is handled via an SPI-compatible serial interface, which can be used with a two-wire connection. On-chip calibration supports self-calibration and system calibration of offset and gain errors for all PGA settings. A general-purpose programmable clock output driver is provided. The DADS1256 is packaged in an SSOP28 package.



Absolute maximum rating

Unless otherwise specified, operate within the room temperature range (1).

	DADS1256	Unit
AVDD to AGND	-0.3 to +6	V
DVDD to DGND	-0.3 to +3.6	V
DGND to AGND	-0.3 to +0.3	V
Input current	100, momentary	mA
	10, continuous	mA
AGND to analog input	- 0.3 to AVDD + 0.3	V
Digital input	- 0.3 to DVDD + 0.3	V
Operating temperature range	- 40 to + 85	℃
Storage temperature range	- 60 to +150	℃
Lead temperature (soldering, 10 seconds)	+300	℃

(1) Stress exceeding the absolute maximum ratings may cause permanent damage to the equipment. Prolonged exposure to absolute maximum conditions may reduce the reliability of the device. These are only rated stresses and do not imply functional operation of the device under these conditions or any other conditions beyond the specified conditions.

This integrated circuit may be damaged by ESD. We recommend taking appropriate preventive measures when handling all integrated circuits. Failure to follow the correct handling and installation procedures will result in damage. The extent of ESD damage ranges from minor performance degradation to complete device failure. Precision integrated circuits are more prone to damage because even the slightest parameter variation can cause the device to fail to meet its stated specifications.

Electrical characteristics

Unless otherwise specified, all specifications are in the temperature range of 40 ℃ to +85 ℃ , AVDD = +5V, DVDD = +1.8V, f_{CLKIN} = 7.68MHz, PGA = 1, V_{REF} = +2.5V.

Parameter	Test conditions	Min	Typ	Max	Unit
Analog Input					
Full-scale input voltage		± 2V_{REF}/PGA			V
Absolute input voltage (AIN0-7, AINCOM to AGND)	Buffer off	AGND - 0.1		AVDD +0.1	V
	Buffer enabled	AGND+0.1		AVDD - 2.0	V
Programmable gain amplifier		1		64	
Differential input impedance	Buffer off, PGA=1, 2, 4, 8, 16	130/PGA			KΩ
	Buffer off, PGA=32,64	5			KΩ
	Buffer enabled	70			MΩ
System performance					
Resolution		24			Bit
No missing codes	All data rates and PGA settings	24			Bit
Data rate	f_{CLKIN} = 7.68MHz	2.5		15000	SPS (1)
Integral nonlinearity	Differential input, PGA = 1	± 0.001			% FSR(2)
	Differential input, PGA = 64	± 0.002			%FSR
Offset error	After calibration	Comparable to noise level			
Offset drift	PGA = 1	± 110			nV / ℃
	PGA = 64	± 5			nV / ℃
Gain error	After calibration, PGA = 1, and the buffer is enabled.	± 0.005			%
	After calibration, PGA = 64, buffer enabled.	± 0.03			%
Gain drift	PGA = 1 to 64	±1			ppm/℃
Common-mode rejection ratio		105			dB
Noise		See the noise performance table.			
AVDD power supply rejection ratio	± 5%Δ in AVDD	70			dB
DVDD power rejection ratio	± 10%Δ in DVDD			102	dB
Reference voltage input					
Reference input voltage	V_{REF} = VREFP - VREFN	0.5	2.5	2.6	V
Negative reference voltage input (VREFN)	Buffer off	AGND - 0.1		VREFP - 0.5	V
	Buffer activated (5)	AGND+0.5		VREFP - 0.5	V
Positive reference voltage input (VREFP)	Buffer off	VREFN + 0.5		AVDD + 0.1	V
	Buffer activated (5)	VREFN+0.5		AVDD - 2.0	V
Reference voltage impedance	f_{CLKIN} = 7.68MHz	18			KΩ

Electrical characteristics (continued)

Unless otherwise specified, all specifications are in the temperature range of 40 ℃ to +85 ℃ , AVDD = +5V, DVDD = +1.8V, fCLKIN = 7.68MHz, PGA = 1, VREF = +2.5V.

Parameter	Test conditions	Min	Typ	Max	Unit
Digital Input/Output					
VIH		0.8 DVDD		DVDD	V
VIL		DGND		0.2 DVDD	V
VOH	IOH = 5mA	0.8 DVDD			V
VOL	IOL = 5mA			0.2 DVDD	V
Input hysteresis			0.5		V
Input leakage	0 < VDIGITAL INPUT < DVDD			± 10	μA
Master clock rate	External crystal oscillator between XTAL1 and XTAL2	2	7.68	8	MHz
	External oscillator drives CLKIN	0.1	7.68	8	MHz
Power supply					
AVDD		4.75		5.25	V
DVDD		1.8		3.6	V
AVDD current	Power saving mode		1		μA
	Alternative method		25		μA
	In normal mode, PGA = 1, buffer off.		7		mA
	Normal mode, PGA = 64, buffer off.		16		mA
	In normal mode, PGA = 1, buffer enabled.		14		mA
	In normal mode, PGA = 64, buffer enabled.		38		mA
DVDD current	Power saving mode		1		μA
	Standby mode, CLKOUT off. DVDD = 3.3V		100		μA
	In normal mode, CLKOUT is off. DVDD = 3.3V		3		mA
Power consumption	Normal mode, PGA = 1, buffer off. DVDD = 3.3V		45		mW
	Standby mode, DVDD = 3.3V		0.45		mW
Temperature range					
Nominal value		-40		+85	℃
Operating value		-55		+105	℃
Storage		-60		+150	℃

(1) SPS = Samples per second.

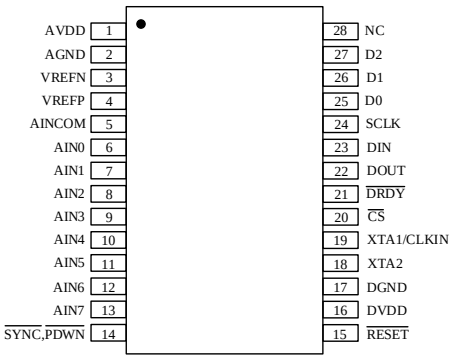
(2) FSR = Full Scale Range = $4V_{REF}$/PGA.

(3) f_{CM} is the frequency of the common-mode input signal.

(4) Setting the notch frequency of the digital filter to 60Hz (setting fDATA = 60SPS, 30SPS, 15SPS, 10SPS, 5SPS, or 2.5SPS) will further improve the common-mode rejection performance at that frequency.

(5) The reference input range when buffering is enabled is limited only when self-calibration or gain self-calibration is used.

SSOP28 package pin definitions



Pin Function Description

Name	Pin No.	Function	Description
AVDD	1	Analog	Analog power supply
AGND	2	Analog	Analog ground
VREFN	3	Analog Input	Negative reference input
VREFP	4	Analog Input	Positive reference input
AINCOM	5	Analog Input	Analog input common terminal
AIN0	6	Analog Input	Analog input 0
AIN1	7	Analog Input	Analog input 1
AIN2	8	Analog Input	Analog input 2
AIN3	9	Analog Input	Analog input 3
AIN4	10	Analog Input	Analog input 4
AIN5	11	Analog Input	Analog input 5
AIN6	12	Analog Input	Analog input 6
AIN7	13	Analog Input	Analog input 7
$\overline{\text{SYNC}}$/PDWN	14	Digital input (1)	Synchronization/shutdown input, active low
$\overline{\text{RESET}}$	15	Digital input (1)	Reset input, active low
DVDD	16	Digital	Digital power supply
DGND	17	Digital	Digital
XTAL2	18	Digital (2)	Crystal oscillator interface
XTAL1/CLKIN	19	Digital	Crystal oscillator interface /external clock input
$\overline{\text{CS}}$	20	Digital input (1)	Chip selection, active low
$\overline{\text{DRDY}}$	21	Digital output	Data ready output, active low
DOUT	22	Digital output	Serial data output
DIN	23	Digital input (1)	Serial data input
SCLK	24	Digital input (1)	Serial clock input
D0	25	Digital I/O	Digital I/O 0, for chip testing only
D1	26	Digital I/O	Digital I/O 1, for chip testing only
D2	27	Digital I/O	Digital I/O 2, for chip testing only
NC	28		Not connected

(1) Schmitt trigger digital input.

(2) If an external clock input is applied to XTAL1/CLKIN, then remain disconnected.

Parameter measurement information

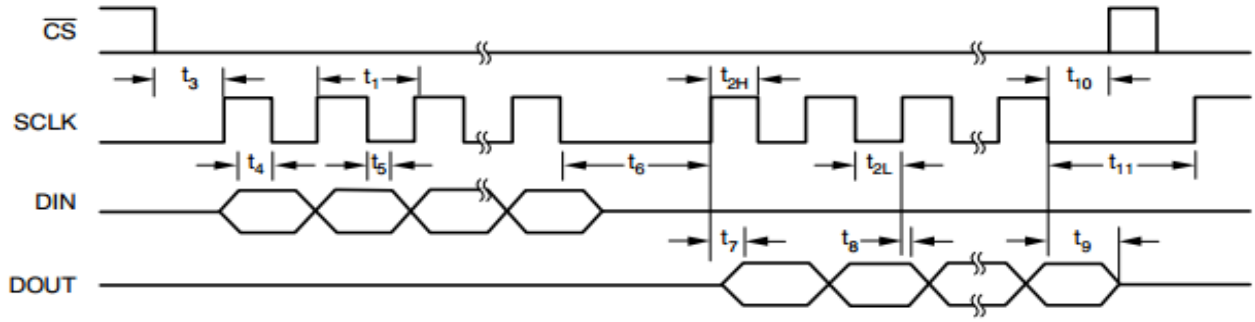


Figure 1. Serial interface timing diagram

Timing characteristics of Figure 1

Symbol	Description		Min	Max	Unit
t1	SCLK cycle		4		T_{CLKIN}(1)
				10	T_{DATA} (2)
t2H	SCLK pulse width: High		200		ns
				9	T_{DATA}
t2L	SCLK pulse width: Low		200		ns
t3	CS_N low level to the first SCLK: Setup time (3)		0		ns
t4	Effective DIN to SCLK falling edge: Setup time		50		ns
t5	Effective DIN to SCLK falling edge: Hold time		50		ns
t6	Delay of DIN from the last SCLK edge to the first SCLK rising edge of DOUT: RDATA, RDATAC, RREG commands		50		T_{CLKIN}
t7	SCLK rising edge to valid new DOUT: Propagation delay (4)			50	ns
t8	SCLK rising edge to DOUT invalid: Hold time		0		ns
t9	The last falling edge of SCLK leads to DOUT in a high-impedance state. Note : When CS_N goes high, DOUT immediately goes into a high-impedance state.		6	10	T_{CLKIN}
t10	Finally, the CS_N low level after the falling edge of SCLK		8		T_{CLKIN}
t11	The final falling edge of the command's SCLK extends to the first rising edge of the next command's SCLK.	RREG, WREG, RDATA	4		T_{CLKIN}
		RDATAC, SYNC_N	24		T_{CLKIN}
		RDATAC, RESET_N , STANDBY, SELFOCAL, SYSOCAL, SELFGCAL, SYSGCAL, SELFCAL	Wait for DRDY_N to go low.		

(1) T_{CLKIN} = master clock period = 1/ f_{CLKIN} .

(2) T_{DATA} = Output data period 1 / f_{DATA} .

(3) CS_N can be connected to low.

(4) DOUT load = 20pf || 100 kΩ to DGND.

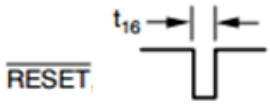


Figure 2. Reset Timing

Timing characteristics of Figure 2

Symbol	Description	Min	Max	Unit
t16	The pulse width of RESET_N	4		T_{CLKIN}(1)

(1) T_{CLKIN} = master clock period = 1/ f_{CLKIN} .

Figure 3. SYNC_PDWN_N Timing

Timing characteristics of Figure 3

Symbol	Description	Min	Max	Unit
t16	SYNC_PDWN_N , pulse width	4		T_{CLKIN}(1)
t16B	From the rising edge of SYNC_PDWN_N to the rising edge of CLKIN	-25	25	ns

(1) T_{CLKIN} = master clock period = 1/ f_{CLKIN} .

Figure 4. DRDY_N Update Timing

Timing characteristics of Figure 4

Symbol	Description	Min	Max	Unit
t17	The data conversion was invalid during the update (displaying DRDY_N, no data retrieved).	16		T_{CLKIN}(1)

(1) T_{CLKIN} = master clock period = 1/ f_{CLKIN} .

Overview

The DADS1256 is an ultra-low noise analog-to-digital converter. It supports four differential inputs or eight single-ended inputs. Figure 5 shows a block diagram of the DADS1256. An input multiplexer selects which input pins are connected to the analog-to-digital converter. An optional on-chip input buffer provides impedance up to 70 MΩ, significantly reducing input circuit load. A low-noise PGA provides gains of 1, 2, 4, 8, 16, 32, or 64 times. The DADS1256 converter consists of a 4th-order, ΔΣ modulator and a programmable digital filter. The modulator measures the amplified differential input signal VIN = (AINP – AINN) based on a differential reference voltage VREF = (VREFP - VREFN). The differential reference voltage is internally amplified by a factor of 2 , resulting in a full-scale input range of ± 2 VREF (PGA = 1).

The digital filter receives the modulator signal and provides a low-noise digital output. The filter's data rate is programmable from 2.5 SPS to 16 KSPS, allowing for a trade-off between resolution and speed. Communication is accomplished via an SPI-compatible serial interface, with a simple set of commands providing control over the DADS1256. On-chip registers store various settings such as input multiplexer, input buffer enable, PGA settings, and data rate. An external crystal oscillator or clock oscillator can be used to provide the clock source.

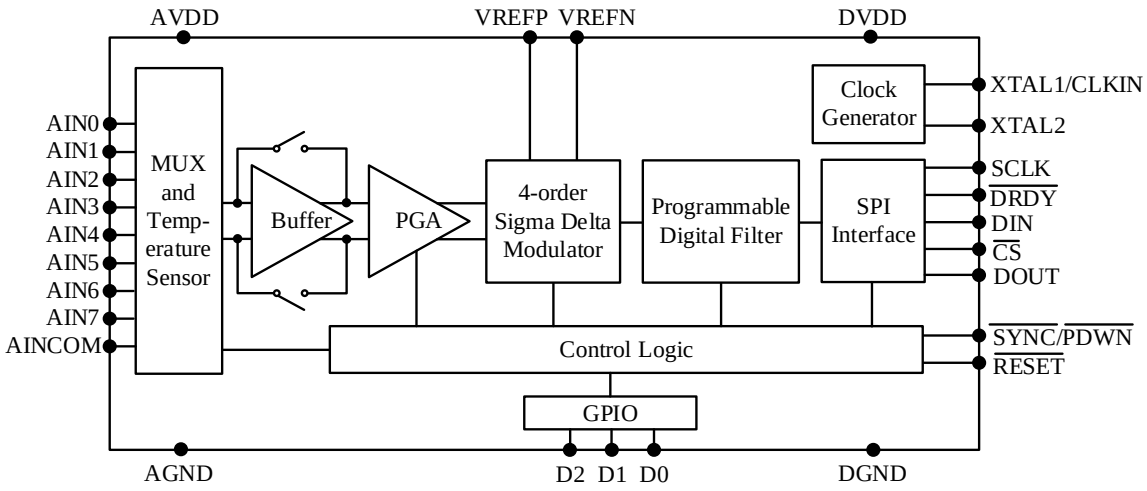


Figure 5. Top-level block diagram

Noise performance

The DADS1256 exhibits excellent noise performance, which can be optimized by adjusting the data rate or PGA settings. As the mean is increased by reducing the data rate, the noise decreases accordingly. When measuring low-level signals, the PGA reduces noise referred to the input. Tables 1 to Table 6 summarize typical noise performance with an external short circuit at the input. In all six tables, the following conditions apply: T = +25 °C , AVDD = 5V, DVDD = 1.8V, VREF = 2.5V, fCLKIN = 7.68MHz. Tables 1 to table 3 reflect the device's input buffer disabled. Table 1 shows the root mean square (RMS) noise referred to the input in volts. Table 2 shows the effective bits per second (ENOB) of the resolution using the noise data from Table 1. ENOB is defined as:

ENOB = ln(FSR/ RMS_NOISE)/ln2

Where FSR is the full-scale range. Table 3 shows the noise-free bits at resolution. Its calculation formula is the same as ENOB, except that peak-to-peak noise values are used instead of root-mean-square noise. Tables 4 to table 6 show the same noise data, but with the input buffer enabled.

Table 1. Noise referred to the input when buffer is off (μV , rms)

Data Rate (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	0.36	0.2	0.16	0.1	0.06	0.04	0.03
5	0.38	0.24	0.17	0.12	0.06	0.05	0.04
10	0.43	0.26	0.18	0.12	0.07	0.06	0.05
15	0.45	0.3	0.18	0.14	0.08	0.07	0.07
25	0.54	0.36	0.2	0.17	0.10	0.08	0.09
30	0.63	0.36	0.25	0.18	0.11	0.09	0.1
50	0.72	0.49	0.3	0.19	0.14	0.11	0.12
60	0.81	0.5	0.36	0.2	0.15	0.13	0.14
100	1.08	0.68	0.52	0.26	0.22	0.2	0.18
500	2.7	1.6	0.9	0.71	0.56	0.49	0.43
1000	3.6	1.9	1.6	1	0.77	0.68	0.78
2000	5.04	3.1	2.2	1.7	1.12	1.1	1.3
3750	10.4	5.1	3.7	2.8	2.2	2.1	1.9
7500	16.3	9.9	5.8	5.2	4.5	3.6	3.2
15,000	18.9	13.1	9.4	6.8	4.8	4.3	4.1

Table 2. Significant bits when the buffer is off (ENOB, rms)

Data Rate (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	24.7	24.3	24	23.6	23.2	22.8	22.3
5	24.6	24.2	23.9	23.2	23.2	22.7	21.6
10	24.5	24.1	23.8	23.2	23	22.3	21.5
15	24.4	23.8	23.7	23.1	22.8	22.1	21
25	24	23.7	23.4	22.8	22.6	21.8	20.7
30	23.9	23.7	23.2	22.7	22.4	21.7	20.5
50	23.6	23.3	23	22.6	22.1	21.3	20.3
60	23.5	23.2	22.7	22.5	21.9	21.1	20
100	23	22.8	22.2	22.2	21.4	20.7	19.5
500	21.8	21.5	21.4	20.7	20	19.3	18.4
1000	21.4	21.3	20.6	20.2	19.6	18.8	17.6
2000	20.9	20.6	20.1	19.4	19	18.1	16.8
3750	19.8	19.9	19.3	18.7	18.1	17.2	16.3
7500	19.2	18.9	18.7	17.8	17.1	16.4	15.6
15,000	19	18.6	18	17.5	17	16.2	15.2

Table 3. Noise -free resolution (bits) with buffer off

Data Rate (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	21.9	21.5	21.2	20.8	20.4	20	19.5
5	21.8	21.4	21.1	20.4	20.3	19.9	18.8
10	21.6	21.3	21.0	20.3	20.2	19.5	18.7
15	21.3	21.0	20.9	20.2	20.0	19.3	18.2
25	21.2	20.9	20.6	20.0	19.8	19	17.9
30	21.1	20.8	20.4	19.9	19.6	18.9	17.7
50	20.8	20.5	20.2	19.8	19.3	18.5	17.5
60	20.7	20.4	19.9	19.7	19.1	18.3	17.2
100	20.2	20.0	19.4	19.4	18.6	17.9	16.7
500	19.0	18.7	18.6	17.9	17.2	16.5	15.6
1000	18.6	18.5	17.8	17.4	16.8	16	14.8
2000	18.1	17.8	17.3	16.6	16.2	15.3	14.0
3750	17.0	17.1	16.5	15.9	15.3	14.4	13.5
7500	16.4	16.1	15.9	15.0	14.3	13.6	12.8
15,000	16.2	15.8	15.2	14.7	14.2	13.4	12.4

Table 4. Noise referred to the input when the buffer is on (μV , rms)

Data Rate (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	0.38	0.25	0.18	0.11	0.06	0.04	0.04
5	0.39	0.29	0.19	0.13	0.07	0.06	0.05
10	0.44	0.3	0.2	0.14	0.08	0.07	0.06
15	0.46	0.34	0.21	0.15	0.09	0.07	0.08
25	0.56	0.41	0.22	0.17	0.11	0.08	0.1
30	0.64	0.39	0.28	0.19	0.12	0.1	0.11
50	0.74	0.53	0.31	0.2	0.15	0.12	0.13
60	0.84	0.54	0.37	0.23	0.16	0.14	0.14
100	1.1	0.71	0.54	0.29	0.24	0.21	0.19
500	2.73	1.66	0.91	0.78	0.58	0.51	0.46
1000	3.64	1.97	1.63	1.1	0.78	0.7	0.8
2000	5.08	3.16	2.21	1.73	1.15	1.2	1.4
3750	10.5	5.2	3.73	2.9	2.24	2.3	2.0
7500	16.5	10.05	5.82	5.24	4.6	3.7	3.5
15,000	19.4	13.2	9.47	6.85	5.0	4.4	4.2

Table 5. Effective number of bits when the buffer is enabled (ENOB, rms)

Data Rate (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	24.6	24.2	23.8	23.5	23.1	22.7	22.2
5	24.5	24.1	23.8	23.2	23	22.6	21.5
10	24.4	24.0	23.7	23.1	22.9	22.2	21.3
15	24.3	23.8	23.6	23	22.7	22	20.8
25	24	23.7	23.4	22.7	22.5	21.7	20.6
30	23.8	23.6	23.1	22.6	22.4	21.6	20.4
50	23.6	23.2	22.9	22.5	22	21.2	20.2
60	23.4	23.1	22.6	22.4	21.9	21	19.8
100	22.8	22.6	22.1	22.1	21.2	20.5	19.4
500	21.7	21.4	21.2	20.5	19.9	19.2	18.1
1000	21.4	21.2	20.5	20.1	19.5	18.6	17.4
2000	20.8	20.4	20	19.3	19	18	16.6
3750	19.6	19.8	19.2	18.6	18	17.1	16.2
7500	19.1	18.7	18.6	17.8	16.9	16.2	15.5
15,000	18.9	18.5	17.9	17.4	16.7	16	15

Table 6. Noise -free resolution (bits) with buffer enabled

Data Rate (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	21.8	21.4	21.0	20.7	20.3	19.9	19.4
5	21.7	21.3	21.0	20.4	20.2	19.8	18.7
10	21.6	21.2	20.9	20.3	20.1	19.4	18.5
15	21.5	21.0	20.8	20.2	19.9	19.2	18.0
25	21.2	20.9	20.6	19.9	19.7	18.9	17.8
30	21.0	20.8	20.3	19.8	19.6	18.8	17.6
50	20.8	20.4	20.1	19.7	19.2	18.4	17.4
60	20.6	20.3	19.8	19.6	19.1	18.2	17.0
100	20.0	19.8	19.3	19.3	18.4	17.7	16.6
500	18.9	18.6	18.4	17.7	17.1	16.4	15.3
1000	18.6	18.4	17.7	17.3	16.7	15.8	14.6
2000	18.0	17.6	17.2	16.5	16.2	15.2	13.8
3750	16.8	17.0	16.4	15.8	15.2	14.3	13.4
7500	16.3	15.9	15.8	15.0	14.1	13.4	12.7
15,000	16.1	15.7	15.1	14.6	13.9	13.2	12.2

Input multiplexer

Figure 6 shows a simplified diagram of the input multiplexer. This flexible module allows any analog input pin to be connected to any converter differential input. That is, any pin can be selected as the actual input (AINP); similarly, any pin can be selected as the negative input (AINN). Pin selection is controlled by the multiplexer register.

The DADS1256 provides eight analog inputs, configurable as four independent differential inputs, eight single-ended inputs, or a combination of differential and single-ended inputs. Generally, there are no restrictions on the input pin selection. However, for optimal analog performance, we offer the following recommendations:

1. For differential measurements, use AIN0 through AIN7, preferably adjacent inputs. For example, use AIN0 and AIN1. Do not use AINCOM.

2. For single-ended measurements, AINCOM is used as a common input, and AIN0 through AIN7 are used as single-ended inputs.

3. Leave any unused analog inputs floating. This minimizes input leakage current. ESD diodes protect the analog inputs. To prevent these diodes from conducting, ensure that the voltage on the input pins is not lower than 100mV above AGND and not higher than 100mV above AVDD.

When using the DADS1256 for single-ended measurements, it is important to note that the common input AINCOM does not need to be grounded. For example, AINCOM can be connected to a midpoint reference voltage, such as +2.5V or even AVDD.

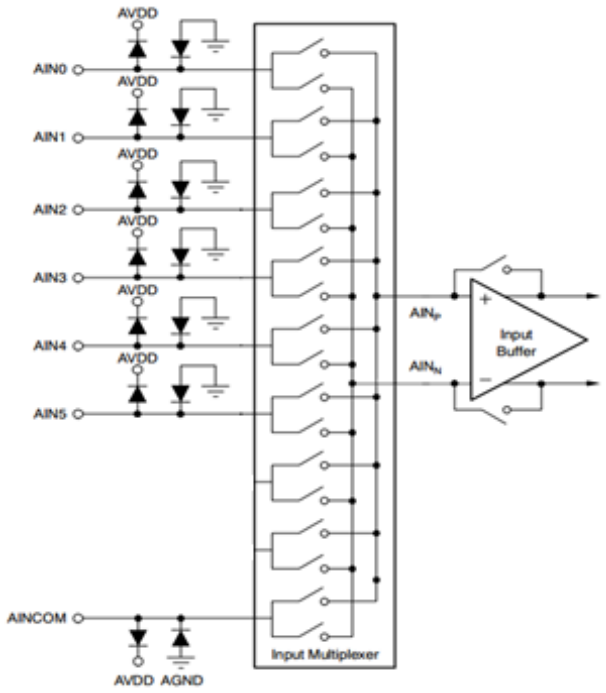


Figure 6. Simplified diagram of input multiplexer

Analog input buffer

To significantly increase the input impedance of the DADS1256, a low-drift chopper stabilization buffer can be enabled. The input impedance when the buffer is enabled can be Analog using a resistor, as shown in Figure 8. Table 7 lists the Zeff values for different data rate settings. The input impedance is inversely proportional to the CLKIN frequency. For example, if fclkin is halved to 3.84MHz, the Zeff at a 50SPS data rate will double from 70MΩ to 140MΩ.

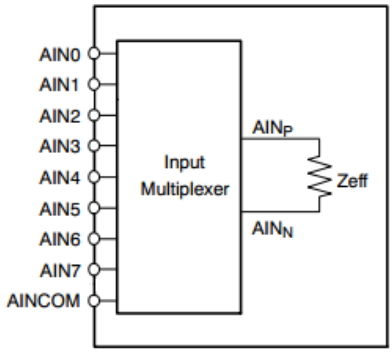


Figure 8. Effective impedance when the buffer is turned on

Table 7. Input impedance when the buffer is on

DATA RATE(SPS)	Zeff (m Ω)
≤ 50	70
60	40
100	40
500	40
1000	20
2000	10
3750	10
7500	10
15,000	10

Note: fCLKIN = 7.68MHz.

When the buffer is enabled, the voltage across the analog input switch relative to ground (listed as absolute input voltage in the electrical characteristics) must be maintained between AGND +0.5V and AVDD 2.0V. Exceeding this range will degrade performance, especially the linearity of the DADS1256. The same voltage range (AGND +0.5V to VDD - 2V) applies to the reference voltage input when performing self-gain calibration with the buffer enabled.

Programmable gain amplifier (PGA)

The DADS1256 is a high-resolution converter. To further enhance its performance, a low-noise PGA provides even higher resolution when measuring smaller input signals. For optimal resolution, set the PGA to the highest possible value. This will depend on the largest input signal you are measuring. The DADS1256's full-scale input voltage is equal to 2VREF/PGA. Table 8 shows the full-scale input voltage for different PGA settings at VREF = 2.5V. For example, if the maximum signal to be measured is 1.0V, the optimal PGA setting is 4, resulting in a full-scale input voltage of 1.25V. Higher PGAs cannot be used because they cannot handle a 1.0V input signal.

Table 8. Relationship between full-scale input voltage and PGA settings

PGA settings	Full-scale input voltage VIN(1) (VREF = 2.5V)
1	± 5V
2	± 2.5V
4	± 1.25 V
8	± 0.625 V
16	± 312.5 mV
32	± 156.25 mV
64	± 78.125 mV

(1) The input voltage is the difference between the positive and negative inputs. Ensure that no input violates the absolute input voltage relative to ground listed in the electrical characteristics. The PGA is controlled by the ADCON register. It is recommended to recalibrate the analog-to-digital converter after changing the PGA settings. The time required for self-calibration depends on the PGA settings. See the calibration section for details. Analog current and input impedance (when the buffer is disabled) vary as a function of the PGA settings.

Modulator input circuit

The DADS1256 modulator uses an internal capacitor that is continuously charged and discharged to measure the input signal. Figure 9 shows a simplified schematic of the DADS1256 input circuit with the input buffer disabled. Figure 10 shows the on/off timing of the switches in Figure 9. Switch S1 is closed during the input sampling phase. After S1 is closed, CA1 charges ANINP , CA2 charges ANINN, and CB charges (AINP-AINN). For the discharge phase, S1 is opened first, and then S2 is closed. CA1 and CA2 discharge to approximately AVDD/2, and CB discharges to 0V. This two-stage sampling/discharging cycle repeats with a sampling period. This time is a function of the PGA setting and the capacitance values CA1 = CA2 = CA and CB, as shown in Table 9.

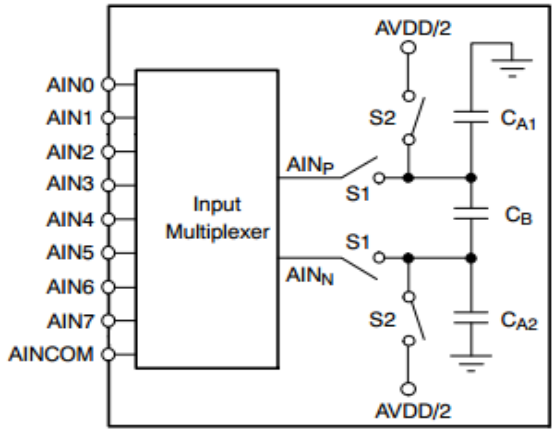


Figure 9. Simplified input structure

When the buffer is off

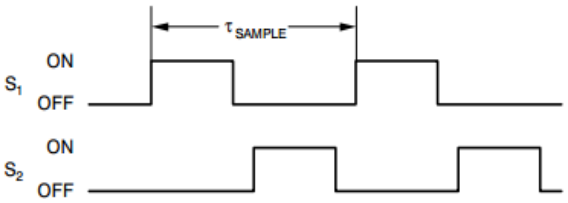


Figure 10. Timing of S1 and S2 switching in Figure 9

Table 9. Input sampling time , T SAMPLE(1) and the relationship between CA and CB and PGA

PGA settings	TSAMPLE	CA	CB
1	f_{CLKIN}/4 (260ns)	2.1pF	2.4pF
2	f_{CLKIN} /4 (260ns)	4.2pF	4.9pF
4	f_{CLKIN} /4 (260ns)	8.3pF	9.7pF
8	f_{CLKIN} /4 (260ns)	17pF	19pF
16	f_{CLKIN} /4 (260ns)	33pF	39pF
32	f_{CLKIN} /2 (260ns)	33pF	39pF
64	f_{CLKIN} /2 (260ns)	33pF	39pF

(1) f_{clkin} ' s T_{SAMPL} = 7.68 MHz.

The charging of the input capacitor draws a transient current from the sensor driving the DADS1256 input. The average value of this current can be used to calculate the effective impedance Zeff, where Zeff = VIN/IAVERAGE. Figure 11 shows the input circuit, with the capacitor and switch in Figure 9 replaced by their effective impedances. These impedances are inversely proportional to the CLKIN frequency. For

example, if fCLKIN is halved, the impedance will double. They also vary with the PGA setting. Table 10 lists the effective impedances when the buffer is off at fCLKIN = 7.68MHz.

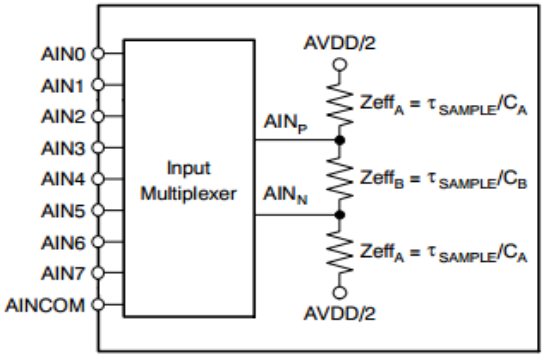


Figure 11. Effective impedance of analog input-Buffer is off

Table 10. Analog Input Impedance-Buffer is off

PGA settings	ZeffA (kΩ)	ZeffB (kΩ)
1	260	220
2	130	110
4	65	55
8	33	28
16	16	14
32	8	7
64	8	7

Note: f_{CLKIN} = 7.68MHz.

Reference voltage input (VREFP, VREFN)

The DADS1256's reference voltage source is the differential voltage between VREFP and VREFN: VREF = VREFP - VREFN. The reference input adopts a similar structure to the analog input, and the circuitry on the reference input is shown in Figure 12. When fCLKIN = 7.68MHz, the load represented by the switched capacitor can be modeled using an effective impedance (Zeff) of 18kΩ. The temperature coefficient of the effective impedance of the reference voltage input is approximately 35 ppm/ ℃ .

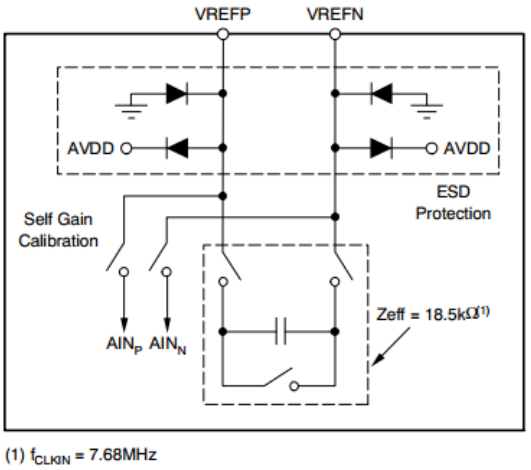


Figure 12. Simplified reference input circuit

The ESD diode protects the reference input. To prevent these diodes from conducting, ensure that the voltage at the reference pin is not lower than AGND by more than 100mV, nor higher than AVDD by more than 100mV. During self-gain calibration, all switches in the input multiplexer are disconnected, with VREFN internally connected to AINN and VREFP connected to AINP. During calibration, the input buffer can be disabled or enabled. When the buffer is disabled, the reference pin will drive the circuit shown in Figure 9 during self-gain calibration, resulting in an increase in the load. To prevent this additional load from introducing gain errors, ensure that the circuit driving the reference pin has sufficient drive capability. When the buffer is enabled, the load on the reference pin will be much smaller, but during self-calibration or self-gain calibration, the buffer will limit the allowable voltage range on VREFP and VREFN because the reference pin must remain within the rated input range of the buffer to establish the correct gain calibration. High-quality reference voltages capable of driving the DADS1256 switch-capacitor load are crucial for achieving optimal performance. Noise and drift on the reference voltage source will reduce the overall system performance. When operating in a low-noise setting (i.e., low data rate), special attention must be paid to the circuit and layout that generates the reference voltage to prevent the reference voltage from limiting performance. For details, see the "Applications" section.

Digital Filters

A programmable low-pass digital filter receives the modulator output and produces a high-resolution digital output. A trade-off between resolution and data rate can be struck by adjusting the amount of filtering: more filtering for higher resolution, less filtering for higher data rates. The filter consists of two parts: a fixed filter followed by a programmable filter. Figure 13 shows a block diagram of the analog modulator and digital filter. The analog modulator supplies data to the filter at a rate of f_{CLKIN} /4. The fixed filter is a fifth-order sinc filter with a decimation of 64, outputting data at a rate of f_{CLKIN}/256. The second stage of the filter is a programmable averaging filter (a first-order sinc filter). The mean number is set by the DRATE register. The data rate is a function of the mean number (Num_Ave), given by Equation1.

$$DataRate = \frac{f_{CLKIN}}{256} \cdot \frac{1}{Num\_Ave} \quad (1)$$

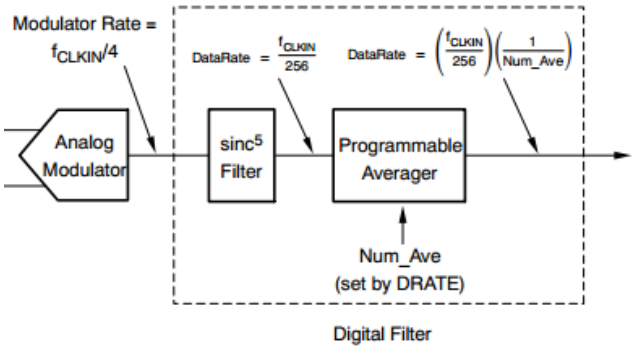


Figure 13. Block diagram of modulator and digital filter

Table 11 shows the average settings of the 16 valid DRATE registers and the corresponding data rates when f_{CLKIN}= 7.68MHz. Note that the data rate is proportional to the CLKIN frequency. For example, reducing f_{CLKIN} from 7.68MHz to 3.84MHz will reduce the data rate of DR[7:0] = 0000 0000 from 15000SPS to 7500SPS.

Table 11. Average number of records and data rate for each valid DRATE register settings

DRATEDR [7:0]	The average value (Num_Ave) of the programmable filter	Data rate (1)(SPS)
00000010	2	15,000
00000011	4	7500
00000100	8	3750
00000101	15	2000
00000110	30	1000
00000111	60	500
00001000	300	100
00001001	500	60
00001010	600	50
00001011	1000	30
00001100	1200	25
00001101	2000	15
00001110	3000	10
00001111	6000	5
00010000	12,000	2.5

(1) For f_{CLKIN} = 7.68MHz

Amplitude-frequency response

The low-pass digital filter sets the overall frequency response of the DADS1256. The filter response is the product of the fixed and programmable filter partial responses, given by Equation2.

$$|H(f)| = |H_{\sin c^5}(f)| \cdot |H_{Averager}(f)| = \left| \frac{\sin(\frac{256\pi \cdot f}{f_{CLKIN}})}{64 \cdot \sin(\frac{4\pi \cdot f}{f_{CLKIN}})} \right| \cdot \left| \frac{\sin(\frac{256\pi \cdot Num\_Ave \cdot f}{f_{CLKIN}})}{Num\_Ave \cdot \sin(\frac{256\pi \cdot f}{f_{CLKIN}})} \right| \quad (2)$$

The digital filter attenuates noise at the modulator output, including noise from within the DADS1256 and external noise from the DADS1256 input signal. The filtering is adjusted by changing the amount of average value used in the programmable filter, thus changing the filter bandwidth. A larger average value results in a smaller bandwidth and attenuates more noise.

The low-pass filter has a notch (or zero) at the data output rate and its multiples. At these frequencies, the filter gain is zero. This feature is useful when attempting to eliminate specific interfering signals. For example, to eliminate 60Hz (harmonic) interference , set the data rate to 2.5SPS, 5SPS, 10SPS, 15SPS, 30SPS, or 60SPS. To help illustrate the filter characteristics, Figures 14 and 15 show the response at the extreme data rates of 16KSPS and 2.5SPS, respectively. Table 12 summarizes the first notch frequency and 3dB bandwidth for different data rate settings .

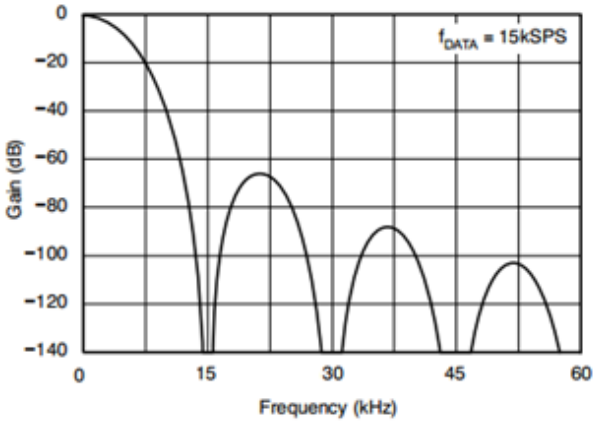


Figure 14. Frequency response at a data rate of 16 KSPS

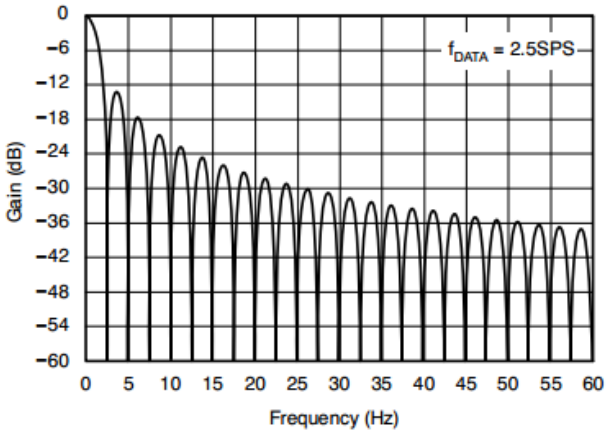


Figure 15. Frequency response at a data rate of 2.5 SPS

Table 12. First notch frequency and -3dB filter bandwidth

Data rate (SPS)	The first notch point (Hz)	- 3dB bandwidth (Hz)
15,000	15,000	4807
7500	7500	3003
3750	3750	1615
2000	2000	878
1000	1000	441
500	500	221
100	100	44.2
60(1)	60	26.5
50(2)	50	22.1
30(1)	30	13.3
25(2)	25	11.1
15(1)	15	6.63
10(3)	10	4.42
5(3)	5	2.21
2.5(3)	2.5	1.1

Note: f_{CLKIN} = 7.68MHz.

(1) Notch wave at 60Hz.

(2) Notch filtering at 50Hz.

(3) Notch filtering at 50Hz and 60Hz .

The low-pass characteristics of the digital filter repeat at modulator rate multiples of $f_{CLKIN}/4$. Figures 16 and 17 show the response at 7.68 MHz at data rate extremes of 16 KSPS and 2.5 SPS. Note that the responses near DC (1.92 MHz, 3.84 MHz, 5.76 MHz, and 7.68 MHz) are identical. The digital filter attenuates high-frequency noise at the DADS1256 input, up to the frequency of the response repetition. If significant noise at the input exceeds this frequency , ensure it is eliminated by external filtering. Fortunately, this can be achieved on the DADS1256 using a simple RC filter, as shown in the Applications section.

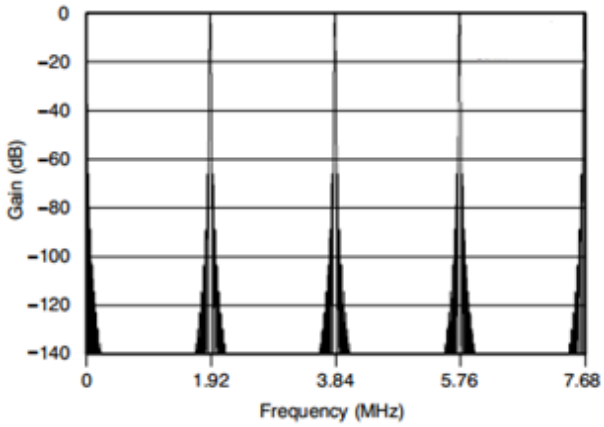


Figure 16. Frequency response of 7.68MHz at a data rate of 16KSPS.

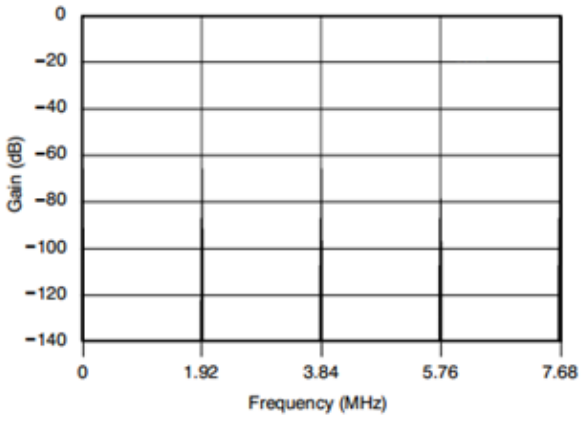


Figure 17. Frequency response of 7.68MHz at a data rate of 2.5 SPS.

Time settings

The DADS1256 features a digital filter optimized for fast setup. The setup time (the time required for a step change in the analog input to propagate through the filter) at different data rates is shown in Table 13. The following sections focus on the filter's single-cycle setup capability and demonstrate various methods for controlling the conversion process.

Table 13. Relationship between setup time and data rate

Data rate (SPS)	Setup time (t18) (ms)
15,000	0.25
7500	0.31
3750	0.44
2000	0.68
1000	1.18
500	2.18
100	10.18
60	16.84
50	20.18
30	33.51
25	40.18
15	66.84
10	100.18
5	200.18
2.5	400.18

Note: f_{CLKIN} = 7.68MHz.

Note: Single trigger mode requires a small additional delay when the device powers on from standby.

Synchronization establishment time

The SYNC_PDWN_N pin allows direct control of the conversion timing. After changing the analog input, simply issue a Sync command or strobe the SYNC_PDWN_N pin (see the Synchronization section for more information). When SYNC_PDWN_N goes high, the conversion begins, stops the current conversion, and restarts the digital filter. Once SYNC_PDWN_N goes low, the DRDY_N output goes high and remains high during the conversion. After the setup time (τ18), DRDY_N goes low, indicating that data is available. The DADS1256 sets up in a single cycle, and there is no need to ignore or discard data after synchronization. Figure 18 shows the data retrieval sequence after synchronization.

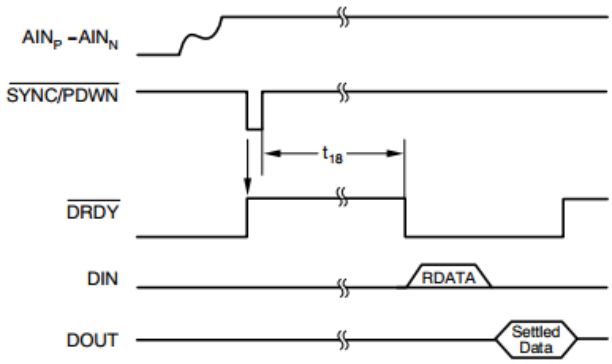


Figure 18. Data retrieval after synchronization

Setup time of input multiplexer

The most efficient method for cyclic input is to change the multiplexer settings immediately after DRDY_N goes low (using the WREG command to control the multiplexer register MUX). Then, after changing the multiplexer, restart the conversion process by issuing the SYNC and WAKEUP commands, and retrieve the data using the RDATA command. Changing the multiplexer before reading data allows the DADS1256 to start measuring new input channels more quickly. Figure 19 illustrates efficient input cycling. When cycling between channels of the input multiplexer, there is no need to ignore or discard data because the DADS1256 is fully established, indicating data readiness, before DRDY_N goes low.

Step 1: When DRDY_N goes low, it indicates that data can be retrieved. Use the WREG command to update the multiplexer register MUX. For example, if the multiplexer is set to 23h, then ANIP = AIN2 and ANIN = AIN3.

Step 2: Restart the conversion process by issuing the SYNC command, followed immediately by the WAKEUP command. Ensure that the commands follow the timing specification t11.

Step 3: Use the RDATA command to read the data from the previous conversion.

Step 4: When DRDY_N goes low again, repeat the cycle, first update the multiplexer register, and then read the previous data.

Table 14 shows the effective total throughput (1/t19) for the cyclic input multiplexer. The throughput (1/t19) value assumes that the multiplexer is changed using a 3-byte WREG command and that $f_{SCLK} = f_{CLKIN}/4$.

Table 14. Cyclic Throughput of Multiplexers

Data rate (SPS)	Cyclic throughput (1/t19) (Hz)
15,000	3817
7500	3043
3750	2165
2000	1438
1000	837
500	456
100	98
60	59
50	50
30	30
25	25
15	15
10	10
5	5
2.5	2.5

Note: f_{CLKIN} = 7.68MHz.

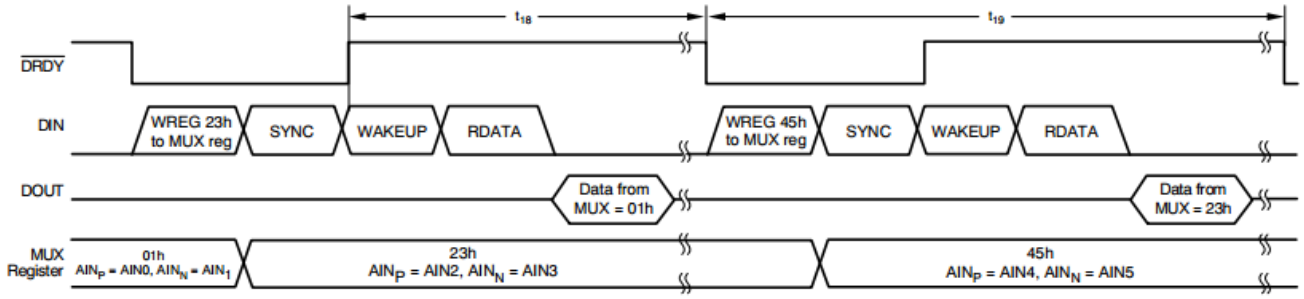


Figure 19. Cyclic input multiplexer of DADS1256

Establishment time of single-trigger mode

Utilizing a standby command to perform a single conversion can significantly reduce the power consumption of the DADS1256; the sequence is shown in Figure 20. A wake-up command is issued from standby mode to begin the single conversion. When using single-trigger mode, modulator power-up and setup require additional delay. For a 7.68MHz master clock, this delay can be as high as 64 modulator clock cycles (64 × 4 × T CLKIN) or 33.3μs. After the setup time (t18 + 256 × T CLKIN), DRDY_N will go low, indicating that the conversion is complete and data can be read using the RDATA command. The DADS1256 establishes itself within a single cycle, without ignoring or discarding data. After the data read cycle, another standby command is issued to reduce power consumption. The cycle repeats from another wake-up command when ready for the next measurement.

Setup time during continuous conversion

After synchronization, input multiplexer change, or wake-up from standby mode, the DADS1256 will continuously switch analog inputs. The switching occurs on the falling edge of DRDY_N. For continuous switching, it is generally more convenient to consider the setup time using the DRDY_N period, as shown in Table 15. The DRDY_N period is equal to the reciprocal of the data rate.

If the input signal undergoes a step change during a continuous conversion, it is recommended to perform a synchronization operation to initiate a new conversion. Otherwise, the next data will represent a combination of the previous and current input signals and should therefore be discarded. Figure 21 shows an example of readback in this case.

Table 15. Relationship between data setup delay and data rate

Data rate (SPS)	Establishment time (DRDY_N cycle)
15,000	3
7500	2
3750	1
2000	1
1000	1
500	1
100	1
60	1
50	1
30	1
25	1
15	1
10	1
5	1
2.5	1

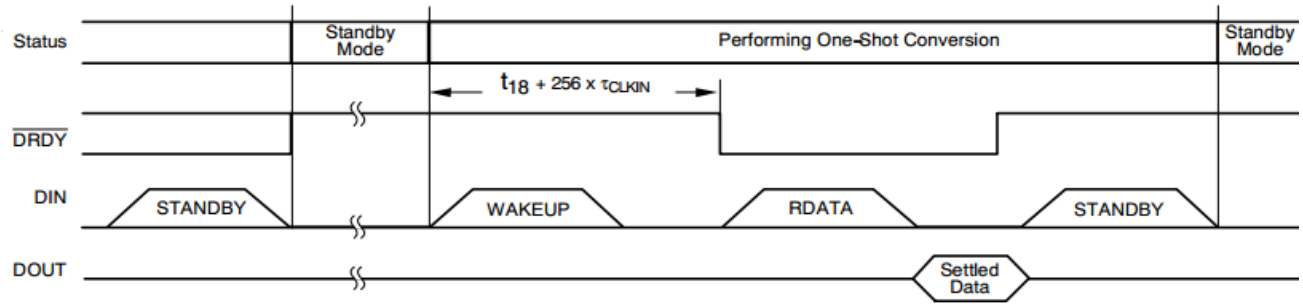


Figure 20. Single conversion using the STANDY command

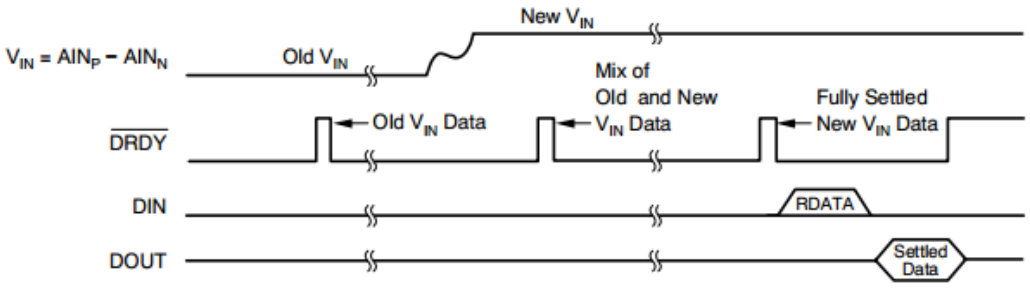


Figure 21. Step change of VIN when the continuous conversion data rate is ≤3750SPS

Data format

The DADS1256 outputs 24-bit data in true binary format. The LSB weight is 2VREF / (PGA(2^23 - 1)). Table 16 summarizes the ideal output codes for different input signals.

Table 16. Relationship between ideal output code and input signal

Input signal VIN(AINP - AINN)	Truth table (1)
$\geq \frac{+2V_{REF}}{PGA}$	7FFFFFh
$\frac{+2V_{REF}}{PGA}\left(\frac{2^{23}-2}{2^{23}-1}\right)$	7FFFFEh
$\frac{+2V_{REF}}{PGA(2^{23}-1)}$	000001h
0	000000h
$\frac{-2V_{REF}}{PGA(2^{23}-1)}$	800001h
$\frac{-2V_{REF}}{PGA}$	FFFFFFh
$\leq \frac{-2V_{REF}}{PGA}\left(\frac{2^{23}}{2^{23}-1}\right)$	800000 h

(1) Ideal output code that eliminates the effects of noise, INL, offset and gain error.

Clock generation

The master clock source for the DADS1256 can be provided using an external crystal oscillator or a clock generator. When using a crystal oscillator to generate the clock, an external capacitor must be provided to ensure the startup and clock frequency, as shown in Figure 22. Any crystal can work with the DADS1256. Table 17 lists two verified crystals. When placing the crystal near the DADS1256 pins, long leads should be minimized.

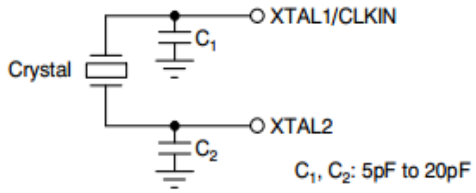


Figure 22. Crystal Oscillator Connection

Table 17. Sample Crystal Oscillators

Manufacturer	Frequency	Part number
Citizen	7.68 MHz	CIA /53383
ECS	8.0 MHz	ECS-80-5-4

When using a crystal oscillator, neither the XTAL1/CLKIN nor XTAL2 pins can be used to drive any other logic. If other devices require a clock source, the D0 pin can be used for this function. When using an external clock generator, provide a clock signal to XTAL1/CLKIN and leave XTAL2 floating. Ensure the external clock generator provides a clean clock waveform. Overshoot and glitches on the clock will degrade overall performance.

Calibration

Using the DADS1256 on-chip calibration circuitry minimizes offset and gain errors. Figure 23 shows the calibration block diagram. Offset error is corrected via the Offset Calibration (OFC) register, and similarly, full-scale error is corrected via the Full-Scale Calibration (FSC) register. Both registers are 24-bit and can be read or written.

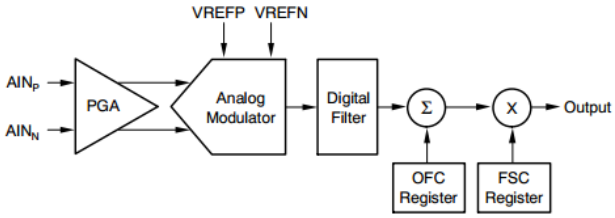


Figure 23 Calibration block diagram

The output of DADS1256 after calibration is shown in Formula3.

Output = (Vin * PGA / (2 * VREF) - OFC / α) * FSC * β(3)

Among them, α and β vary with the data rate setting and the ideal values of OFC and FSC (assuming perfect simulation performance), as shown in Table 18.

The DADS1256 supports self-calibration and system calibration for any PGA setting using a set of five commands: SELFOCAL, SELFGCAL, SELFCAL, SYSOCAL, and SYSGCAL.

Calibration can be performed at any time, although in many applications, the CP 1256's drift performance is very low, requiring only one calibration. Calibration begins when DRDY_N goes high and remains high until the data is ready to be established. No data needs to be discarded after calibration. The DADS1256 performs self-calibration upon reset. Calibration must be performed whenever the data rate changes; it should also be performed when the buffer configuration or PGA changes.

Self-calibration

Self-calibration can correct internal offset and gain errors. During self-calibration, appropriate calibration signals are applied internally to the analog input.

The SELFOCAL instruction performs self-offset calibration. The analog inputs AINP and AINN are disconnected from the signal source and connected to AVDD/2. The time required for self-offset calibration under different data rate settings can be found in Table 19. Like most DADS1256 timings, the calibration time is directly proportional to fCLKIN. Self-offset calibration updates the OFC register.

Table 19. Calibration Time for Self-Offset and System Offset

Data rate (SPS)	Self-off calibration and System offset calibration time
15,000	453 us
7500	587 US
3750	853 us
2000	1.3 ms
1000	2.3 ms
500	4.3 ms
100	20.3 ms
60	33.7 ms
50	40.3 ms
30	67.0 ms
25	80.3 ms
15	133.7 ms
10	200.3 ms
5	400.3 ms
2.5	800.3 ms

Note: f_{CLKIN} = 7.68MHz .

SELFGCAL performs self-gain calibration. The analog inputs AINP and AINN are disconnected from the signal source. AINP is internally connected to VREFP, while AINN is connected to VREFN. Self-gain calibration can be used for any PGA setting. Even at higher PGA settings, the DADS1256 has excellent gain calibration performance, as shown in the typical characteristics section. Using a buffer limits the common-mode range of the reference input during self-gain calibration because they will be connected to the buffer input and must be within the rated analog input range. When the voltage on VREFP or VREFN exceeds the buffer's analog input range (AVDD–2.0V), the buffer must be turned off during self-gain calibration. Otherwise, use system gain calibration or directly write the gain coefficient to the FSC register. Table 20 shows the time required for self-gain calibration at different data rates and PGA settings. Self-gain calibration updates the FSC register.

Table 20. Self -gain calibration timing

Data rate (SPS)	Self-gain calibration time
15,000	484 us
7500	617 us
3750	884 us
2000	1.4 ms
1000	2.3 ms
500	4.3 ms
100	20.3 ms
60	33.7 ms
50	40.3 ms
30	67.0 ms
25	80.3 ms
15	133.7 ms
10	200.3 ms
5	400.3 ms
2.5	800.3 ms

Note: f_{CLKIN} = 7.68MHz .

SELFCAL first performs self-offset calibration, followed by self-gain calibration. During self-calibration, the analog input is disconnected from the signal source. When using an input buffer with self-calibration capability, be sure to observe the common-mode range of the reference input mentioned above. Table 21 shows the time required for self-calibration at different data rate settings. Self-calibration updates the OFC and FSC registers.

Table 21. Self -calibration timing

Data rate (SPS)	Self-gain calibration time
15,000	696 us
7500	896 us
3750	1.3 ms
2000	2.0 ms
1000	3.6 ms
500	6.6 ms
100	31.2 ms
60	50.9 ms
50	61.8 ms
30	101.3 ms
25	123.2 ms
15	202.1 ms
10	307.2 ms
5	613.8 ms
2.5	1227.2 ms

Note: f_{CLKIN} = 7.68MHz.

System calibration

System calibration utilizes the SYSOCAL and SYSGCAL commands to correct internal and external offsets and gain errors. During system calibration, the user must apply appropriate calibration signals to the inputs.

SYSOCAL performs system offset calibration. The user must provide a zero-input differential signal. The DADS1256 then calculates a value that makes the offset in the system zero. Table 19 shows the time required for system offset calibration at different data rate settings. Note that this timing is the same as for self-offset calibration. System offset calibration updates the OFC register.

SYSGCAL performs system gain calibration. The user must provide a full-scale input signal to the DADS1256. The DADS1256 then calculates a value to eliminate gain errors in the system. System gain calibration can correct for inputs of 80% or more of the full-scale input voltage. When using system gain calibration, ensure that the full-scale input voltage is not exceeded. Table 22 shows the time required for system gain calibration at different data rate settings. System gain calibration updates the FSC register .

Table 22. System Gain Calibration Timing

Data rate (SPS)	Self-gain calibration time
15,000	484 us
7500	617 us
3750	884 us
2000	1.4 ms
1000	2.3 ms
500	4.3 ms
100	20.3 ms
60	33.7 ms
50	40.3 ms
30	67.0 ms
25	80.3 ms
15	133.7 ms
10	200.3 ms
5	400.3 ms
2.5	800.3 ms

Note: f_{CLKIN} = 7.68MHz.

Serial interface

The SPI-compatible serial interface consists of four signals: CS_N, SCLK, DIN, and DOUT, allowing the controller to communicate with the DADS1256. Programmable functions are controlled by a set of on-chip registers. Data is written to and read from these registers via the serial interface. The DRDY_N output line serves as a status signal, indicating when a transition is complete. DRDY_N goes low when new data is available. The timing specification shows a timing diagram for interfacing with the DADS1256. The chip select (CS_N) input allows individual selection of the DADS1256 device when multiple devices share the serial bus. CS_N must be held low during serial communication. When CS_N goes high, the serial interface resets, and DOUT enters a high-impedance state. CS_N may be held low indefinitely.

Serial clock (SCLK)

The serial clock (SCLK) has a Schmitt trigger input for inputting data from the DIN and DOUT pins to the DADS1256 or outputting it from the CP1256. Although input hysteresis exists, it is recommended to keep SCLK as clean as possible to prevent accidental data shifting due to glitches. Keep SCLK low when the serial interface is idle.

Data Input (DIN) and Data Output (DOUT)

The data input pin (DIN), along with SCLK, is used to send data to the DADS1256. The data output pin (DOUT), along with SCLK, is used to read data from the DADS1256. Data on DIN is shifted into the device on the falling edge of SCLK, while data on DOUT is shifted out on the rising edge of SCLK.

Data ready (DRDY_N)

The DRDY_N output serves as a status signal, indicating when converted data is available to read. DRDY_N goes low when new converted data is available. It resets to high when all 24 bits have been read back using the Read Data (RDATA) or Read Data Continuous (RDATAC) command. It also goes high while new converted data is being updated. Do not retrieve data during this update period, as the data is invalid. If no data is retrieved, DRDY_N remains high only during the update period, as shown in Figure 24.

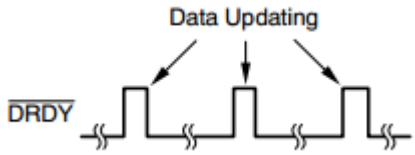


Figure 24. DRDY_N without data retrieval

After changing the PGA, data rate, and buffer state, write to the OFC or FSC register to perform a synchronization operation, forcing DRDY_N high. It will remain high until valid data is ready. Exiting reset, synchronization, standby, or power-down mode will also force DRDY_N high. Once valid data is ready, DRDY_N will go low.

Synchronization

The synchronization function of DADS1256 can be used to coordinate A/D conversion with external events, and can also be used to accelerate the settling time after instantaneous changes in analog input (see the "Conversion Time Using Synchronization" section).

Synchronization can be achieved via the SYNC_PDWN_N pin or the SYNC command. To use the SYNC_PDWN_N pin, pull it low and then high, ensuring it conforms to timing specifications t16 and t16B. Synchronization occurs when SYNC_PDWN_N goes high. The serial interface cannot communicate when SYNC_PDWN_N is low. If the SYNC_PDWN_N pin remains low for 20 DRDY_N cycles, the DADS1256 will enter power-saving mode.

To synchronize using the SYNC command, first shift in all 8 bits of the SYNC command. This will stop the DADS1256 from running. Once synchronized, issue a wake-up command. Synchronization occurs on the first rising edge of the master clock, after the first SCLK used for shifting in the wake-up command. After synchronization, DRDY_N will remain high until valid data is ready, regardless of whether the SYNC_PDWN_N pin is used or the SYNC command is executed.

Standby mode

Standby mode shuts down all analog circuitry and most digital functions. The oscillator continues to run to allow for rapid wake-up. To enter standby mode, issue a standby command. To exit standby mode, issue a WAKEUP command. After exiting standby mode, DRDY_N will remain high until valid data is ready. Standby mode can be used to perform single-sampling conversions; see the "Setup Time Using Single-Sampling Mode" section for details.

Power saving mode

Holding the SYNC_PDWN_N pin low for 20 DRDY_N cycles activates power-saving mode. In power-down mode, all circuitry is disabled, including the oscillator and clock output. To exit power-saving mode, pull the SYNC_PDWN_N pin high. After exiting power-down mode, the DADS1256 crystal oscillator typically requires 30ms to wake up. If using an external clock source, 8192 CLKIN cycles are required before the transition begins.

Reset

There are two methods to reset the CP 1256: the reset _N input pin

and the RESET command .

When using the RESET_N pin, pull it low to force a reset. Before pulling the RESET_N pin back high, ensure that the minimum pulse width timing specification is followed.

The reset command takes effect after all 8 bits are shifted into DIN. The reset is then automatically released. During reset, the configuration registers are initialized to their default state. Self-calibration is recommended after the reset is complete.

Power on

Upon power-up, all configuration registers are initialized to their default states. Self-calibration is then performed automatically. For optimal performance, it is strongly recommended to perform additional self-calibration by issuing the SELFCAL command after the power supply and reference voltage sources have had time to establish final values.

Application Information

The DADS1256 is a very high-resolution analog-to-digital converter. For optimal performance, careful consideration must be given to its supporting circuitry and printed circuit board (PCB) design. Figure 25 shows the basic connections for the DADS1256. It is recommended that the analog and digital power supplies use the same ground plane. This ground plane should be shared with bypass capacitors and analog conditioning circuitry. However, this ground plane should be avoided for high-noise digital devices such as microprocessors. If the DADS1256 uses a separate ground plane, ensure that the analog and digital planes are connected together. There should be no voltage difference between the DADS1256's analog and digital ground pins (AGND and DGND).

As with any precision circuit, use good power supply bypass techniques. Smaller ceramic capacitors work well in parallel with larger tantalum capacitors or larger low-voltage ceramic capacitors. Place capacitors, especially ceramic capacitors, close to the power supply pins. Run digital logic at the lowest possible voltage. This helps reduce coupling back to analog inputs. Avoid digital input ringing. A small resistor (≈100 ohms) in series with the digital pin helps control trace impedance.

When not using the RESET_N or SYNC_PDWN_N inputs, connect them directly to the DADS1256 DVDD pin.

Pay special attention to the reference and analog inputs. These are the most critical circuits. Bypass the reference voltage input with low equivalent series resistance (ESR) capacitors. Make these capacitors as large as possible to maximize the filtering performance of the reference voltage source. Due to the excellent performance of the DADS1256, the reference voltage source can easily limit overall performance if not carefully selected. When using a separate reference voltage source, ensure it has extremely low noise, extremely low drift, and is capable of driving the DADS1256 reference voltage input. For reference voltage sources that are not suitable for directly driving the DADS1256 (e.g., high output impedance reference voltage sources or resistive voltage dividers), use the recommended buffer circuit shown in Figure 26. The ratio measurement sensitivity for the input signal and reference signal tracking each other is slightly lower, but it verifies that the reference signal is clean.

Typically, only a simple RC filter is needed at the input (as shown in Figure 25). This circuit limits high-frequency noise near the modulator frequency; see the Frequency Response section. Avoid using capacitors made with low-grade dielectrics to minimize temperature variations and leakage. Keep input traces as short as possible, place components close to the input pins, and ensure filtering for all used input channels.

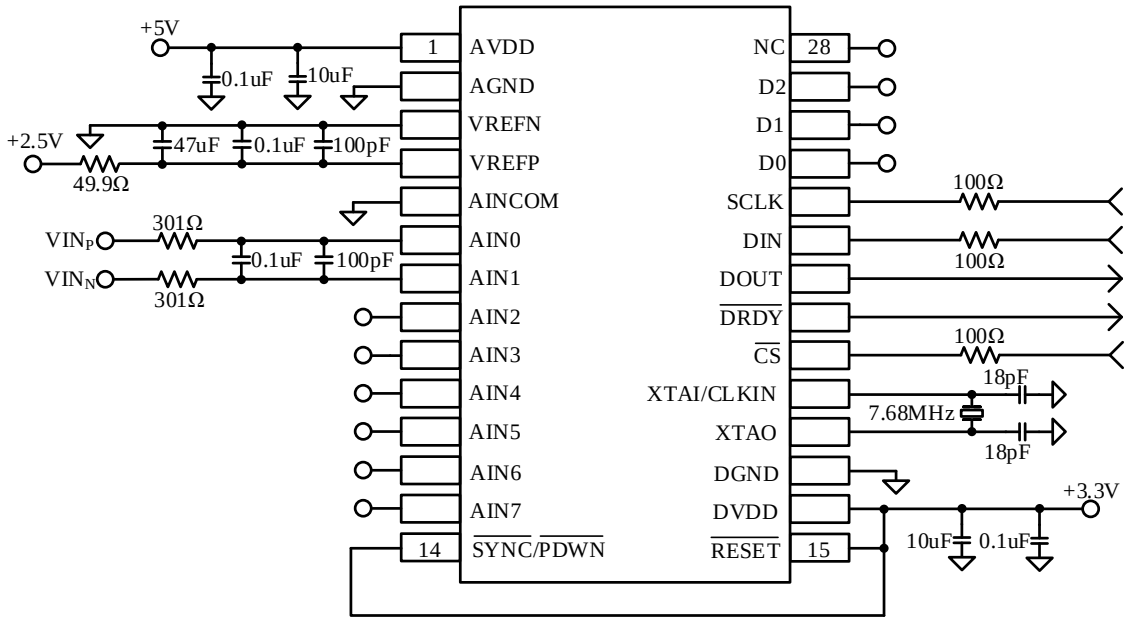


Figure 25. Basic connection of DADS1256

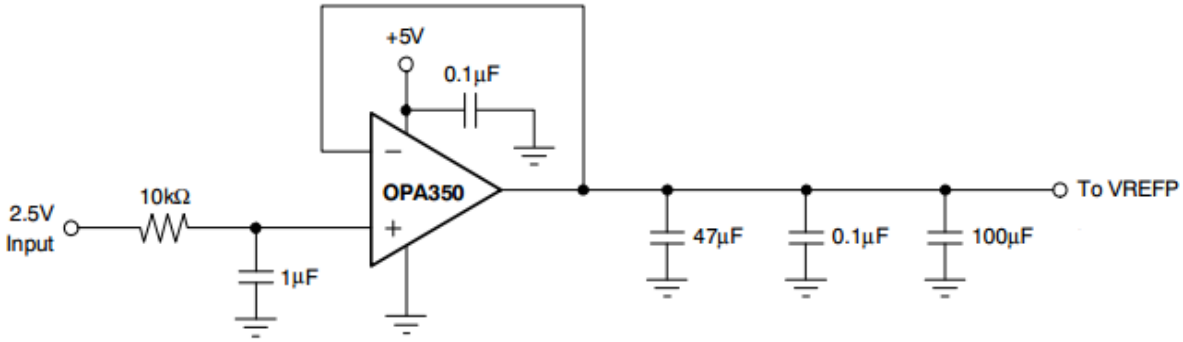


Figure 26. Recommended reference voltage buffer circuit

Digital interface connection

The DADS1256's SPI, QSPI, and MICROWIRE-compatible interfaces allow for easy connection to a wide variety of microcontrollers . Figure 27 shows a basic connection for the TI MSP 430 series low-power microcontrollers. Figure 28 shows connections to microcontrollers with SPI interfaces, such as TI's MSC 12xx series or 68HC11 series. Note that the MSC12xx includes a high-resolution analog-to-digital converter; the DADS1256 can be used to add additional measurement channels or provide higher conversion speeds.

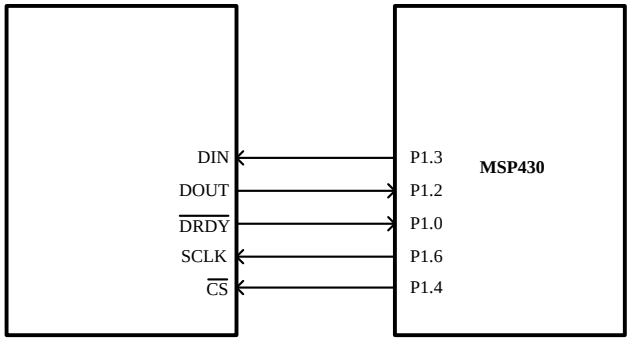


Figure 27. Connection to the MSP430 microcontroller (reference)

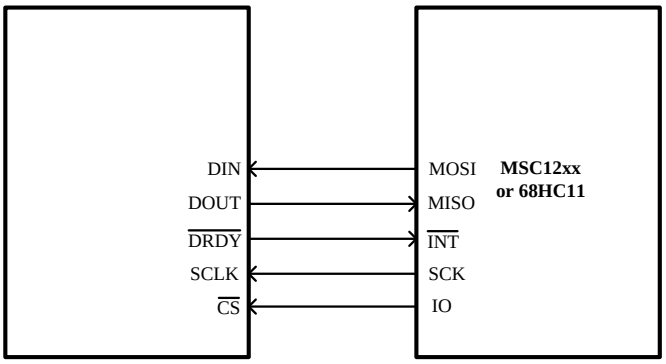


Figure 28. Connecting to a microcontroller via SPI interface (reference)

Register mapping

The DADS1256 operates through a set of registers. These registers collectively contain all the information needed to configure the device, such as data rate, multiplexer settings, PGA settings, calibration, etc., as shown in Table 23.

Table 23 Register Mapping

Address	Register name	Reset value	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	STATUS	A0H	ID3	ID2	ID1	ID0	-	-	BUFEN	-
01h	MUX	01H	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02h	ADCON1	20H	-	-	-	-	-	PGA2	PGA1	PGA0
03h	DRATE	02H	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
05h	OFC0	xxH	OFC 07	OFC 06	OFC 05	OFC 04	OFC 03	OFC 02	OFC 01	OFC 00
06h	OFC1	xxH	OFC 15	OFC 14	OFC 13	OFC 12	OFC 11	OFC 10	OFC 09	OFC 08
07h	OFC2	xxH	OFC 23	OFC 22	OFC 21	OFC 20	OFC 19	OFC 18	OFC 17	OFC 16
08h	FSC0	xxH	FSC 07	FSC 06	FSC 05	FSC 04	FSC 03	FSC 02	FSC 01	FSC 00
09h	FSC1	xxH	FSC 15	FSC 14	FSC 13	FSC 12	FSC 11	FSC 10	FSC 09	FSC 08
0Ah	FSC2	xxH	FSC 23	FSC 22	FSC 21	FSC 20	FSC 19	FSC 18	FSC 17	FSC 16
83H	ADCON2	00H	-	-	-	-	-	PGACON	-	-

STATUS: Status Register (Address 00h)

Reset value = A0h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID3	ID2	ID1	ID0	-	-	BUFEN	-

Bits 7-4, ID3, ID2, ID1, and ID0, are factory programming identification bits (read-only).

Bits 3-2 are reserved and always set to 0 (read-only).

Bit 1BUFEN: Input buffer control bit:

0 = Disable input buffer (default)

1 = Enable input buffer.

Bit 0 is reserved and always set to 1 (read-only).

MUX: Input Multiplexer Control Register (Address 01h)

Reset value = 01h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

Bits 7-4 PSEL3, PSEL2, PSEL1, PSEL0: Positive Input Channel (AINP) Selection

0000 = AIN0 (default)

0001 = AIN1

0010 = AIN2

0011 = AIN3

0100 = AIN4

0101 = AIN5

0110 = AIN6

0111 = AIN7

1xxx = AINCOM (when PSEL3 = 1, PSEL2, PSEL1, PSEL0 are "irrelevant")

Bits 3-0 NSEL3, NSEL2, NSEL1, NSEL0: Negative Input Channel (AINN) Selection

0000 = AIN0

0001 = AIN1 (default)

0010 = AIN2

0011 = AIN3

0100 = AIN4

0101 = AIN5

0110 = AIN6

0111 = AIN7

1xxx = AINCOM (When NSEL3 = 1, NSEL2, NSEL1, and NSEL0 are "irrelevant")

ADCON 1: Modular-to-Digital Control Register 1 (Address 02h)

Reset value = 20h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PGA2	PGA1	PGA0

Bits 7-3 are reserved (read-only)

Bits 2-0PGA2, PGA1, PGA0: Programmable gain amplifier settings

000 = 1 (default)

001 = 2

010 = 4

011 = 8

100 = 16

101 = 32

110 = 64

111 = 64

DRATE: Output rate (address 03h)

Reset value = 02h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

The 16 valid data rate settings are shown below. Please ensure that a valid setting is selected, as invalid settings may produce unpredictable results.

Bits 7-0DR[7: 0]: Data rate setting (1)

0000 0010 = 15000 SPS (default)

0000 0011 = 7500 SPS

0000 0100 = 3750 SPS

0000 0101 = 1875 SPS

0000 0110 = 1000 SPS

0000 0111 = 500 SPS

0000 1000 = 100 SPS

0000 1001 = 60 SPS

0000 1010 = 50 SPS

0000 1011 = 30 SPS

0000 1100 = 25 SPS

0000 1101 = 15 SPS

0000 1110 = 10 SPS

0000 1111 = 5 SPS

0001 0000 = 2.5 SPS

(1) For f_{CLKIN} = 7.68MHz, the data rate is linearly proportional to f_{CLKIN}.

OFC0: Offset calibration byte 0, least significant byte (address 05h)

The reset value depends on the calibration result.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00

OFC1: Offset calibration byte 1 (address 06h)

The reset value depends on the calibration result.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08

OFC2: Offset calibration byte 2, most significant byte (address 07h)

The reset value depends on the calibration result.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16

FSC0: Full-scale calibration byte 0, least significant byte (address 08h)

The reset value depends on the calibration result.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSC 07	FSC 06	FSC 05	FSC 04	FSC 03	FSC 02	FSC 01	FSC 00

FSC 1: Full-scale calibration byte 1 (address 09h)

The reset value depends on the calibration result.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSC 15	FSC 14	FSC 13	FSC 12	FSC 11	FSC 10	FSC 09	FSC 08

FSC2: Full-scale calibration byte 2, most significant byte (address 0Ah)

The reset value depends on the calibration result.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSC 23	FSC 22	FSC 21	FSC 20	FSC 19	FSC 18	FSC 17	FSC 16

ADCON 2: Modular-to-Digital Control Register 2 (Address 83h)

Reset value = 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PGACON	-	-

Bits 7-3 and 1-0 are reserved and always equal to 0 (read-only).

Bit 2PGACON: PGA control bit

0 = When PGA = 1, 2, 4, 8, 16 (default)

1 = This position is 1 when PGA=32 and 64.

Command definition

Table 24 summarizes the command control operation of the DADS1256. Additional command and data bytes can be shifted in without delay after the first command byte. CS_N must be held low throughout the command sequence.

Table 24. Command Definitions

Command	Description	1st command byte	2nd command byte	3rd command byte
WAKE UP	Complete synchronization and exit standby mode	0000 0000(00h)	-	-
RDATA	Read data	0000 0001(01h)	-	-
RDATAC	Continuous data reading	0000 0011(03 h)	-	-
SDATAC	Stop continuously reading data	0000 1111(0Fh)	-	-
RREG	Read from register rrr	0001 adrh (1) (1xh)	adrl (2) xxxx (3)	dddddddd (4)
WREG	Write to register rrr	0101 adrh (5xh)	adrlxxxx	dddddddd
SELFCAL	Offset and gain self-calibration	0101 0010(52h)	1110 0000(E0h)	0000 0101(05 h)
SELFOCAL	Imbalance Self-calibration	0101 0010(52h)	1110 0000(E0h)	0000 0001(01 h)
SELFGCAL	Gain self-calibration	0101 0010(52h)	1110 0000(E0h)	0000 0010(02h)
SYSOCAL	System offset calibration	0101 0010(52h)	1110 0000(E0h)	0000 0011(03 h)
SYSGCAL	System gain calibration	0101 0010(52h)	1110 0000(E0h)	0000 0100(04h)
SYNC	Synchronous Analog-to-Digital Conversion	1111 1100(FCh)	-	-
STANDBY	Start standby mode	1111 1101(FDh)	-	-
RESET	Reset to power-on value	1111 1110(FEh)	-	-
WAKE UP	Complete synchronization and exit standby mode	1111 1111(FFh)	-	-

Notice:

(1) adrh = the high four bits of the target register address.

(2) adrl = the lower four bits of the target register address.

(3) xxxx = can be set to any value.

(4) dddddddd = data to be read or written .

RDATA: Read data

Description: This command is issued after DRDY_N goes low to read a single conversion result. DRDY_N goes high after all 24 bits have been converted to the dot output. It is not necessary to read back all 24 bits, but DRDY_N will not return high until new data is updated. See the timing characteristics for the required delay between the end of the RDATA command and the start of the data shift on DOUT: t6.

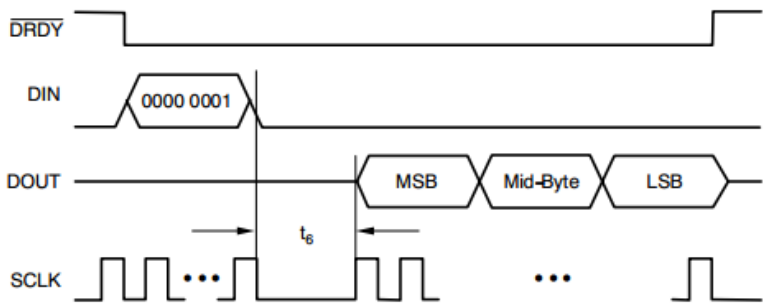


Figure 30 RDATA command sequence

RDATAC: Continuous data reading

Description: A command is issued after DRDY_N goes low to enter continuous read mode. This mode allows for continuous output of new data on each DRDY_N without issuing subsequent read commands. DRDY_N goes high after all 24 bits have been read. It is not necessary to read back all 24 bits, but DRDY_N will not return to high until new data is updated. This mode can be terminated by the Stop Continuous Read Command (SDATAC). Because DIN is continuously monitored in continuous read mode under SDATAC or RESET commands, this mode should not be used if DIN and DOUT are connected together.

In Figure 31, the delay between the second falling edge of DRDY_N and the next rising edge t18 of SCLK should be at least 500ns. See the timing characteristics for the required delay between the end of the RDATAC command and the start of the data shift on DOUT: t6.

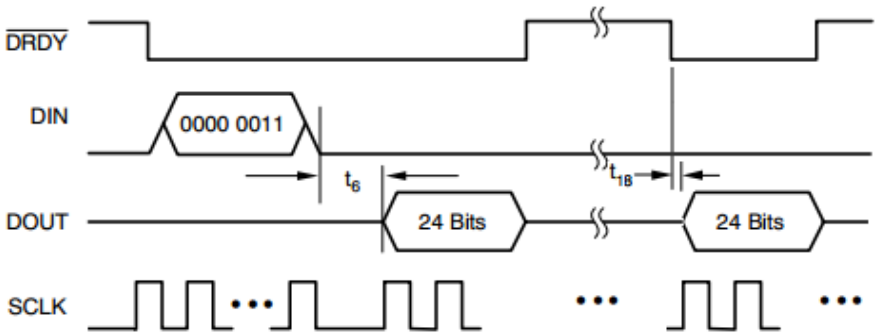


Figure 31 RDATAC command sequence

On the next DRDY_N, data is shifted out by applying SCLKs. The continuous data reading mode terminates if input_data equals any of the three bytes on DIN via an SDATAC or RESET command.

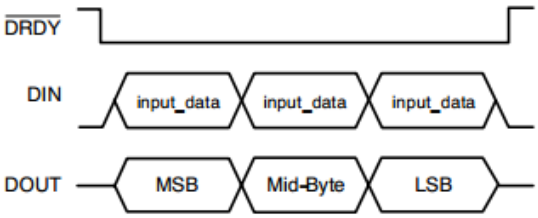


Figure 32. DIN and DOUT command sequences in continuous read mode

SDATAC: Stop continuous data reading

Description: Ends continuous data output mode. (See RDATAC). This command must be issued after DRDY_N goes low and completed before DRDY_N goes high.

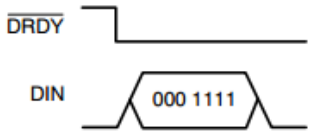


Figure 33SDATAC command sequence

RREG: Read from register

Description: Output data from the register.

The first command byte: 0001 adrh , where adrh is the high four bits of the address of the register to be read.

The second command byte: adrl xxxx , where adrl is the lower four bits of the register address to be read, and xxxx can be set to any value.

See DOUT: t6 for the timing characteristics of the delay required between the end of the RREG command and the start of the data shift.

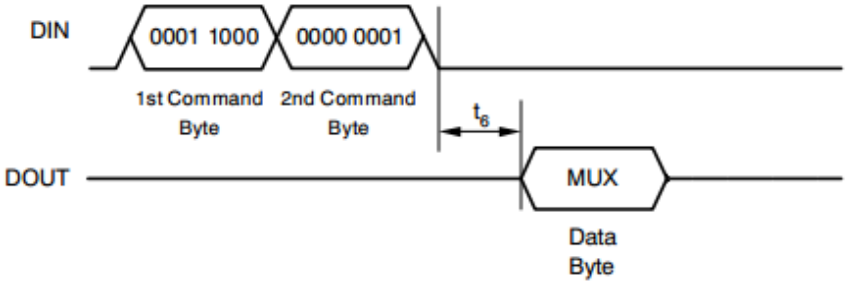


Figure 34 RREG command example: Reading from register 80h (multiplexer)

Write to register

Description: Writes to the register specified by three command bytes.

The first command byte: 0101 adrh , where adrh is the high four bits of the register address to be written.

The second command byte: adrl xxxx , where adrl is the lower four bits of the register address to be written, and xxxx can be set to any value.

The third command byte (data byte): the data to be written to the register.

Figure 35 shows an example of the WREG command: writing data to 80h (multiplexer).

SELFCAL: Self-Offset and Gain Calibration

Description: Performs offset and gain calibration. The offset calibration register (OFC) and full-scale calibration register (FSC) are updated after this operation. DRDY_N goes high at the start of calibration. It goes low once calibration is complete and the established data is ready. Do not send any other commands after issuing this command until DRDY_N goes low, indicating calibration is complete.

Self-focusing: Self-Offset Calibration

Description: Performs self-offset calibration. The Offset Calibration Register (OFC) is updated after this operation. DRDY_N goes high at the start of calibration. It goes low once calibration is complete and the established data is ready. Do not send other commands after issuing this command until DRDY_N goes low, indicating calibration is complete.

SELFGCAL: Self-Gain Calibration

Description: Perform self-gain calibration. Upon completion, the Full-Scale Calibration Register (FSC) will be updated to its new value. DRDY_N goes high at the start of calibration. It goes low once calibration is complete and the established data is ready. Do not send any other commands after issuing this command until DRDY_N goes low, indicating calibration is complete.

System Offset Calibration

Description: Perform system offset calibration. The Offset Calibration Register (OFC) will be updated after this operation. DRDY_N goes high at the start of calibration. It goes low once calibration is complete and the established data is ready. Do not send any other commands after issuing this command until DRDY_N goes low, indicating calibration is complete.

SYSGCAL: System Gain Calibration

Description: Perform system gain calibration. The Full Scale Calibration Register (FSC) will be updated after this operation. DRDY_N goes high at the start of calibration. It goes low once calibration is complete and the established data is ready. Do not send any other commands after issuing this command until DRDY_N goes low, indicating calibration is complete.

Synchronization: Synchronous Analog-to-Digital Conversion

Description: This command synchronizes the A/D conversion. To use it, first shift in the command prompt. Then type the wake-up command. Synchronization occurs on the first rising edge of CLKIN after the first SCLK used for shifting in the wake-up command.

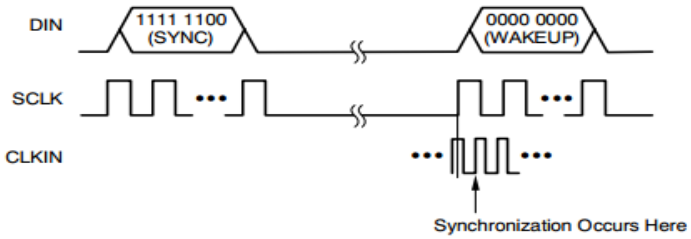


Figure 36. Synchronization command sequence

Standby: Standby Mode / Single Use Mode

Description: This command puts the DADS1256 into low-power standby mode. After issuing the standby command, ensure there is no activity on SCLK while CS_N is low, as this will interrupt standby mode. If CS_N is high, SCLK activity is allowed in standby mode. To exit standby mode, issue the WAKEUP command. This command can also be used to perform a single conversion (see the "Single Sampling Mode" section).

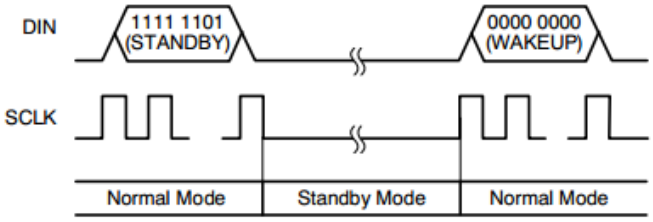


Figure 37. Alternate command sequence

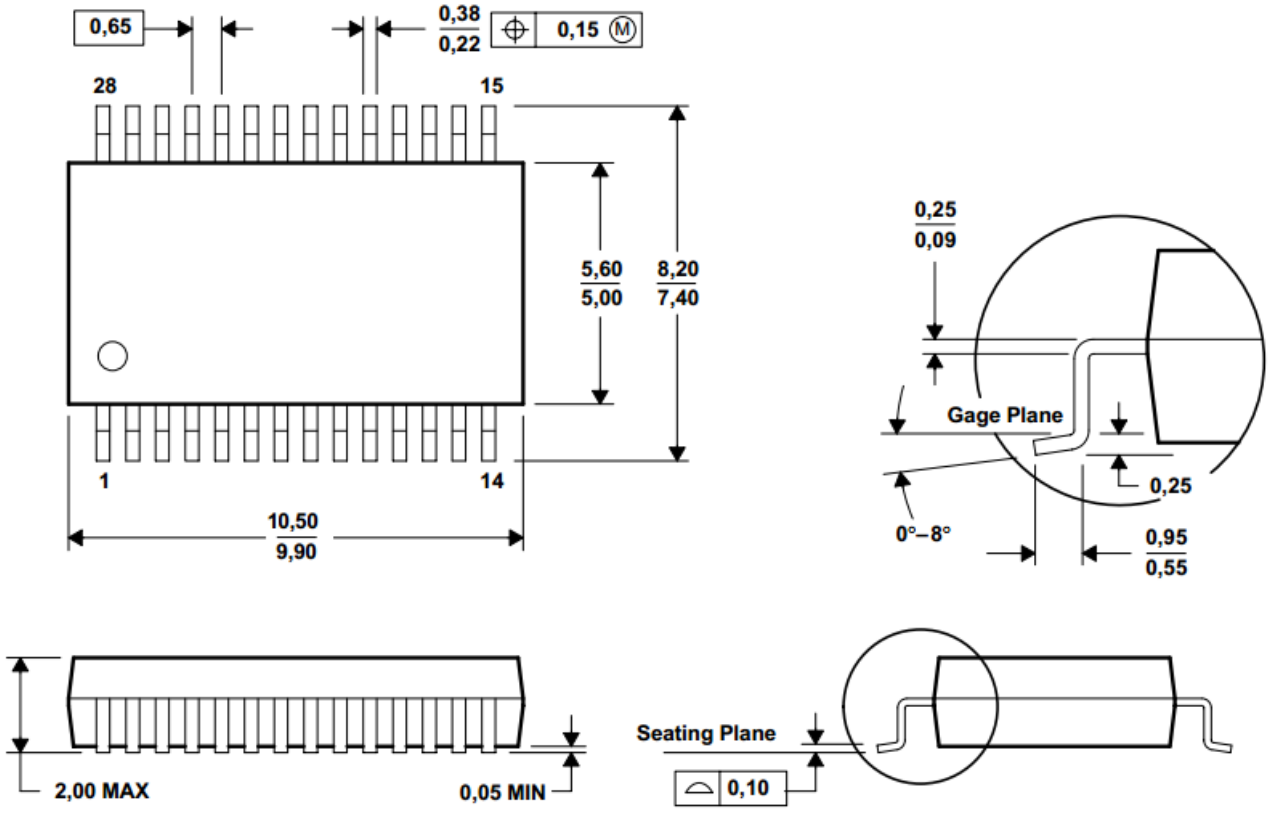
Wake Up: Complete Synchronization or Exit Standby Mode

Description: Used with the SYNC and STANDBY commands. This command has two values (all zeros or all one).

Reset: Resets the Registers to Default Values

Description: Restores all registers in the ADCON1 register except for the CLK0 and CLK1 bits to their default values. This command also stops continuous read mode: in this case, a RESET command is issued after DRDY_N goes low.

28-Pin SSOP28 Package Dimensions Information



Device Ordering Information List

Product Model	Temperature range	Packaging	Package	ROHS
DADS1256	-40°C to +85°C	2 8-SSOP	1,000/tray	Y