DADS1248 Low Noise, 24-Bit ADC

Features

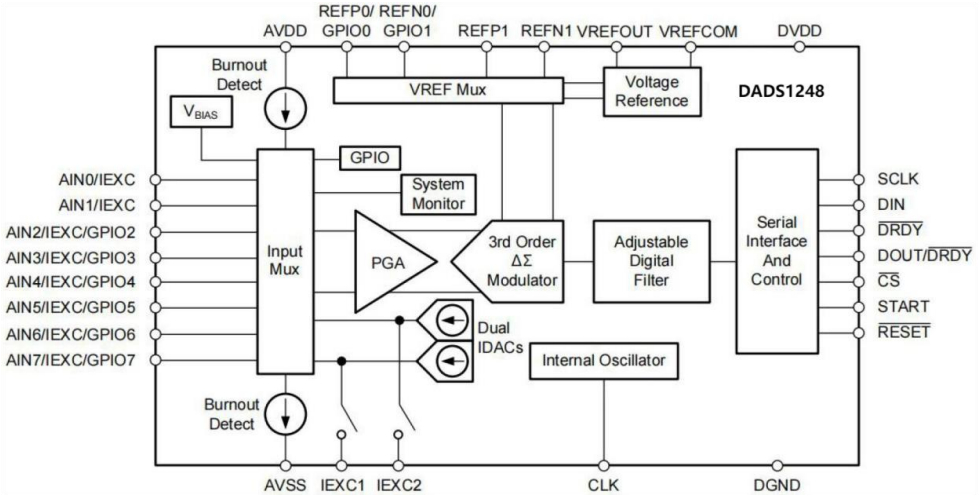
- Programmable data rate: up to 2kSPS
- Single-cycle setup for all data rates
- Achieve 50Hz and 60Hz harmonic suppression at 20SPS
- Analog multiplexer with 8 independently selectable inputs
- Low-noise programmable gain amplifier: 48nVRMS when PGA=128
- Two matched programmable excitation current sources
- Integrated low-drift 2.048V reference voltage: 10ppm/°C
- Sensor failure detection
- 8 general purpose input /output interfaces
- Built-in temperature sensor:
- Power supply and reference voltage monitoring
- Self-calibration and system calibration
- SPI interface compatible
- Analog power supply: unipolar (2.7V) to 5.25V) and bipolar (±2.5V) operating voltage
- Digital power supply: 2.7V to 5.25V

Applications

- Temperature sensor measurement:
- Resistance temperature detectors (RTDs), thermocouples and thermistors
- Pressure measurement
- Flow meter
- Factory automation and process control

Description

The DADS1248 is a precision 24-bit analog-to-digital converter (ADC) that includes numerous integrated features to reduce system cost and component count for sensor measurement applications. This chip features a low-noise programmable gain amplifier (PGA), a single-cycle digital filter, a high-precision Delta-Sigma (ΔΣ) A/D converter, and an internal oscillator. The DADS1248 also provides a built-in, low-drift reference voltage and two matched programmable excitation current sources (IDACs). The DADS1248's input analog multiplexer supports four differential inputs. Furthermore, this multiplexer integrates sensor failure detection, thermocouple voltage biasing, system monitoring, and general-purpose digital I/O. The programmable gain amplifier (PGA) offers selectable gain up to 128x. These features provide a complete front-end solution for temperature sensor measurement applications, including thermocouples, thermistors, and resistance temperature detectors (RTDs), as well as other small-signal measurements including resistance bridge sensors. The digital filter enables single-cycle setup to support fast channel cycling when using the input multiplexer and provides data rates up to 2kSPS. For data rates of 20 SPS or lower, the filter will suppress power frequency interference at 50Hz and 60Hz



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Absolute Maximum Ratings

Unless otherwise stated, operate within the room temperature range (1).

		Min	Max	Unit
Power supply voltage	AVDD to AVSS	-0.3	5.5	V
	AVSS to DGND	-2.8	0.3	
	DVD to DGND	-0.3	5.5	
Analog input voltage	AINx, REFPx, REFNx, VREFOUT, VREFCOM, IEXC1, IEXC2	AVSS-0.3	VDD+0.3	V
Digital input voltage	SCLK, DIN, DOUT/DRDY, DRDY, CS, START, RESET, CLK	DGND-0.3	DVDD+0.3	V
Input current	Continuous, any pin except power supply pins	-10	10	mA
	Instantaneously, any pin except the power supply pin	-100	100	
Temperature	Junction temperature, TJ		150	₤
	Storage, Tstg	-60	150	

Stress values exceeding the absolute maximum ratings listed below may cause permanent damage to the device. These are operating conditions only at the stress ratings; functional operation of the device at the ratings and any other operation beyond the recommended operating conditions are not described here. Prolonged operation at the absolute maximum ratings will affect device reliability.

Electrical Characteristics

Minimum and maximum specification values apply to a temperature range of TA = -40 °C to +125°C. Typical specification values were determined at TA = 25°C. All specification values are at AVDD = 5 V, DVDD = 3.3 V, AVSS = 0 V, external VREF = 2.048 V, and fCLK = 4.096 MHz (unless otherwise noted) .

Parameter	Test conditions	Min	Typ	Max	Unit
Analog Input					
Differential input current			100		pA
Absolute input current			See Table 8		
PGA					
PGA gain settings			1, 2, 4, 8, 16, 32, 64, 128		V/V
System performance					
Resolution		24			Bits
DR data transfer rate			5, 10, 20, 40, 80, 160, 320, 640, 1000, 2000		SPS
ADC conversion time			Single cycle		
INL Integral Nonlinearity	Differential input, endpoint fitting, gain = 1, VCM = 2.5 V		6	15	ppm
V_{IO} input offset voltage	After calibration (1)	-15		15	uV
Offset Drift			See Figures 9 to 12		
Gain error	TA = 25°C, All Gain DR = 40 SPS, 80 SPS, or 160 SPS	-0.02%	±0.005%	0.02%	
Gain drift			See Figures 17 to 20		
Noise			See Tables 1 to 4		
NMRR Normative Suppression Ratio			See Table10		
CMRR (Common Mode Rejection Ratio)	Gain under DC conditions = 1	80	90		dB
	Gain under DC conditions = 32	90	125		
PSRR (Power Supply Rejection Ratio)	AVDD/DVDD DC gain = 32, bitrate = 80 SPS	100	135		dB
Voltage reference input					
Reference input current			30		nA
Internal reference benchmark					
V REF internal reference voltage		2.038	2.048	2.058	V
Reference drift (2)	T A = 25°C to 105°C		2	10	ppm/°C
	T A = -40°C to 105°C		6	15	ppm/°C
Output current (3)		– 10		10	mA
Load regulation			50		μV/mA
Startup time			See Table 11		
Internal oscillator					
Internal oscillator frequency		3.89	4.096	4.3	MHz
Excitation current sources (IDACs)					
Output current setting			50, 100, 250, 500, 750, 1000, 1500		μA
Compliant voltage	All current settings				
Absolute error	All current settings, per IDAC	– 6%	±1%	6%	
Absolutely no match	All current settings, between IDACs		±0.15%		
Temperature drift	Each IDAC		100		ppm/°C
Temperature drift matching	Between IDACs		10		ppm/°C
Failure Current Source					
Failure current source setting			0.5, 2, 10		μA

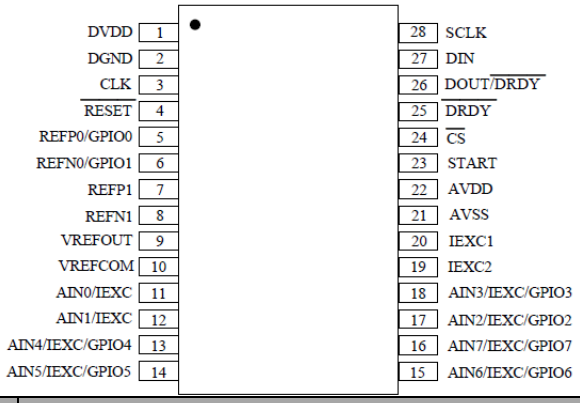
1. Noise level misalignment calibration
2. Specified by a combination of design and final production testing
3. Do not exceed the load of the internal reference voltage source

Electrical Characteristics (continued)

Minimum and maximum specification values apply to a temperature range of TA = -40 °C to +105°C. Typical specification values were determined at TA = 25°C. All specification values are at AVDD = 5V, DVDD = 3.3V, AVSS = 0V, external VREF = 2.048V, and fCLK = 4.096MHz (unless otherwise noted).

Parameter	Test conditions	Min	Typ	Max	Unit
Bias voltage					
Bias voltage			(AVDD + AVSS) / 2		V
Bias voltage output impedance			400		Ω
Temperature sensor					
Output voltage	TA = 25°C		118		mV
Temperature coefficient			405		uA/℃
General Purpose Input / Output (GPIO)					
V_{IL} Low-level input voltage		AVSS		0.3×AVDD	V
V_{IH} High-level input voltage		0.7×AVDD		AVDD	V
V_{OL}Low-level output voltage	I_{OL} = 1 mA			0.2×AVDD	V
V_{OH} High-level output voltage	I_{OH} = 1 mA	0.8×AVDD			V
Digital inputs / outputs (Besides GPIO)					
V_{IL} Low-level input voltage		DGND		0.3 ×DVDD	V
V_{IH} High-level input voltage		0.7 × DVDD		DVDD	V
V_{OL} Low-level output voltage	I_{OL} = 1 mA	DGND		0.2 × DVDD	V
V_{OH} High-level output voltage	I_{OH} = 1 mA	0.8×DVDD			V
Input leakage	DGND < VIN < DVDD	−10		10	μA
Power supply					
I_{AVDD} analog power supply current	Power saving mode		0.1		μA
	Normal conversion mode , AVDD=3.3V, DR=20 SPS. When selecting an external reference		200		
	Normal conversion mode , AVDD=5V, DR=20 SPS. When selecting an external reference		225		
	Additional current when internal reference voltage is enabled		180		
I_{DVDD} digital power supply current	Power saving mode		0.2		μA
	Normal mode, DVDD=3.3V, DR =20SPS, internal oscillator		210		
	Normal mode, DVDD=5V, DR=20SPS, internal oscillator		230		
Power consumption	AVDD=DVDD=5V, DR=20SPS, internal oscillator, external reference		2.3		mW
	AVDD=DVDD=3.3V, DR=20SPS, internal oscillator, external reference		1.4		

TSSOP28 Package Pin Definition



Pin Name	Pin No.	Function	Description
DVDD	1	Power supply	A 0.1uF capacitor is connected between the positive digital power supply and DGND.
DGND	2	Ground	Digital ground
CLK	3	Input	External clock source pin. If this pin is not used, it is connected to DGND.
RESET	4	Input	Reset (active low)
REFP0/GPIO0	5	Input/Output	Positive external reference voltage input 0 or general purpose digital input/output pin 0
REFN0/GPIO1	6	Input/Output	Negative external reference voltage input 0 or general purpose digital input/output pin 1
REFP1	7	Input	Positive external reference voltage input 1
REFN1	8	Input	Negative external reference voltage input 1
VREFOUT	9	Output	Positive internal reference voltage output; connect a capacitor ranging from 1uF to 47uF to VREFCOM.
VREFCOM	10	Output	The output is a negative internal reference voltage. When using a unipolar power supply, it is connected to the AVSS; when using a bipolar power supply, it is connected to the intermediate voltage of the power supply.
AIN0/IEXC	11	Input	Analog input 0, selectable excitation current output
AIN1/IEXC	12	Input	Analog input 1, selectable excitation current output
AIN4/IEXC/GPIO4	13	Input/Output	4 analog inputs, optional drive current output, or 4 general purpose digital inputs/outputs (GPIOs).
AIN5/IEXC/GPIO5	14	Input/Output	Analog input 5, optional excitation current output, or general purpose digital input/output GPIO5
AIN6/IEXC/GPIO6	15	Input/Output	Analog inputs 6, optional drive current output, or general purpose digital input/output GPIO 6
AIN7/IEXC/GPIO7	16	Input/Output	Analog input 7, optional drive current output, or general purpose digital input/output GPIO7
AIN2/IEXC/GPIO2	17	Input/Output	Analog input 2, optional excitation current output, or general purpose digital input/output GPIO2
AIN3/IEXC/GPIO3	18	Input/Output	Analog input 3, optional excitation current output, or general purpose digital input/output GPIO3
IEXC2	19	Output	Excitation current source output 2
IEXC1	20	Output	Excitation current source output 1
AVSS	21	Power supply	Negative analog power supply
AVDD	22	Power supply	Positive analog power supply
TART	23	Input	Start conversion
CS	24	Input	Chip select; active low
DRDY	25	Output	Data ready, active low
DOUT/DRDY	26	Output	Serial data output in conjunction with data ready; active low.
DIN	27	Input	Serial data input
SCLK	28	Input	Serial clock input

Switching Characteristics

Operating ambient temperature TA = -40 °C to 105 °C and DVDD = 2.7 V to 5.5 V (unless otherwise noted; see Figures 1 and 2).

Parameter	Test conditions	Min	Typ	Max	Unit
tDOPD propagation delay time, from the rising edge of SCLK to the valid new DOUT	DVDD ≥ 3.6V		50		ns
	DVDD > 3.6V		180		
tDOHDDOUT retention time			0		ns
The propagation delay time of tCSDO, from the rising edge of CS to the high-impedance state of DOUT			10		ns
tPWH pulse duration, DRDY high level			3		tCLK

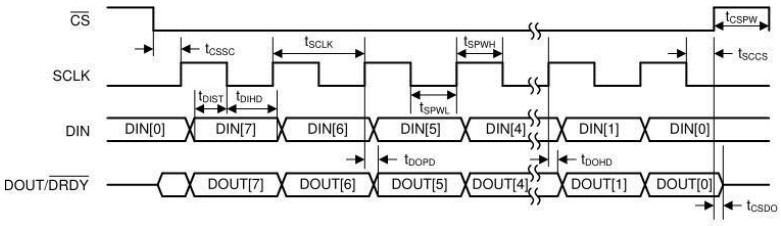
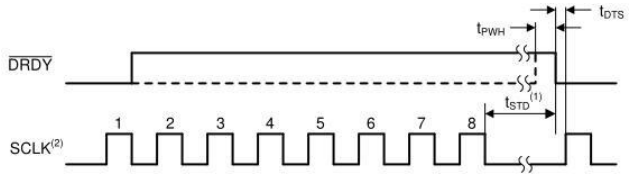


Figure 1. Serial interface timing, DRDY mode bit = 0



(1) This timing diagram only applies when the CS pin is low. When CS is high, SCLK does not need to be low during tSTD.
(2) During partial retrieval of output data, SCLK can only be sent in multiples of eight.

Figure 2. Serial interface timing for allowing loading conversion results

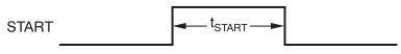


Figure 3. Minimum start pulse duration

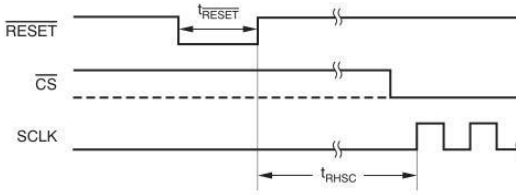


Figure 4. Reset pulse duration and serial interface after reset

Noise Performance

Optimize ADC noise performance by adjusting the data rate and PGA settings. Typically, use the highest gain that matches the input signal range to achieve the lowest input noise. Do not set the gain too high to prevent the ADC output from going out of range. Noise also depends on the output data rate; as the data rate decreases, the ADC bandwidth decreases accordingly. A reduction in total bandwidth results in a reduction in overall noise. From table 1 to table 6 summarize the device's noise performance. These data represent typical noise performance at TA=25°C. The data shown are the result of averaging readings from multiple chips, with the input signal shorted during measurement. At least 128 consecutive readings are required to calculate each root mean square noise (RMS) and peak (PP) noise.

Tables 1, 3, and 5 list the input noise in μVRMS and μVPP. Tables 2, 4, and 6 list the corresponding ENOB data (significant bits), where the ENOB for RMS noise is defined by Equation 1:

$$ENOB=\ln((2\cdot V_{REF}/Gain)/V_{NRMS})/\ln(2) \quad (1)$$

Among them V_{NRMS} = The equivalent RMS noise voltage of the input is used to calculate the peak-to-peak noise ENOB in the same way.

Table 1. Noise levels, in μVRMS and (μVPP)

Conditions: AVDD=5V, AVSS=0V, External reference voltage=2.5V

Data transfer rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
5	1.1 (4.99)	0.68 (3.8)	0.37 (1.9)	0.19 (0.98)	0.1 (0.44)	0.07 (0.31)	0.05 (0.27)	0.05 (0.21)
10	1.53 (8.82)	0.82 (3.71)	0.5 (2.69)	0.27 (1.33)	0.15 (0.67)	0.08 (0.5)	0.06 (0.36)	0.07 (0.34)
20	2.32 (13.37)	1.23 (6.69)	0.71 (3.83)	0.34 (1.9)	0.18 (1.01)	0.12 (0.71)	0.10 (0.51)	0.09 (0.54)
40	2.72 (17.35)	1.33 (7.65)	0.68 (3.83)	0.38 (2.21)	0.22(1.13)	0.14 (0.77)	0.15 (0.78)	0.14 (0.76)
80	3.56 (22.67)	1.87 (12.3)	0.81 (5.27)	0.5 (3.49)	0.3 (1.99)	0.19 (1.24)	0.19 (1.16)	0.18 (1.04)
160	5.26 (42.03)	2.52 (17.57)	1.32 (9.22)	0.67 (5.25)	0.41 (2.89)	0.26 (1.91)	0.27 (1.74)	0.26 (1.74)
320	9.39 (74.91)	4.68 (39.48)	2.69 (18.95)	1.24 (9.94)	0.68 (5.25)	0.45 (3.08)	0.38 (2.71)	0.36 (2.46)
640	13.21 (119.66)	6.93 (59.31)	3.59 (28.55)	1.53 (10.68)	0.95 (8.7)	0.63 (4.94)	0.53 (3.74)	0.5 (3.55)
1000	32.34 (443.91)	16.11 (185.67)	11.54 (92.23)	4.65 (37.55)	2.02 (23.14)	1.15 (12.29)	0.77 (7.42)	0.64 (4.98)
2000	32.29 (372.54)	15.99 (182.27)	8.02 (91.73)	4.08 (45.89)	2.19(24.14)	1.36 (12.32)	1.08 (8.03)	1.0 (6.93)

Table 2. ENOB (Peak-to-Peak Noise) derived from root mean square (RMS) noise.

Conditions: AVDD=5V, AVSS=0V, External reference voltage=2.5V

Data transfer rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
5	22.1(19.9)	21.8(19.3)	21.7(19.3)	21.6 (19.3)	21.6(19.4)	21.1(18.9)	20.6(18.1)	19.6(17.5)
10	21.6(19.1)	21.5(19.4)	21.3(18.8)	21.1(18.8)	21(18.8)	20.9(18.3)	20.3(17.7)	19.1(16.8)
20	21(18.5)	21(18.5)	20.7(18.3)	20.8 (18.3)	20.7(18.2)	20.3(17.7)	19.6(17.2)	18.7(16.1)
40	20.8(18.1)	20.8(18.3)	20.8(18.3)	20.6 (18.1)	20.4(18.1)	20.1(17.6)	19(16.6)	18.1(15.6)
80	20.4(17.8)	20.4(17.6)	20.6(17.9)	20.3 (17.5)	20(17.3)	19.6(16.9)	18.6(16)	17.7(15.2)
160	19.9(16.9)	19.9 (17.1)	19.9(17)	19.8 (16.9)	19.5(16.7)	19.2(16.3)	18.1(15.5)	17.2(14.5)
320	19(16)	19(16)	18.8(16)	18.9 (15.9)	18.8(15.9)	18.4 (15.6)	17.6(14.8)	16.7(14)
640	18.5(15.4)	18.5 (15.4)	18.4 (15.4)	18.6 (15.8)	18.3(15.1)	17.9 (14.9)	17.2(14.4)	16.3(13.4)
1000	17.2(13.5)	17.2(13.7)	16.7 (13.7)	17(14)	17.2(13.7)	17.1(13.6)	16.6(13.4)	15.9(12.9)
2000	17.2(13.7)	17.3(13.7)	17.2(13.7)	17.2(13.7)	17.1(13.7)	16.8(13.6)	16.1(13.2)	15.3(12.5)

Table 3. Noise levels, in μV RMS and (μV P).

Conditions: AVDD=5V, AVSS=0V, Internal reference voltage=2.048V

Data transfer rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
5	1.35 (7.78)	0.7 (4.17)	0.35 (2.03)	0.17 (0.95)	0.1 (0.53)	0.06(0.32)	0.05(0.31)	0.05(0.29)
10	1.8 (10.82)	0.88 (5.26)	0.5 (2.75)	0.24 (1.47)	0.13 (0.8)	0.09(0.49)	0.07(0.39)	0.07 (0.4)
20	2.62 (14.32)	1.22 (7.05)	0.66 (3.88)	0.35 (2.05)	0.19 (1.09)	0.12(0.66)	0.1 (0.61)	0.1 (0.55)
40	2.64 (16.29)	1.34 (7.75)	0.69 (4.06)	0.35 (2.07)	0.21(1.15)	0.15(0.85)	0.14(0.81)	0.13(0.75)
80	3.69 (23.62)	1.82 (10.81)	0.89 (5.48)	0.51 (2.68)	0.3 (1.69)	0.21(1.32)	0.2 (1.09)	0.18(0.98)
160	5.7 (35.74)	2.63 (16.9)	1.34 (8.82)	0.68 (4.24)	0.4 (2.65)	0.3 (1.92)	0.28(1.88)	0.26(1.57)
320	9.67 (67.44)	4.95 (35.3)	2.59(17.52)	1.29 (8.86)	0.72 (4.35)	0.49(3.03)	0.4 (2.44)	0.37(2.34)
640	13.66 (93.06)	7.04 (45.2)	3.63(18.73)	1.84(12.97)	1.02 (6.51)	0.68(4.2)	0.58(3.69)	0.53 (3.5)
1000	31.18 (284.59)	16 (129.77)	7.58 (61.3)	3.98(33.04)	2.08 (16.82)	1.16(9.08)	0.83(5.42)	0.68(4.65)
2000	31.42 (273.39)	15.45(130.68)	8.07(67.13)	4.06(36.16)	2.29 (19.22)	1.38(9.87)	1.06(6.93)	1.0 (6.48)

Table 4. ENOB (Peak-to-Peak Noise) derived from Root Mean Square (RMS) noise

Conditions: AVDD = 5 V, AVSS = 0 V, Internal reference voltage = 2.048 V

Data transfer rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
5	21.5(19)	21.5(18.9)	21.5 (18.9)	21.5(19)	21.3(18.9)	21(18.6)	20.2(17.7)	19.2 (16.8)
10	21.1(18.5)	21.1(18.6)	21(18.4)	21(18.4)	20.9 (18.3)	20.5(18)	19.8 (17.3)	18.7 (16.3)
20	20.6 (18.1)	20.7(18.1)	20.6(18)	20.5 (17.9)	20.4 (17.8)	20.1(17.6)	19.2 (16.7)	18.3 (15.8)
40	20.6 (17.9)	20.5(18)	20.5 (17.9)	20.5 (17.9)	20.2 (17.8)	19.7 (17.2)	18.8 (16.3)	17.9 (15.4)
80	20.1(17.4)	20.1(17.5)	20.1 (17.5)	20 (17.5)	19.7 (17.2)	19.2(16.6)	18.3 (15.8)	17.5(15)
160	19.5 (16.8)	19.6(16.9)	19.5 (16.8)	19.5 (16.9)	19.3 (16.6)	18.7(16)	17.8 (15.1)	16.9 (14.3)
320	18.7 (15.9)	18.7(15.8)	18.6 (15.8)	18.6 (15.8)	18.4 (15.8)	18(15.4)	17.3 (14.7)	16.4 (13.7)
640	18.2 (15.4)	18.1(15.5)	18.1 (15.7)	18.1(15.3)	17.9 (15.3)	17.5 (14.9)	16.8(14.1)	15.9(13.2)
1000	17(13.8)	17(13.9)	17(14)	17(13.9)	16.9 (13.9)	16.8 (13.8)	16.2(13.5)	15.5(12.7)
2000	17(13.9)	17(13.9)	17(13.9)	16.9 (13.8)	16.8 (13.7)	16.5 (13.7)	15.9(13.2)	15(12.3)

Table 5. Noise levels, in μV RMS and (μV P).
Conditions: AVDD=3V, AVSS=0V, Internal reference voltage=2.048V

Data transfer rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
5	2.5 (14.24)	1.32 (6.92)	0.67 (3.48)	0.32 (1.68)	0.17 (0.9)	0.09 (0.51)	0.08 (0.42)	0.07 (0.39)
10	3.09 (16.85)	1.69 (9.32)	0.82 (4.68)	0.42 (2.41)	0.23 (1.18)	0.11 (0.63)	0.11 (0.66)	0.1 (0.55)
20	4.55 (24.74)	2.19 (12.82)	1.07 (5.94)	0.55 (3.38)	0.28 (1.66)	0.16 (1.0)	0.15 (0.92)	0.14 (0.87)
40	5.06 (34.59)	2.39 (14.49)	1.27 (7.75)	0.66 (4.01)	0.36 (2.18)	0.21(1.16)	0.21(1.27)	0.15 (0.84)
80	6.63 (43.46)	3.28 (20.22)	1.79 (10.64)	0.89 (5.48)	0.47 (2.95)	0.29 (1.63)	0.28 (1.64)	0.21 (1.24)
160	9.75 (68.28)	4.89 (32.19)	2.36 (17.74)	1.26 (9.87)	0.65 (4.77)	0.4(2.6)	0.4(2.7)	0.3(2.12)
320	19.22 (140.06)	9.8 (82.24)	4.81 (32.74)	2.47 (18.59)	1.27 (9.45)	0.71 (5.83)	0.5 (3.36)	0.43 (2.86)
640	27.07 (192.96)	13.54 (100.26)	6.88 (49.07)	3.4 (25.93)	1.76 (12.49)	1.02 (7.49)	0.71 (4.81)	0.6 (4.06)
1000	40.83 (388.28)	20.39 (185.96)	10.39 (89.38)	5.09 (43.28)	2.66 (22.78)	1.45 (11.01)	0.93 (6.74)	0.74 (4.86)
2000	42.06 (322.85)	21.15 (166.75)	10.66 (92.68)	5.61 (44.08)	2.92 (23.06)	1.68 (11.71)	1.19 (8.23)	1.05 (6.97)

Table 6. ENOB (Peak-to-Peak Noise) derived from Root Mean Square (RMS) noise
Conditions: AVDD=3V, AVSS=0V, Internal reference voltage=2.048V

Data transfer rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
5	20.6 (18.1)	20.6 (18.2)	20.5 (18.2)	20.6 (18.2)	20.5 (18.1)	20.4 (17.9)	19.6 (17.2)	18.8 (16.3)
10	20.3 (17.9)	20.2(17.7)	20.3 (17.7)	20.2(17.7)	20.1(17.7)	20.1(17.6)	19.1(16.6)	18.3 (15.8)
20	19.8 (17.3)	19.8 (17.3)	19.9 (17.4)	19.8 (17.2)	19.8 (17.2)	19.6(17)	18.7 (16.1)	17.8 (15.2)
40	19.6 (16.9)	19.7 (17.1)	19.6 (17.0)	19.6(17)	19.5 (16.8)	19.2 (16.8)	18.2 (15.6)	17.7 (15.2)
80	19.2 (16.5)	19.3 (16.6)	19.1(16.6)	19.1(16.5)	19(16.4)	18.7 (16.3)	17.8 (15.3)	17.2(14.7)
160	18.7 (15.9)	18.7(16)	18.7 (15.8)	18.6 (15.7)	18.6 (15.7)	18.3 (15.6)	17.3 (14.5)	16.7 (13.9)
320	17.7 (14.8)	17.7 (14.6)	17.7 (14.9)	17.7 (14.7)	17.6 (14.7)	17.5 (14.4)	17(14.2)	16.2(13.4)
640	17.2(14.4)	17.2(14.3)	17.2(14.3)	17.2(14.3)	17.1(14.3)	16.9 (14.1)	16.5 (13.7)	15.7 (12.9)
1000	16.6 (13.4)	16.6 (13.4)	16.6 (13.5)	16.6 (13.5)	16.6 (13.5)	16.4 (13.5)	16.1(13.2)	15.4(12.7)
2000	16.6 (13.6)	16.6 (13.6)	16.6 (13.4)	16.5 (13.5)	16.4 (13.4)	16.2(13.4)	15.7 (12.9)	14.9 (12.2)

Overview

The DADS1248 is a highly integrated 24-bit data converter. These devices include a low-noise, high-input-impedance programmable gain amplifier (PGA), a delta-sigma (ΔΣ) type ADC with a single-cycle setup digital filter, an internal oscillator, and an SPI-compatible serial interface. The DADS1248 also includes a flexible input multiplexer with system monitoring capabilities and general-purpose I/O settings, an extremely low-drift reference voltage source, and two matched current sources for sensor excitation.

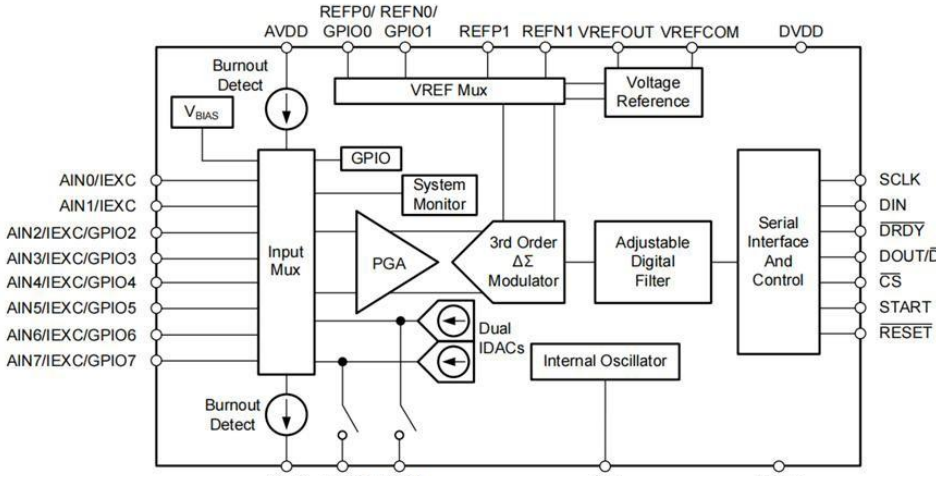


Figure 5: Functional Block Diagram

Function Description

ADC Input Multiplexer

The ADC measures the input signal via an on-chip PGA. All analog inputs are connected to the internal ANINP or ANINN analog inputs via an analog multiplexer. The input multiplexer connects to eight analog inputs. Any analog input pin can be selected as a positive or negative input via the MUX0 register. The multiplexer also allows selection of the on-chip excitation current and bias voltage for specific channels. The input multiplexer allows selection of ambient temperature (internal temperature sensor), AVDD, DVDD, and external reference voltage for measurement. See the system monitor for more details.

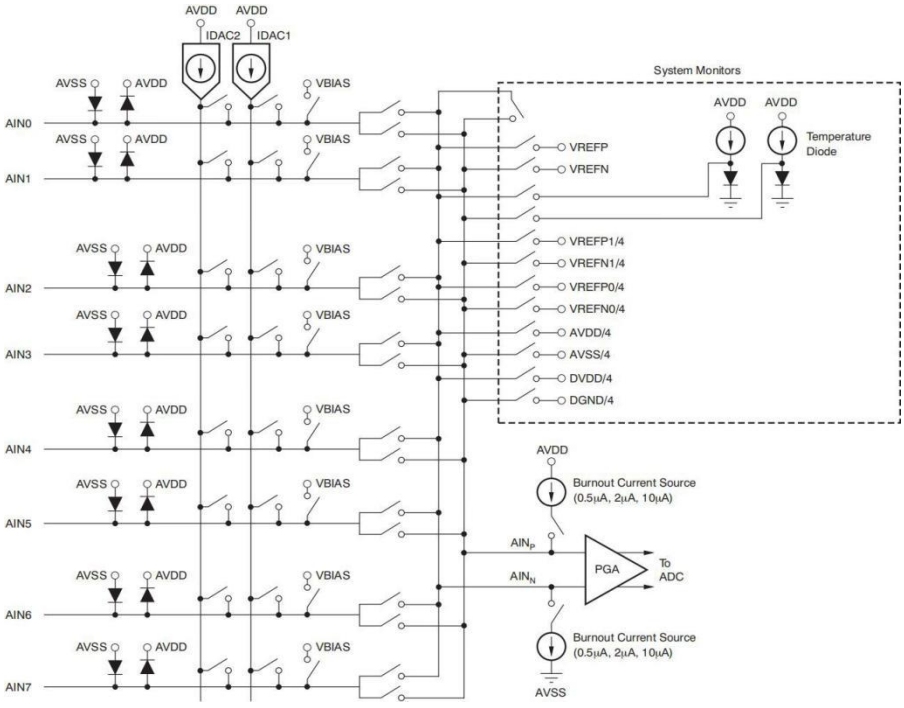


Figure 6. Schematic diagram of input multiplexer

Low-Noise Programmable Gain Amplifier

The DADS1248 features a low-drift, low-noise, high-input-impedance programmable gain amplifier (PGA). The SYS 0 register allows setting the PGA gain to 1, 2, 4, 8, 16, 32, 64, or 128. Figure 7 shows a simplified diagram of the PGA.

The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistive feedback network used to set the PGA gain. The PGA input is equipped with an electromagnetic interference (EMI) filter, as shown in Figure 7. Note that, as with any PGA, ensure the input voltage remains within the specified common-mode input range. The common-mode voltage is calculated using the following equation:

(AVSS+0.1V+(VINMAX × Gain)/2) ≤ VCM ≤ (AVSS-0.1V-(VINMAX×Gain)/2)

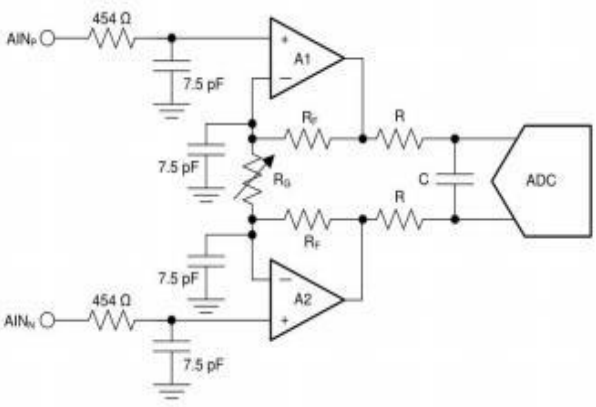


Figure 7.Simplified diagram of PGA

The gain inside the device is changed using a variable resistor RG. The differential full-scale input voltage range (FSR) of the PGA is determined by the gain setting and the reference voltage used, as shown in the following formula: FSR = ±VREF / Gain. Table 7 shows the corresponding full-scale input range when using the internal 2.048 reference voltage source.

Table7. PGA Full scale range

PGA GAIN SETTING	FSR
1	±2.048V
2	±1.024V
4	±0.512V
8	±0.256V
16	±0.128V
32	±0.064V
64	±0.032V
128	±0.016V

PGA Common-Mode Voltage Requirements

To maintain the PGA's linear operating range, the input signal must meet certain requirements discussed in this section. The output swings of the two amplifiers (A1 and A2) in Figure 8 cannot be closer to the power supply (AVSS and AVDD) than 100mV. If the outputs OUTP and OUTN are driven to within 100mV of the power supply rails, the amplifier will saturate and become nonlinear. To prevent this nonlinear operating condition, the output voltage must satisfy the following equation:

AVSS+0.1V ≤ V(OUTN),V(OUTP)≤ AVDD-0.1

It is beneficial to translate the requirements of the above equations into requirements referred to the PGA inputs (AINP and AINN) because the PGA outputs cannot be directly accessed. The PGA employs a symmetrical design; therefore, it can be assumed that the common-mode voltage at the PGA output is the same as the common-mode voltage of the input signal, as shown in Figure 8.

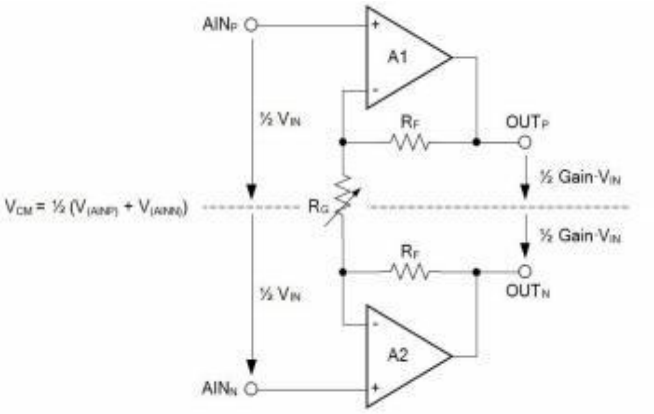


Figure 8. PGA Common Mode Voltage

The common-mode voltage is calculated using equation 6:

VCM = ½ (V(AINP)+V(AINN)) = ½ (V(OUTP)+V(OUTN)) (6)

The voltage at the PGA input terminals (AINP and AINN) can be obtained from the equation 7 and equation 8:

V(AINP) = VCM + ½ VIN (7)

V(AINN) = VCM - ½ VIN (8)

Output voltage (V(OUTP) and V(OUTN)) can be obtained through the equation9 and equation10:

V (OUTP) = VCM + ½ Gain · VIN (9)

V (OUTN) = VCM - ½ Gain · VIN (10)

Now, the output voltages of amplifiers A1 and A2 (as per equation 5) can be converted into the requirements for the input common-mode voltage range through equations 9 and 10, as shown in formulas 11 and 12.

VCM (MIN) ≥ AVSS+0. 1V+ ½ Gain · VIN (MAX) (11)

VCM (MAX) ≤ AVDD – 0.1V– ½ Gain · VIN (MAX)

(12)

To calculate the minimum and maximum common-mode voltage limits , the maximum differential input voltage (VIN (MAX)) that occurs in the application must be used. VIN(MAX) can be less than the maximum possible full-scale value.

PGA Common Mode Voltage Calculation Example

The following paragraphs explain how to apply Equations 11 and 12 to the assumed application. In this example, AVDD=3.3V and AVSS=0V are set. With a gain of 16 and an external reference voltage VREF=2.5V, the maximum possible differential input voltage that can be applied is VIN =(V(AINP)–V(AINN)), which is then limited to FSR=2.5V/16=0. Within the full-scale range of 156V, Equations 11 and 12 yield an allowable VCM range of 1.35V ≤VCM≤1.95V.

For example, in such an application, the sensor signal connected to the input does not utilize the entire full-scale range, but is limited to VIN(MAX)=0.1V Then this reduced input signal amplitude will VCM restrictions relaxed to 0.9V≤VCM≤2.4V.

In the case of fully differential sensor signals, the inputs (AINP, AINN) can swing up to 50 mV around the common mode voltage (V(AINP) + V(AINN))/2 , which must be kept between 0.9V and 2.4V. The output of a symmetrical Wheatstone bridge is an example of a fully differential signal. Figure 9 shows the case where the common mode voltage of the input signal is at its minimum limit. In this case, V(OUTN) is exactly 0.1V. Any further decrease in the common mode voltage (VCM) or an increase in the differential input voltage (VIN) will drive V(OUTN) below 0.1V and cause the amplifier to A2 saturation.

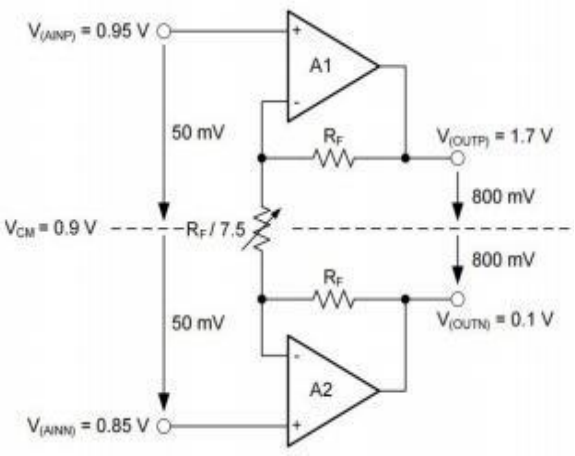


Figure 9. VCM Example at the minimum limit

In contrast, the RTD signal is pseudo-differential in nature, with the negative input maintained at a constant voltage above 0V, and only the voltage at the positive input changing. When it is necessary to measure a pseudo-differential signal, in this example, the negative input must be biased within a voltage range of 0.85V to 2.35V, and the positive input swing can reach up to VIN(MAX)=100 mV above the negative input. In this case, the voltage at the positive input terminal changes along with the common mode voltage. That is, when the input signal fluctuates between 0V≤VIN≤VIN (maximum value) , the common mode voltage fluctuates between V(AINN)≤ VCM≤ V(AINN)+VIN(maximum value). Meeting the common mode voltage requirement of the maximum input voltage VIN (MAX) ensures that the requirement is met across the entire signal range.

Figures 10 and 11 show examples of fully differential and pseudo-differential signals, respectively.

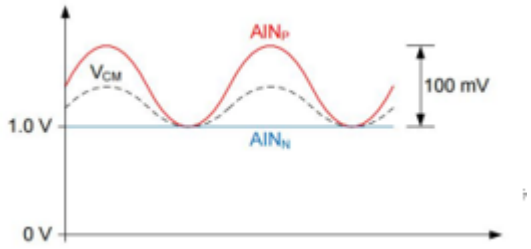


Figure 10. Fully differential input signal

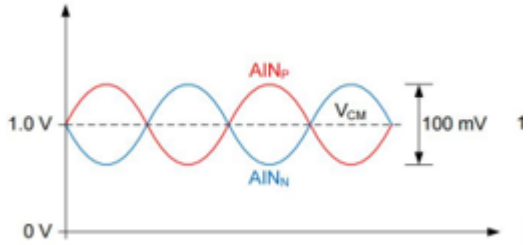


Figure 11. Pseudo -differential input signal

Notice: When using a unipolar power supply, the input range does not extend to ground. Equations 11 and 12 show the common mode voltage requirements.

$$VCM\ (MIN) \geq AVSS + 0.1V + \tfrac{1}{2}\ Gain \cdot VIN\ (MAX)$$

$$VCM\ (MAX) \leq AVDD - 0.1V - \tfrac{1}{2}\ Gain \cdot VIN\ (MAX)$$

Analog Input Impedance

The device input is buffered by a high-input-impedance PGA before reaching the Δ-Σ modulator. For most applications, the input current is small and negligible. However, due to the chopping function of the PGA, the input impedance can be described as a small absolute input current. The absolute input current of the selected channel is approximately proportional to the clock speed of the selected modulator. Table 8 shows typical values for these currents at different voltage coefficients and the corresponding input impedances at different data rates.

Condition	Absolute input current	Effective input impedance
DR=5SPS, 10SPS, 20SPS	±(0.5nA+0. 1nA/V)	5000 MΩ
DR=40SPS, 80SPS 160SPS	±(2nA+0.5nA/V)	1200 MΩ
DR=320SPS, 640SPS 1kSPS	±(4nA+1nA/V)	600 MΩ
DR=2kSPS	±(8nA+2nA/V)	300 MΩ

Table 8. Typical values of analog input current at data rates
VCM = 2.5 V The input current at TA = 25°C AVDD = 5 V AVSS = 0 V

Clock Source

This device can use either an internal oscillator or an external clock. Connect the CLK pin to DGND before powering on or resetting to activate the internal oscillator. Connecting an external clock to the CLK pin disables the internal oscillator at any time, and the device then operates on the external clock. Once the device has switched to an external clock, it cannot switch back to the internal oscillator unless the device is powered on or reset.

Modulator

The DADS1248 device uses a third-order Δ-Σ modulator. The modulator converts the analog input voltage into a pulse code modulation (PDM) data stream. To save power, the modulator clock operates in the range of 32kHz to 512kHz, supporting different data rates, as shown in Table 9.

Table 9. Modulator clock frequencies at different data rates

DATA RATE (SPS)	MODULATOR RATE(f MOD) (1) (kHz)	fCLK/fMOD
5, 10, 20	32	128
40, 80, 160	128	32
320, 640, 1000	256	16
2000	512	8

Use an internal oscillator or an external 4.096 MHz clock.

Digital Filters

This ADC uses a linear-phase finite-impulse-response (FIR) digital filter, which can be adjusted for different output data rates. The digital filter is always built up within a single cycle.

Table 10 shows the precise data rate when using an external clock of 4.096MHz. The figure also shows the signal -3dB bandwidth and 50Hz and 60Hz attenuation. For good 50Hz or 60Hz rejection performance, use a data rate of 20SPS or lower. The frequency response of the digital filter is shown in Figures 12 to 22. Figure 20 shows in detail the filter frequency response in the range of 48Hz to 62Hz at a data rate of 20SPS. All filter curves were generated by an external clock of 4.096MHz.

The data rate and digital filter frequency response are proportional to changes in the system clock frequency. Changes in the internal oscillator frequency, as described in the electrical characteristics section, also affect the data rate and digital filter frequency response.

Table 10. Digital Filter Specifications (1)

Nominal data rate	Actual data rate	-3 dB bandwidth	Attenuation			
			fIN = 50Hz ± 0.3Hz	fIN = 60Hz ± 0.3Hz	fIN = 50Hz ± 1Hz	fIN = 60Hz ± 1Hz
5SPS	5.018 SPS	2.26Hz	-106dB	-74dB	-81dB	-69dB
10SPS	10.037 SPS	4.76Hz	-106dB	-74dB	-80dB	-69dB
20SPS	20.075 SPS	14.8Hz	-71dB	-74dB	-66dB	-68dB
40SPS	40.15SPS	9.03Hz	—	—	—	—
80SPS	80.301 SPS	19.8Hz	—	—	—	—
160SPS	160.6 SPS	118Hz	—	—	—	—
320SPS	321.608 SPS	154Hz	—	—	—	—
640SPS	643.21 SPS	495Hz	—	—	—	—
1000SPS	1000SPS	732Hz	—	—	—	—
2000SPS	2000SPS	1465Hz	—	—	—	—

The value displayed when fCLK = 4.096 MHz.

Reference Voltage Input

The reference voltage for this device is the differential voltage between REFP and REFN, given by Equation 13:

VREF = V(REFP) –V(REFN) (13)

There is a multiplexer for selecting the reference input, as shown in Figure 23. The reference input uses a buffer to increase the input impedance. Similar to the analog inputs, REFP0 and REFN0 can be configured as digital I/O on the DADS1248.

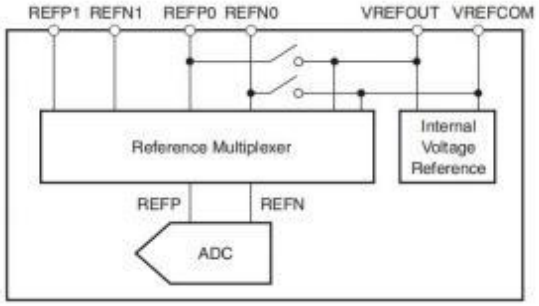


Figure 23. Reference Input Multiplexer

The reference input circuit has an ESD diode to protect the input. To prevent the diode from conducting, ensure that the voltage on the reference input pin is not lower than AVSS - 100mV and does not exceed AVDD + 100mV, as shown in Equation 14.

AVSS–100mV<(V(REFP) or V(REFN))<AVDD+100mV (14)

Internal Reference Voltage

The DADS1248 features an internal reference voltage source with a low temperature coefficient. The reference voltage source outputs 2.048V (nominal value) and can provide a maximum source and sink current of 10mA. A capacitor must be connected between VREFOUT and VREFCOM. The capacitor value must be in the range of 1uF to 47uF. A larger value provides more noise filtering; however, the turn-on time increases with increasing capacitance, as shown in Table 11. For stability, VREFCOM must have an AC ground node path with an impedance less than 10Ω, such as GND (0V to 5V analog power) or AVSS (2.5V analog power). If this impedance is greater than 10Ω, a capacitor of at least 0.1uF should be connected between VREFCOM and the AC ground node (e.g., GND).

Notice:

Because it takes time for the reference voltage source to build up to the final voltage, be careful when shutting down the device between conversions. Allow sufficient time for the internal reference voltage to fully build up before starting a new conversion.

VREFOUT CAPACITOR	SETTLING ERROR	TIME TO REACH THE SETTING ERROR
1uF	±0.5%	70us
	±0.1%	110us
4.7uF	±0.5%	290us
	±0.1%	375us
4.7uF	±0.5%	2.2ms
	±0.1%	2.4ms

Table 11: Internal reference voltage settling time

The internal reference voltage is controlled by the MUX 1 register; by default, the internal reference voltage source is off upon power-up (see the detailed register definitions for DADS1248 for details). Therefore, the internal reference voltage must be enabled first, and then connected via the internal reference voltage multiplexer. Since the internal reference voltage source is used to generate the reference current for the excitation current source, it must be enabled before the excitation current is available.

Excitation Current Source

The DADS1248 provides two matched excitation current sources (IDACs) for RTD applications. For three-wire RTD applications, the matched current sources can be used to eliminate errors caused by sensor lead resistance. The output current of the IDACs can be programmed to be 50μA, 100μA, 250μA, 500μA, 750μA, 1000μA, or 1500μA.

Two matched current sources can be connected to dedicated current output pins IEXC1 and IEXC2, or to any analog input pin; see the DADS1248 detailed registry definition for more information. Two current sources can also be connected to the same pin. When using the excitation current source, the internal reference voltage source must be enabled, and an appropriate capacitance must be applied to VREFOUT.

Sensor Detection

To aid in the detection of potential sensor malfunctions, the device provides selectable current sources (0.5μA, 2μA, or 10μA) as burn-off current sources. When enabled, one current source supplies current to the selected positive analog input (AINP), while the other current source draws current from the selected negative analog input (AINN).

If the sensor is open-circuited, these burn-out current sources
will pull the positive input to AVDD and the negative input
to AVSS, resulting in a full-scale reading. A full-scale reading
may also indicate sensor overload or a missing reference
voltage. A reading close to zero may indicate a sensor short
circuit. The absolute value of the burn-out current source typically varies by 10%, and the internal multiplexer adds a small series resistance. Therefore, distinguishing between a short-circuit sensor condition and a normal reading can be difficult, especially when using an RC filter at the input. In other words, even if the sensor is short-circuited, the voltage drop across the external filter resistor and the remaining resistance of the multiplexer will cause the output reading to be greater than zero.

When a fusible current source is enabled, the ADC readings of the functional sensor may be corrupted. It is recommended to disable fusible current sources when performing precision measurements and to enable them only to test for sensor failure conditions.

Bias Voltage Generation

An optional bias voltage is provided for unbiased thermocouples. The bias voltage is (AVDD + AVSS)/2 and can be applied to any analog input channel via the internal input multiplexer. Table 12 lists the bias voltage turn-on time for different sensor capacitances.

Selecting internal bias voltage generators on multiple channels can cause internal short circuits within those channels. Therefore, it is important to limit the current flowing through the device. We recommend that under no circumstances should a current exceeding 5mA be allowed through this path.

Table 12. Bias voltage settling time

Sensor Capacitor	Establishment Time
0.1uF	220us
1uF	2.2ms
10uF	22ms
200uF	450ms

General Purpose Digital I/O

The DADS1248 has eight pins that can be used as analog inputs or general-purpose digital inputs and outputs (GPIOs). Three registers control the function of the GPIO pins. The GPIO Configuration Register (IOCFG) enables a pin as a GPIO pin. The GPIO Direction Register (IODIR) configures a GPIO pin as either an input or an output. Finally, the GPIO Data Register (IODAT) contains the GPIO data. If a GPIO pin is configured as an input, the corresponding IODAT[x] bit reads the pin's status; if a GPIO pin is configured as an output, the output status is written to the corresponding IODAT[x] bit. For more information on GPIO pin usage, see the DADS1248 detailed register definition section.

Figure 24 illustrates how these functions can be combined
onto a single pin. Note that when the pin is configured as a
GPIO, the corresponding logic is powered by AVDD and AVSS. When the DADS1248 is powered by a bipolar analog supply,
the GPIO outputs a bipolar voltage. When used as an output, care must be taken when loading the GPIO pin, as large currents can cause the analog supply voltage to drop or introduce noise.

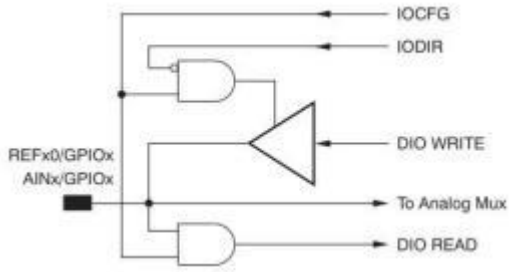


Figure 24. Analog and data interface pins

System Monitor

The DADS1248 provides system monitoring functionality.
This functionality can measure analog power supplies, digital power supplies, external reference voltage sources, or ambient temperature. Note that the system monitoring function only provides a rough estimate. Analog inputs are disconnected
when the system monitor is enabled.

Power monitor

The system monitor can measure analog or digital power supplies. When measuring the power supply (VSP), the conversion result is approximately one-quarter of the

actual power supply voltage, as shown in Equation 15.

Conversion Result=(VSP/4)/VREF (15)

External Reference Voltage Monitor

An ADC can measure an external reference voltage. In this configuration, a monitored external reference voltage source (VREX) is connected to the analog input. The result (converted code) is approximately one-quarter of the actual reference voltage, as shown in Equation 16.

Conversion Result=(VREX/4)/VREF (16)

Note: When using the system monitor to measure external reference voltage, the internal reference voltage must be enabled.

Ambient Temperature Monitor

On-chip diodes provide temperature sensing capability. When the temperature monitoring function is selected, the anodes of the two diodes are connected to the ADC. Typically, at TA=25°C, the diode voltage difference is 118mV, and the temperature coefficient is 405uv/°C.

Device Functional Mode

Power On

When the DVDD is powered on, the internal power-on reset module generates a pulse, resetting all digital circuits. All digital circuits remain in the reset state within 216 system clocks to allow the analog circuit and the internal digital power supply to establish. After the internal reset is released, SPI communication will occur.

Reset

When the RESET pin goes low, the device immediately resets. All registers return to their default values. As long as the reset pin remains low, the device will remain in the reset mode. When the RESET pin goes high, the ADC exits the reset mode and is able to convert data. After the RESET pin goes high, when the system clock frequency is 4.096 MHz, when fCLK = 4.096 MHz, the digital filter and registers remain in the reset state for 0.6 ms. Therefore, only after the RESET pin goes high for 0.6 ms can effective SPI communication be restored; see Figure 4. When the RESET pin goes low, the clock is reset to the internal oscillator. The reset can also be performed through the serial interface by the reset command, which has the same function as using the RESET pin. For information on using the RESET command, please refer to RESET (0000 011X).

Power Saving Mode

By placing the device in power-saving mode, the power consumption is minimized. There are three methods to enable the device to enter the power-saving mode: using the SLEEP command, pulling the START pin low, and when the START/SYNC command controls the conversion mode and the CM of register SYS0 is 0, enter the power-saving mode after each conversion. In the power-off mode, the state of the internal reference voltage depends on the setting of the VREFCON bit in the MUX1 register; for details, refer to the register mapping.

Start Pin Control

The START pin provides precise control over the conversion. By pulling up the START pin to a high level, the conversion begins, as shown in Figure 25 and Table 13. When the DRDY mode bit in the IDAC0 register is set to 1, the DRDY pin goes low, and the DOUT/DRDY pin indicates that the conversion is complete. After the conversion is completed, the device automatically turns off. During power-down, the conversion results can be retrieved; however, before communicating with the configuration register, the START pin must be pulled up. The device remains in the off state until the START pin returns to a high level, initiating a new conversion. When the START pin returns to a high level, the sampling filter remains in the reset state within 32 modulator clock cycles to allow the analog circuit to establish.

Keeping the START pin at a high level will configure the device for continuous conversion, as shown in Figure 26.

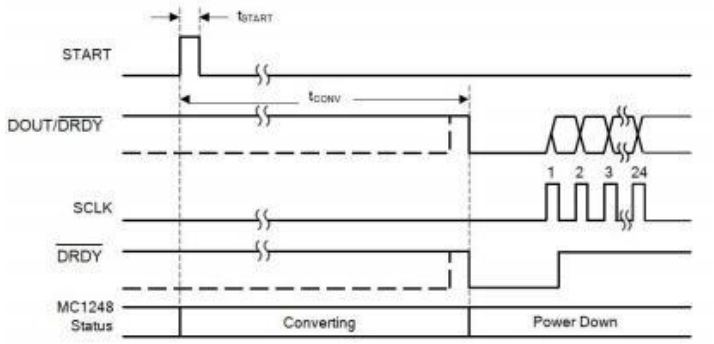


Figure 25. Use Start Pin single-transition timing

Table 13. Figure 25 Start pin switching time

Symbol	Description	Data rate (SPS)	Value	Unit
tCONV	Time from the START rising edge to DRDY and DOUT/DRDY going low	5	200.295	ms
		10	100.644	ms
		20	50.825	ms
		40	25.169	ms
		80	12.716	ms
		160	6.489	ms
		320	3.247	ms
		640	1.692	ms
		1000	1.138	ms
		2000	0.575	ms

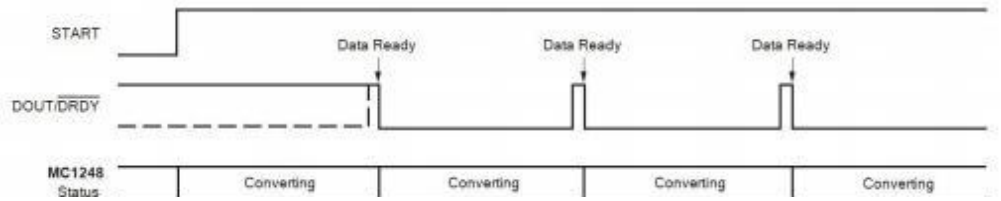


Figure 26. Start Conversion timing when pin is high

Note: SCLK remains low in this example

When the START pin is held high, the ADC continuously converts the selected input channel. This configuration continues until the START pin is pulled low. The START pin can also be used to perform synchronous measurements in multi-channel applications by applying a pulse. For multiple devices, if each device receives a pulse to the START pin simultaneously, all devices will begin conversion when the START pin rises. If all devices are operating at the same data rate, all devices will complete conversion simultaneously.

Command Control

When the START pin is low, the ADC conversion can be controlled by sending a START/SYNC command to the device. When the device receives the START/SYNC command, it determines which conversion mode to enter based on the state of the CM bit in the SYS0 register. In single-conversion mode, as shown in Figure 27, the device completes one conversion each time it receives a START/SYNC command, and then enters power-saving mode. In continuous conversion mode, the device performs conversions continuously. After a conversion is completed, the device places the result into the output buffer and immediately begins another conversion. To initiate continuous conversion mode, the CM bit must be set to 1, followed by the START/SYNC command, as detailed in Figure 28.

To exit the START/SYNC command control switching mode, simply send a stop command to the device once, as shown in the figure 29.

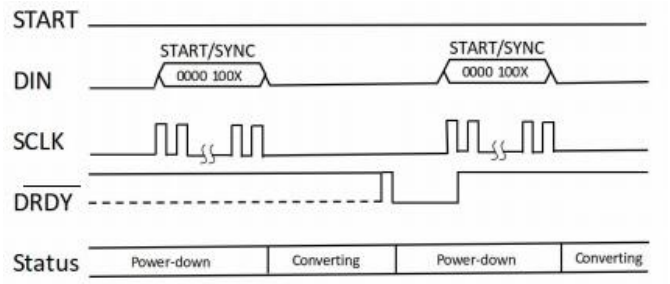


Figure 27. The single conversion timing sequence using the START/SYNC command

Note : CM=0, single conversion

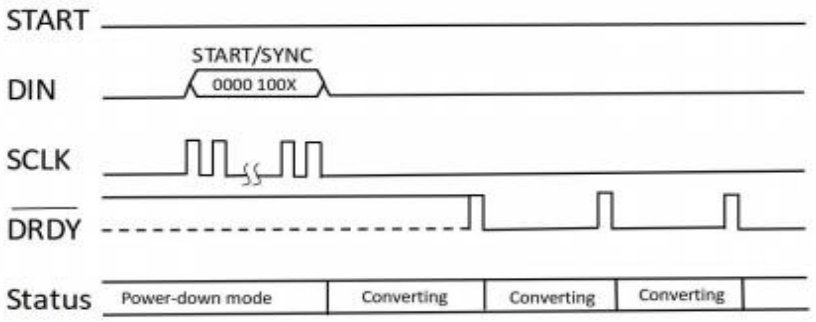


Figure 28. The timing sequence for continuous conversion using the START/SYNC command

Note : CM = 1, continuous conversion

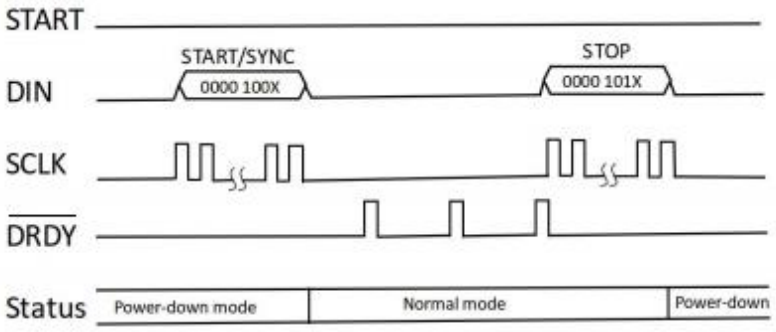


Figure29. Exit START/SYNC Command Control Mode

Conversions can also be initiated via SPI commands. Similar to using the START pin, the SLEEP command can be used to put the device into power-saving mode. Functionally, this is similar to pulling the START pin low or using the START/SYNC command to control entry into single-conversion mode. To initiate a conversion, the WAKEUP command wakes the ADC and starts the conversion, similar to returning the START pin high or sending the START/SYNC command again. Note that sleep and wake-up commands can only be used to control conversions when the device is in continuous conversion mode. Do not use the START pin and commands simultaneously to control conversions. Furthermore, sending the SYNC or START/SYNC command immediately initiates a new ADC conversion. The digital filter then resets, and a new conversion begins without completing the previous one. This is useful for synchronizing conversions of multiple devices or maintaining periodic timing across multiple channels. Similarly, writing to the first four registers (MUX0, VBIAS, MUX1, or SYS0 addresses 00h to 04h) automatically resets the digital filter. A change in any of these registers will cause a corresponding setting change in the device, but will also restart the conversion, just like the SYNC command.

The Setup Time for Channel Multiplexing

This device is a true single-cycle setup ΔΣ converter. Once the input signal has been set to the final result, the first batch of usable data after the conversion begins is fully set and available for use. The setup time is approximately equal to the reciprocal of the data rate. The exact time depends on the specific data rate and the operation that triggers the conversion; specific values are shown in Table 14.

Channel Loop and Overload Recovery

When cycling between channels, pay attention to the device configuration to ensure setup within one cycle. For settings that cycle between multiplexer channels without changing the PGA and data rate settings, changing the MUX 0 register is sufficient. However, when changing the PGA and data rate settings, ensure that no overload occurs during transmission. When configuration register data is transmitted to the device, the new setting takes effect at the end of each transmitted register byte. Therefore, a brief overload may occur during configuration data transmission after the MUX 0 byte has completed and before the SYS 0 byte has completed. This temporary overload can cause intermittent incorrect readings. To ensure no overload occurs, it may be necessary to split the communication into two separate communications so that the SYS 0 register is changed before changing the MUX 0 register . In overload conditions, ensure that a single cycle proceeds to the next cycle. Because the device uses a chopper-stabilized PGA, changing the data rate in overload conditions can cause chopper instability. This instability results in slow setup time. To prevent this slow setup, always change the PGA or multiplexer settings to a non-overload state before changing the data rate.

Single Loop Setting

The DADS1248 is capable of single-cycle setup at all gains and data rates. However, to achieve a 2kSPS single-cycle setup time, special care must be taken when using WREG to modify the configuration register interface. When operating at 2kSPS, the SCLK cycle must not exceed 520ns, and the time between the start of writing a register byte and the start of writing subsequent register bytes must not exceed 4.2us. Furthermore, when executing multiple separate write commands to the first four registers, at least 64 system clock cycles must be waited before initiating another write command.

Digital Filter Reset Operation

In addition to the RESET command and the RESET pin, the digital filter will automatically reset when a write operation is performed on the MUX0, VBIAS, MUX1 or SYS0 register, a SYNC or START/SYNC command is issued, or the START pin goes high.

The filter is reset four system clock cycles (tCLK) after the falling edge of the seventh SCLK following the SYNC or START/SYNC command. Similarly, if any write operation occurs in the MUX 0 register, the filter will be reset after the MUX 0 write operation is complete , regardless of whether the register value changes.

If any write operation occurs in the VBIAS, MUX1, or SYS0 registers , the filter will reset regardless of whether the register value changes. After a write operation completes, the reset pulse lasts for 32 modulator clock cycles. If there are multiple write operations, the resulting reset pulse can be considered as the AND result of different active-low pulses generated individually for each operation.

Table 14 shows the transition times after a filter reset. Note that these times depend on the operation that initiated the reset. Furthermore, the first transition after a filter reset takes slightly different times than the second and subsequent transitions.

Table 14. Data conversion time

Nominal data rate(SPS)	Accurate data rate(SPS)	First Data Conversion Time After Filter Reset				Reset the conversion time filter for the second time and subsequent times	
		Synchronization command, MUX0 Register write		Hardware reset, reset command, start pin at high level, wake-up command, write VBIAS, MUX1 or SYS0 register			
		(ms) (1)	System clock cycle count	(ms) (1)	System clock cycle count	(ms) (1)	System clock cycle count
5	5.019	199.258	816160	200.26	820265	199.250	816128
10	10.038	99.633	408096	100.635	412201	99.625	408064
20	20.075	49.820	204064	50.822	208169	49.812	204032
40	40.151	24.92	102072	25.172	103106	24.906	102016
80	80.301	12.467	51064	12.719	52098	12.453	51008
160	160.602	6.240	25560	6.492	26594	6.226	25504
320	321.608	3.124	12796	3.25	13314	3.109	12736
640	643.216	1.569	6428	1.695	6946	1.554	6368
1000	1000	1.014	4156	1.141	4674	1	4096
2000	2000	0.514	2108	0.578	2370	0.5	2048

(1) fCLK = 4.096 MHz.

Calibration

The converted data is scaled by offset and gain registers to produce the final output code. As shown in Figure 30, the output of the digital filter is first subtracted from the offset register (OFC) and then multiplied by the full-scale register (FSC) to digitally adjust the gain. A digital limiting circuit ensures that the output code does not exceed 24 bits. Equation 17 shows the scaling ratio.

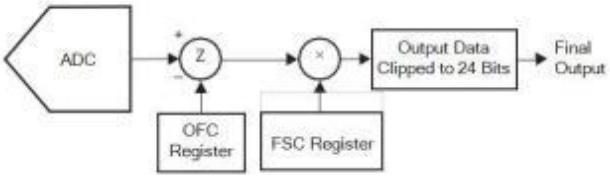


Figure 30. Calibration block diagram

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \text{FSC}[2:0] \quad (17)$$

The values of the offset and full-scale registers can be set directly by writing to them or automatically via calibration commands . Offset and gain calibration features are designed to correct for small system-level offset and gain errors. When manually entering values into the calibration registers, care must be taken to avoid reducing the gain register to values far below the scaling factor of 1.0. In extreme cases, the ADC may over-scale. Avoid connecting analog inputs to voltages greater than VREF/gain. Exercise caution when using FSC to increase digital gain. No special care is needed when achieving a custom digital gain less than 20% above the nominal value and with offset less than 40% of full scale. When the digital gain is more than 20% above the nominal value and offset is greater than 40% of full scale, ensure the offset and gain registers meet the conditions of Equation 18.

$$2\text{V}/\text{Gain Scaling} - 1.125\text{V} > |\text{Offset Scaling}| \quad (18)$$

Offset Calibration Register: OFC[2:0]

The offset calibration register is a 24-bit word consisting of three 8-bit registers. The offset is in two's complement format, with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. This value is subtracted from the converted data. The register value 000000h does not provide offset correction. Note that although the offset calibration register value can correct offsets in the range of –FS to +FS (as shown in Table 15), analog input overload should be avoided.

Table 15. Relationship between the final output code and the offset calibration register settings

Offset Register	Final Output CodeVIN = 0 (1)
7FFFFFh	800000h
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000001h
800000h	7FFFFFh

(1) Eliminate the influence of noise and inherent misalignment error .

Full-scale calibration register: FSC[2:0]

The full-scale or gain calibration register is a 24-bit word composed of three 8-bit registers. The full-scale calibration value is a 24-bit direct binary value, normalized to 1.0 at code 400000h. Table 16 summarizes the scaling of the full-scale register. Note that while the full-scale calibration register can correct for gain errors greater than 1 (gain adjustment less than 1), ensure that analog input overload is avoided. The default or reset value of the FSC depends on the PGA gain setting. A different factory-adjusted FSC reset value is stored for

each PGA gain setting, thus providing gain accuracy across all device inputs .

Note that the factory-adjusted FSC reset value is automatically loaded whenever the PGA gain setting is changed.

Table 16. Relationship between gain correction factor and full-scale calibration register setting

Full-Scale Register	Gain Scale
400000h	2.0
200000h	1.0
100000h	0.5
000000h	0

Calibration Command

This device provides three types of calibration commands: system gain calibration, system offset calibration, and self-offset calibration. For absolute accuracy, we recommend performing calibration after power-on, temperature changes, gain changes, and, in some cases, channel changes. The DRDY signal goes low upon completion of calibration. The first data after calibration is always valid. Issuing commands during calibration after it has begun will result in data corruption. If this occurs, either resend the aborted calibration command or issue a device reset command.

System Offset and Self-Offset Calibration

System offset calibration corrects for both internal and external offset errors. System offset calibration is initiated by sending the SYSOCAL command, simultaneously applying a zero-differential input (VIN=0) to the selected analog input, while the input is within its common-mode range, ideally the intermediate supply voltage. Self-offset calibration is initiated by sending the self-focus command. During self-offset calibration, the selected input is disconnected from internal circuitry, a zero-differential signal is applied internally, and the input is connected to the intermediate supply. The offset calibration register (OFC) is updated after both offset calibrations. When either offset calibration command is issued, the device stops the current conversion and immediately begins the calibration procedure. Offset calibration should be performed before gain calibration.

System Gain Calibration

System gain calibration corrects for gain errors in the signal path. System gain calibration is initiated by sending the SYSGCAL command when a full-scale input is applied to a selected analog input. The Full-Scale Calibration Register (FSC) is then updated. When the system gain calibration command is issued, the device stops the current conversion and immediately begins the calibration procedure.

Calibration Time

When calibration is initiated, the device performs 16 consecutive data conversions and averages the results to calculate the calibration value. This provides a more accurate calibration value. The calibration time is shown in Table17 and can be calculated using equation19:

Calibration Time = tCAL + 50/fCLK + 32/fMOD + 16/fDATA (19) where fDATA is the data rate

Table 17. Relationship between calibration time and data rate

Data rate (SPS)	Calibration time (tCAL) (ms)
5	3201.01
10	1601.01
20	801.012
40	400.26
80	200.26
160	100.14
320	50.14

Programming : Serial Interface

This device provides an SPI-compatible serial communication interface and a data ready signal (DRDY). Communication is full-duplex, except for some limitations of the RREG and RDATA commands. These limitations are explained in detail in the commands. For the basic serial interface timing characteristics, please refer to Figures 1 and 2 of this document.

Film Selection (CS)

The CS pin activates SPI communication. CS must be low before data transmission and must remain low throughout the entire SPI communication cycle. When CS is high, the DOUT/DRDY pin enters a high-impedance state. Therefore, serial interface read/write operations are ignored, and the serial interface is reset. The DRDY pin operates independently of CS. Even if CS is high, DRDY will still indicate that a new transition has been completed and will be forcibly pulled high in response to SCLK.

Pulling CS high only disables SPI communication with the device. Data conversion continues, and the DRDY signal can be monitored to check if a new conversion result is ready. The master monitoring the DRDY signal can select the appropriate slave by pulling the CS pin low.

Serial clock (SCLK)

SCLK provides the clock for serial communication. SCLK is a Schmitt trigger input, but we recommend keeping it as free from noise as possible to prevent glitches from unintentionally shifting data. Data is shifted into DIN on the falling edge of SCLK and out dout on the rising edge of SCLK.

Data Input (DIN)

DIN, along with SCLK, is used to send data to the device. Data on DIN is shifted into the device on the falling edge of SCLK.

The device's communication is essentially full-duplex. Even as data is being shifted out, the device monitors the commands being shifted in. When a command is sent, data is shifted out of the output shift register. Therefore, it is crucial to ensure that any signals sent to the DIN pin are valid when shifting out data. When no command is sent to the device while reading data, a NOP command is sent to DIN.

Data Ready (DRDY)

When the DRDY pin goes low, it indicates that a new conversion is complete, and the conversion result is stored in the conversion result buffer. After the DRDY goes low, SCLK must remain low for tDTS (see Figure 2) to load the conversion result into the result buffer and the output shift register. Therefore, if the conversion result needs to be read later, no commands should be issued during this period. This restriction only applies when CS is set and the device is in RDATAC mode. When CS is not set, SPI communication with other devices on the SPI bus does not affect the loading of the conversion result. After the DRDY pin goes low, it is forced to go high on the first falling edge of SCLK (so that the DRDY pin can poll 0 instead of waiting for the falling edge). If the DRDY pin does not go high after the SCLKs clock cycle after going low, a short high-level pulse lasting tPWH indicates that new data is ready.

Data Output and Data Readiness (DOUT/DRDY)

The OUT/DRDY pin has two modes: Data Output Only (DOUT) or DOUT Combined with Data Ready (DRDY). The DRDY mode bit determines the function of this pin and can be found in the IDAC0 register of the DADS1248. In either mode, the DOUT/DRDY pin enters a high-impedance state when CS goes high.

When the DRDY mode bit is set to 0, this pin is used only for DOUT. Data is output sequentially on the rising edge of SCLK, with MSB priority (as shown in Figure 31).

When the DRDY mode is set to 1, this pin is used for both DOUT and DRDY. Like DOUT, data is shifted out, but this pin adds DRDY functionality. Note that this mode is unavailable if the device is in stop-read continuous data mode when the SDATAC command is issued. The DRDY mode bit only modifies the functionality of the DOUT/DRDY pins. The functionality of the DRDY pins remains unaffected.

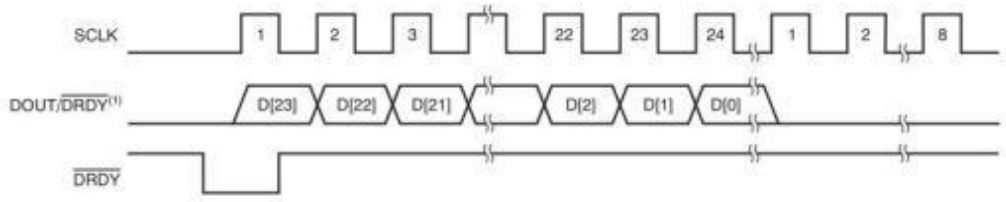
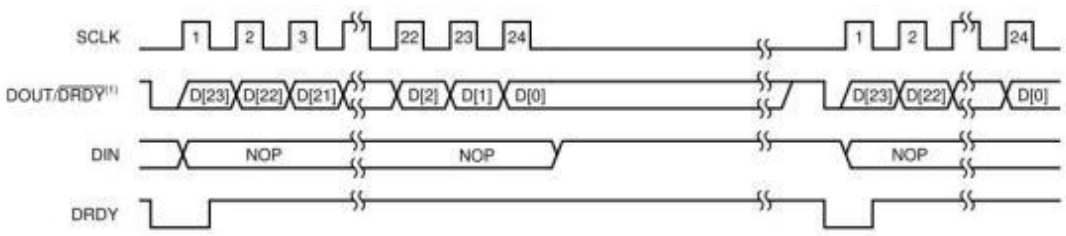


Figure 31. Data retrieval when DRDY mode bit = 0 (disabled)

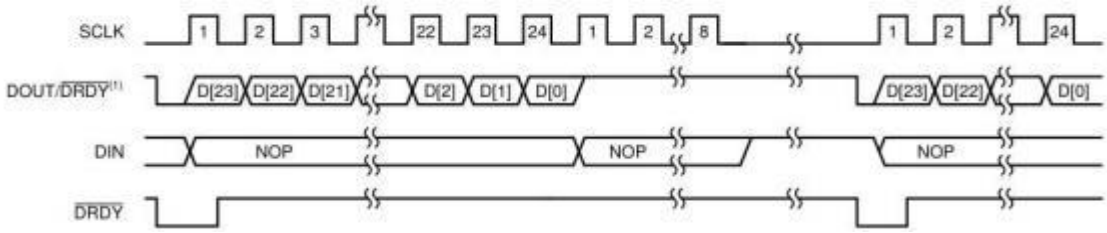
When the DRDY mode bit is enabled and a new conversion is complete, DOUT/DRDY will go low if it was high. If it was already low, DOUT/DRDY will first go high and then low (as shown in Figure 32). Similar to the DRDY pin, a falling edge on the DOUT/DRDY pin indicates that a new conversion result is ready. After DOUT/DRDY goes low, if the device is in continuous read mode, data can be output sequentially by providing 24 SCLKs. To force DOUT/DRDY to go high (so that DOUT/DRDY can poll 0 instead of waiting for a falling edge), a No Operation (NOP) command or any other command that does not load the data output register can be sent after reading the data. Since SCLKs can only be sent in multiples of 8, a NOP can be sent to force DOUT/DRDY to go high if no other commands are pending. After the conversion result is fully read, the DOUT/DRDY pin goes high on the first rising edge of the SCLK (as shown in Figure 33). The same conditions apply after the RREG command. After reading all register bits, the first rising edge of SCLK forces DOUT/DRDY high. Figure 34 shows an example of reading using the RREG command.

Sending an additional NOP command after registering will force the DOUT/DRDY pin to go high.



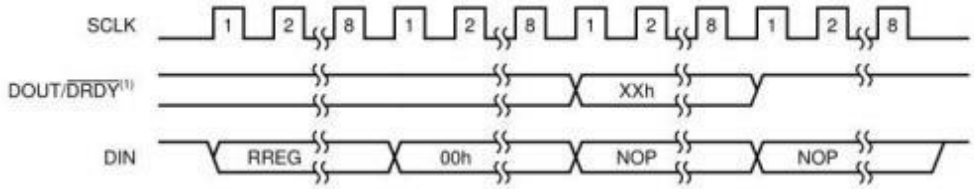
(1) CS is connected to a low level

Figure 32. Data retrieval (enable) when DRDY mode bit is 1



(1) DRDY mode bit enabled, CS connected to low level

Figure33. After the retrieval conversion results are obtained, DOUT/DRDY is forcibly raised



(1) DRDY mode bit enabled, CS connected to low level

Figure34. After reading the register data, DOUT/DRDY is forcibly raised

SPI Reset

There are several ways to reset SPI communication. To reset the serial interface (without resetting registers or digital filters), pull the CS pin high. Pulling the RESET pin low will reset the serial interface and all other digital functions. It will also restore all registers to their default values and begin a new transition.

In systems where CS is permanently connected low, register write operations must always be completed in 8-bit increments. If a small fault on SCLK interrupts SPI communication, the device will not recognize the command. If data is corrupted and the CS pin is permanently held low, the device will perform a timeout for all listed commands. The SPI timeout will reset the interface if 64 transition cycles are idle.

SPI Communication in Power-Down Mode

When the START pin is low or the device is in power-down mode, only the RDATA, RDATAC, SDATAC, WAKEUP, and NOP commands can be issued. The RDATA command can be used to repeatedly read the last conversion result in power-down mode. Other commands have no effect because the internal clock is turned off in power-down mode to save power.

Data format

This device provides 24 bits of data in binary two's complement format. The size of a code (LSB) is calculated using Equation 20.

$$1LSB = (2 \times V_{REF} / Gain) / 2^{24} = +FS / 2^{23} \quad (20)$$

A positive full-scale (FS) input [VIN ≥ (+FS – 1 LSB) = (VREF / gain – 1 LSB)] produces an output code of 7FFFFFh, while a negative full-scale input (VIN ≤ –FS = –VREF / gain) produces an output code of 800000h. For signals exceeding full scale, the output is clipped at these codes. Table 18 summarizes the ideal output codes for different input signals.

Table 18. The relationship between the ideal output code and the input signal

Input Signal, VIN(AINP – AINN)	Ideal Output Code (1)
≥FS ($2^{23} - 1$)/2^{23}	7FFFFFh
FS/2^{23}	000001h
0	000000h
–FS/2^{23}	FFFFFFh
≤–FS	800000h

The effects of noise, linearity, offset, and gain error are eliminated.

The mapping from analog input signal to output code is shown in Figure 35.

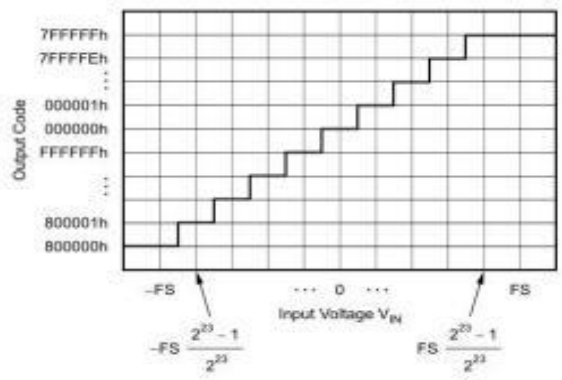


Figure 35. Code Conversion Diagram

Command

The device provides 13 commands to control its operation, as shown in Table 19. Some commands are independent (WAKEUP, SLEEP, SYNC, RESET, SYSOCAL, SYSGCAL, and SELFOCAL). There are also three commands for controlling data reading from the device (RDATA, RDATAC, and SDATAC). Commands for reading from the device (RREG) and writing to the device (WREG) configuration register data require additional information as part of the instruction. No-Operation (NOP) commands can be used to output data from the device one by one without requiring individual command input.

Operands:

• n = Number of registers to read or write (bytes – 1)

• r = registers (0 to 15)

• x = doesn't care

Table 19. SPI Commands

Command	Description	First command byte	Second command byte
WAKEUP	Exit power saving mode	0000 000x(00h,01h)	
SLEEP	Enter power saving mode	0000 001x(02h,03h)	
SYNC	Synchronous ADC conversion	0000 010x(04h,05h)	0000 010x(04h,05h)
RESET	Reset to default value	0000 011x(06h,07h)	
START/SYNC	Command and control conversion	0000 100x(08h,09h)	
STOP	Stop command control conversion	0000 101x(0ah,0bh)	
NOP	No operation	1111 1111(FFh)	
RDATA	Read data once	0001 001x(12h, 13h)	
RDATAC	Read data continuously mode	0001 010x(14h, 15h)	
SDATAC	Stop reading data in continuous mode	0001 011x(16h, 17h)	
RREG	From register rrrr read	0010 rrrr(2xh)	0000 nnnn
WREG	Write to register rrrr	0100 rrrr(4xh)	0000 nnnn
SYSOCAL	System offset calibration	0110 0000(60h)	
SYSGCAL	System gain calibration	0110 0001(61h)	
SELFOCAL	Self-off calibration	0110 0010(62h)	

WAKEUP(0000 000x)

Use a wake-up command to power on the device after a sleep command. After the wake-up command is executed, the device powers on on the falling edge of the eighth SCLK.

SLEEP(0000 001x)

The SLEEP command puts the device into power-saving mode. When the SLEEP command is issued, the device completes the current transition and then enters power-saving mode. Note that this command does not automatically shut down the internal reference voltage source; see the VREFCON bit of each device in MUX1 for details. To exit power-down mode, issue a wake-up command. A single transition can be performed by issuing a wake-up command followed by a SLEEP command. Both WAKEUP and SLEEP are software commands, equivalent to using the START pin to control the device, as shown in Figure 36. Note that if the START pin is held low, or if the START/SYNC command controls the single transition mode, the wake-up command will not power on the device. When using the SLEEP command, CS must be held low during power-down mode.

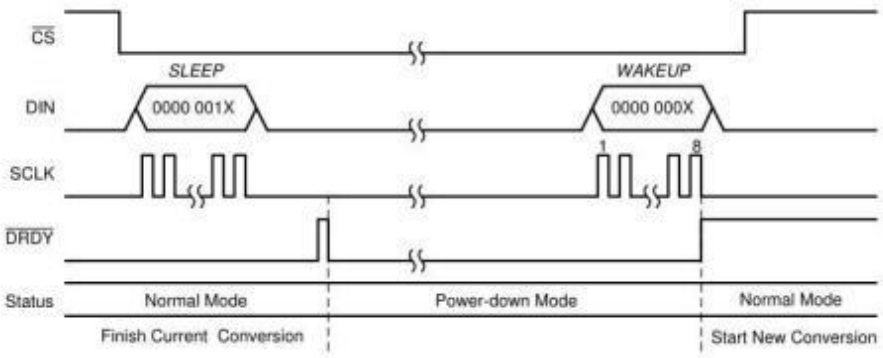


Figure 36. Sleep and wake command operations

SYNC(0000 010x)

The SYNC command resets the ADC digital filter and initiates a new conversion. Multiple devices connected to the same SPI bus can be synchronized by simultaneously issuing the SYNC command to all devices on their DRDY pins.

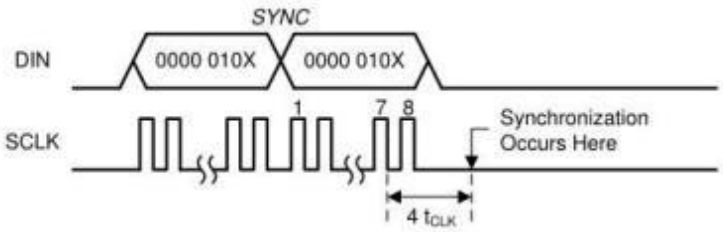


Figure 37. Synchronous command operation

RESET (0000 011x)

The RESET command restores the registers to their default values. This command also resets the digital filters. The RESET command is equivalent to using the RESET pin to reset the device. However, the RESET command does not reset the serial interface. If a reset command is issued when the serial interface is out of sync due to a glitch on SCLK, the device will not reset. The CS pin can be used to reset the serial interface first, and then a reset command can be issued to reset the device. When the system clock frequency is 4.096MHz, the reset command keeps the registers and decimation filter in a reset state for 0.6ms, similar to a hardware reset. Therefore, SPI communication can only be initiated 0.6ms after the RESET command is issued, as shown in Figure 38.

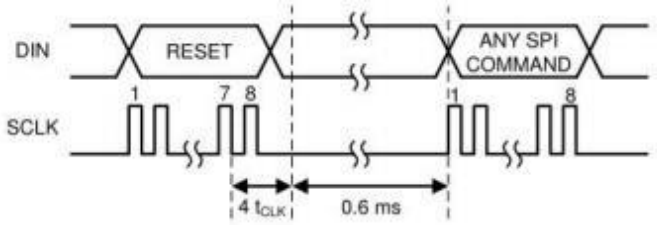


Figure 38. SPI After resetSPI communication

START/SYNC (0000 100x)

The START/SYNC command controls the device to enter command-controlled conversion mode. In single-trigger mode, the START/SYNC command is used to initiate a single conversion, or (when sent during an ongoing conversion) to reset the digital filter and then restart a new single conversion. When the device is set to continuous conversion mode, a START/SYNC command must be issued to begin continuous conversion. During conversion in continuous conversion mode, sending the START/SYNC command resets the digital filter and restarts the continuous conversion.

STOP (0000 101x)

When the device is in START/SYNC command control switching mode, it can exit this mode by sending a STOP command. The device is powered on on the falling edge of the eighth SCLK.

RDATA (0001 001x)

The RDATA command loads the most recent conversion result into the output register. After issuing this command, the conversion result is read by sending 24 SCLKs, as shown in Figure 39. This command also applies to RDATAC mode.

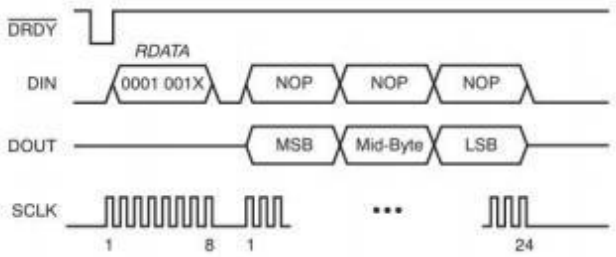


Figure 39. Read data once

When performing multiple reads on the conversion result, the full-duplex communication feature of the serial interface is utilized. When the last 8 bits of the conversion result are shifted out during the first read operation, the RDATA command can be sent, as shown in Figure 40.

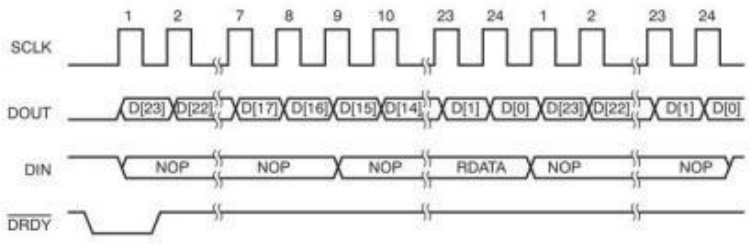


Figure 40. Use in full-duplex modeRDATA

RDATAC (0001 010x)

The RDATAC command enables continuous read mode. This is the default mode after power-on or reset. In continuous read mode, new conversion results are automatically loaded into DOUT. Conversion results can be received from the device after the DRDY signal goes low by sending 24 SCLKs. It is not necessary to read back all bits as long as the number of bits read is a multiple of 8. The RDATAC command must be issued after DRDY goes low, and the command takes effect on the next DRDY. Ensure that data retrieval (conversion result or register readback) is completed before DRDY returns low; otherwise, the resulting data will be corrupted. Successful register read operations in RDATAC mode require knowledge of when the next falling edge of DRDY occurs.

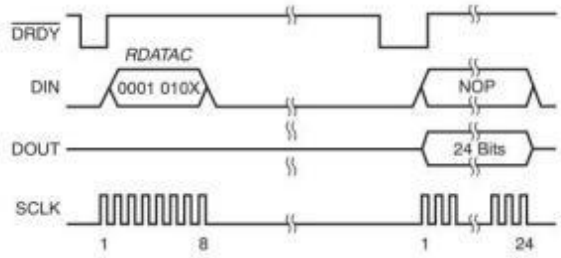


Figure 41. Continuous data reading

SDATAC (0001 011x)

The SDATAC command terminates continuous data read mode. In continuous data read mode, when DRDY goes low, the conversion result is not automatically loaded into DOUT; register read operations can be performed without interruption due to the loading of a new conversion result into the output shift register. Use the RDATA command to retrieve the converted data. The SDATAC command takes effect after the next DRDY.

If there is no active monitoring of DRDY data conversions, stopping continuous data reading mode is the preferred method for reading data. In this mode, the completion of a new ADC conversion will not interrupt the reading of ADC data.

RREG (0010rrrr, 0000nnnn)

The RREG command starts at the register address specified in the instruction and outputs data from up to 15 registers. The number of registers read is 1 plus the value of the second byte. If the count exceeds the remaining registers, the address returns to the starting position. The two-byte command structure of RREG is shown below.

• First command byte: 0010 rrrr, where rrrr is the address of the first register to be read

• The second command byte: 0000 nnnn, where nnnn is the number of bytes to read –1

• Byte: Data read from the register is output via nop

When reading register data, the full-duplex feature of the serial interface cannot be used. For example, when reading VBIAS and MUX1 data, the SYNC command cannot be issued, as shown in Figure 42. Any commands sent during register data reading will be ignored. Therefore, we recommend sending nop via DIN when reading register data.

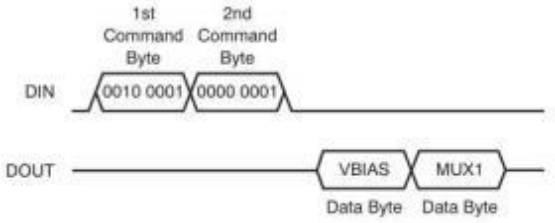


Figure 42. Read from register

WREG (0100rrrr,0000nnnn)

The WREG command writes to registers, starting with the register specified in the instruction. The number of registers written is 1 plus the value of the second byte. The command structure for WREG is shown below.

• First command byte: 0100rrrr, where rrrr is the address of the first register to be written

• The second command byte: 0000nnnn, where nnnn is the number of bytes to be written –1

• Byte: The data to be written to the register

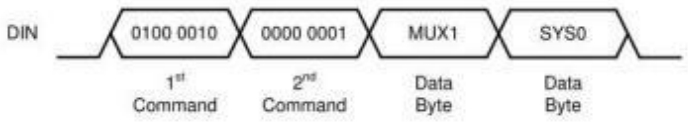


Figure 43. Write to register

SYSOCAL (0110 0000)

The SYSOCAL command initiates system offset calibration. For system offset calibration, the input must be externally shorted to a voltage within the input common-mode range. The input should be close to the midpoint of the supply voltage (AVDD+AVSS)/2. The OFC register is updated upon command completion. The timing of the calibration command is shown in Figure 44.

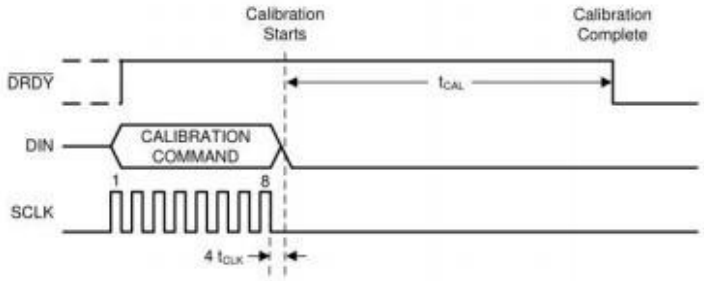


Figure 44. Calibration Command

SYSGCAL (0110 0001)

The SYSGCAL command initiates system gain calibration. For system gain calibration, the input should be set to full scale. The FSC register is updated after this operation. The timing of the calibration command is shown in Figure 44.

SELFOCAL (0110 0010)

The SELFOCAL command initiates self-offset calibration. Internally, the device shorts the input to the intermediate power supply and performs the calibration. The OFC register is updated after this operation. The timing of the calibration command is shown in Figure 44.

NOP (1111 1111)

This is a no-action command. It is used to output data without requiring a command to be entered.

DADS1248 Register Mapping

Table 20. DADS 1248 Register Mapping

ADDRESS	REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00h	MUX0	BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]		
01h	VBIAS	VBIAS[7:0]							
02h	MUX1	CLKSTAT	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		
03h	SYS0	CM	PGA[2:0]			DR[3:0]			
04h	OFC0	OFC[7:0]							
05h	OFC1	OFC[15:8]							
06h	OFC2	OFC[23:16]							
07h	FSC0	FSC[7:0]							
08h	FSC1	FSC[15:8]							
09h	FSC2	FSC[23:16]							
0Ah	IDAC0	ID[3:0]				DRDY MODE	IMAG[2:0]		
0Bh	IDAC1	I1DIR[3:0]				I2DIR[3:0]			
0Ch	GPIOCFG	IOCFG[7:0]							
0Dh	GPIODIR	IODIR[7:0]							
0Eh	GPIODAT	IODAT[7:0]							

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Detailed Register Definitions for DADS1248

MUX0 — Multiplexer Control Register 0 (offset=00h) [reset=01h]

This register allows selection of any combination of differential inputs on either input channel. Note that this setting can be overridden by the MUXCAL and VBIAS bits.

Figure 45. Multiplexer Control Register 0

7	6	5	4	3	2	1	0
BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]		
R/W-0h		R/W-0h			R/W-1h		

Legend : R/W = Read / Write; R = Read Only; -n = Reset Value; -x = Variable

Table 21. Multiplexer Control Register0 Register field description

Bit	Field	Type	Reset	Description
7:6	BCS[1:0]	R/W	0h	Failure detection current source register These position control sensors are equipped with a setting current source for burnout detection. 00: Failure current source off (default) 01: Failed current source turned on, 0.5 μA 10: Failed current source turned on, 2 μA 11: Failed current source turned on, 10 μA
5:3	MUX_SP[2:0]	R/W	0h	Multiplexer Selection - ADC Positive input Positive input channel selection bit 000: AIN0 (default) 001: AIN1 010: AIN2 011: AIN3 100: AIN4 101: AIN5 110: AIN6 111: AIN7
2:0	MUX_SN[2:0]	R/W	1h	Multiplexer Selection - ADC negative input Negative input channel selection bit 000: AIN0 001: AIN1 (default) 010: AIN2 011: AIN3 100: AIN4 101: AIN5 110: AIN6 111: AIN7

VBias— Bias Voltage Register (offset=01h) [reset=00h]

Figure 46. Bias Voltage Register

7	6	5	4	3	2	1	0
VBIAS[7:0]							
R/W-00h							

Legend: R/W = Read/Write; R = Read Only; -n = Reset Value; -x = Variable

Table22. Bias Voltage Register Domain Description

Bit	Field	Type	Reset	Description
7	VBIAS[7]	R/W	0h	VBIAS[7] Voltage Enable The bias voltage applied to AIN7 is the intermediate supply voltage (AVDD + AVSS) / 20: Bias voltage is not enabled (default). 1: Bias voltage applied to AIN7
6	VBIAS[6]	R/W	0h	VBIAS[6] Voltage Enable The bias voltage applied to AIN6 is the intermediate supply voltage (AVDD + AVSS) / 20: Bias voltage is not enabled (default). 1: Bias voltage applied to AIN6
5	VBIAS[5]	R/W	0h	VBIAS[5] Voltage Enable The bias voltage applied to AIN5 is the intermediate supply voltage (AVDD + AVSS) / 20: Bias voltage is not enabled (default). 1: Bias voltage applied to AIN5
4	VBIAS[4]	R/W	0h	VBIAS[4] Voltage Enable The bias voltage applied to AIN4 is the intermediate supply voltage (AVDD + AVSS) / 20: Bias voltage is not enabled (default). 1: Bias voltage applied to AIN4
3	VBIAS[3]	R/W	0h	VBIAS[3] Voltage Enable The bias voltage applied to AIN3 is the intermediate supply voltage (AVDD + AVSS) / 20: Bias voltage is not enabled (default). 1: Bias voltage applied to AIN3
2	VBIAS[2]	R/W	0h	VBIAS[2] Voltage Enable The bias voltage applied to AIN2 is the intermediate supply voltage (AVDD + AVSS) / 20: Bias voltage is not enabled (default). 1: Bias voltage applied to AIN2
1	VBIAS[1]	R/W	0h	VBIAS[1] V Voltage Enable The bias voltage applied to AIN1 is the intermediate supply voltage (AVDD + AVSS) / 20: Bias voltage is not enabled (default). 1: Bias voltage applied to AIN1
0	VBIAS[0]	R/W	0h	VBIAS[0] Voltage Enable The bias voltage applied to AIN0 is the intermediate supply voltage (AVDD + AVSS) / 20: Bias voltage is not enabled (default). 1: Bias voltage applied to AIN0

Mux1 — Multiplexer control register1(offset=02h) [reset=x0h]

Figure 47. Multiplexer Control Register 1

7	6	5	4	3	2	1	0
CLKSTAT	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		
R-xh	R/W-0h		R/W-0h		R/W-0h		

Legend : R/W = Read / Write; R = Read Only; -n = Reset value; -x = Variable

Table 23. Multiplexer Control Register0 Register field description

Bit	Field	Type	Reset	Description
7	CLKSTAT	R	xh	Clock status This bit is read-only, indicating that the internal oscillator is in use or an external clock is being employed. 0: Use internal oscillator 1: An external clock is being used.
6:5	VREFCON[1:0]	R/W	0h	Internal reference voltage control These bits control the internal reference voltage. These bits allow the reference voltage to be fully turned on or off, or allow the reference voltage state to follow the device state. Note that the IDAC function requires an internal reference voltage source to operate. 00: Internal reference voltage source is always off (default) 01: Internal reference voltage source is always on. 10 or 11: The internal reference voltage source is turned on when a conversion is in progress; the internal reference voltage source is turned off when the device receives a sleep command or the START pin goes low.
4:3	REFSELT[1:0]	R/W	0h	Reference selection control These bits select the reference input for the ADC. 00: Select REFP0 and REFN0 reference inputs (default) 01: Select REFP1 and REFN1 reference voltage input 10: Select the internal reference voltage source 11: Select the internal reference voltage source and connect it internally to the REFP0 and REFN0 input pins.
2:0	MUXCAL[2:0] (1)	R/W	0h	System monitoring These bits are used to select the system monitor. The MUXCAL selection overrides the selection of the MUX0, MUX1, and VBIAS registers (including MUX_SP, MUX_SN, VBIAS, and reference voltage selection). 000: Normal operation (default) 001: Offset calibration. Analog input disconnected; AINP and AINN are internally connected to the intermediate power supply (AVDD + AVSS)/2. 010: Gain calibration. The analog input is connected to a reference voltage source. 011: Temperature Measurement. The input is connected to a diode circuit that generates a voltage proportional to the ambient temperature of the device. 100: REF1 Monitor. Analog input disconnected; AINP and AINN internally connected to (V(ref P1)-V(ref n1))/4). 101: REF0 Monitor. Analog input disconnected; AINP and AINN internally connected to (V(ref P0)-V(ref n0))/4. 110: Analog power supply monitor. Analog input disconnected; AINP and AINN are internally connected to (AVDD – AVSS)/4. 111: Digital power supply monitor. Analog input disconnected; AINP and AINN internally connected to (DVDD – DGND)/4.

When using any reference voltage monitor, the internal reference voltage should be enabled.

Table 24 provides each MUXCAL settings ADC input connection and PGA settings. When MUXCAL resumes normal operation or when the imbalance measurement is completed, the PGA settings are restored to the original SYS0 register settings.

Table 24. Multiplexer Control Register 0 Register field description

MUXCAL [2:0]	PGA Gain Settings	ADC Input
000	Depend on SYS0 Register settings	Normal operation
001	Depend on SYS0 Register settings	Input short-circuit to the intermediate power supply (AVDD + AVSS) / 2
010	Forced 1	$V(_{REFP}) - V(_{REFN})$ (Full Scale)
011	Forced 1	Temperature measurement diode
100	Forced 1	$(V(_{REFP1}) - V(_{REFN1}))$ / 4
101	Forced 1	$(V(_{REFP0}) - V(_{REFN0}))$ / 4
110	Forced 1	(AVDD – AVSS) / 4
111	Forced 1	(DVDD – DGND) / 4

SYS0 — System Control Register 0 (offset = 03h) [reset = 00h]

Figure 48. System Control Register0

7	6	5	4	3	2	1	0
CM	PGA[2:0]			DR[3:0]			
R/W-0h	R/W-0h			R/W-0h			

Legend : R/W = Read / Write; R = Read Only; -n = Reset Value; -x = Variable

Table 25. System Control Register0 field description

Bit	Domain	Type	Reset	Description
7	CM	R/W	0h	Switching modes This bit sets the start / synchronization command and controls the switching mode of the device. 0: Single Shooting Mode (Default) 1: Continuous Conversion Mode
6:4	PGA[2:0]	R/W	0h	PGA gain settings These bits determine the PGA gain. 000: PGA = 1 (Default) 001: PGA = 2 010: PGA = 4 011: PGA = 8 100: PGA = 16 101: PGA = 32 110: PGA = 64 111: PGA = 128
3:0	DR[3:0]	R/W	0h	Data output rate settings These bits determine ADC Data output rate 0000: DR = 5 SPS (Default) 0001: DR = 10 SPS 0010: DR = 20 SPS 0011: DR = 40 SPS 0100: DR = 80 SPS 0101: DR = 160 SPS 0110: DR = 320 SPS 0111: DR = 640 SPS 1000: DR = 1000 SPS 1001 to 1111: DR = 2000 SPS

OFC— Offset Calibration Coefficient Register (offset=04h, 05h, 06h) [reset=00h, 00h, 00h]

Table 49. Offset Calibration Coefficient Register

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
OFC[15:8]							
R/W-0h							
7	6	5	4	3	2	1	0
OFC[23:16]							
R/W-0h							

Legend : R/W = Read / Write; R = Read Only; -n = Reset Value; -x = Variable

Table 26. Description of the offset calibration coefficient register field

Bit	Field	Type	Reset	Description
23:0	OFC[23:0]	R/W	000000h	Offset Calibration Register Composed of three registers ADC 24 -bit offset calibration word. 24 -bit It is in two's complement format, with the internal left shifted to match. ADC 24 -bit conversion junction Alignment. Before full-scale operation, the ADC subtracts from the conversion result. Register value.

FSC— Full-scale calibration coefficient register (offset = 07h, 08h, 09h) [reset = PGA related]
These bits constitute the full-scale calibration coefficient register. For each PGA setting, the FSC reset value is factory-tuned. Whenever the PGA setting changes, the factory-tuned FSC reset value is automatically loaded.

Figure 50. Full-scale calibration coefficient register

7	6	5	4	3	2	1	0
FSC[7:0]							
R/W-00h							
7	6	5	4	3	2	1	0
FSC[15:8]							
R/W-00h							
7	6	5	4	3	2	1	0
FSC[23:16]							
R/W-20h							

Legend : R/W = Read / Write; R = Read Only; -n = Reset value; -x = Variable

Table 27. Full-scale calibration coefficient register field description

Bit	Field	Type	Reset	Description
23:0	FSC[23:0]	R/W	200000h	Full-scale calibration register Composed of three registers The ADC uses a 24- bit full-scale calibration word. A 24- bit word is standard binary. The ADC stores the gain coefficient obtained after gain calibration in the FSC register, the ADC multiplies the scaling factor by the conversion result. Whenever PGA settings change, automatically load the factory adjustments. FSC reset value.

IDAC0 — IDAC Control Register 0 (offset = 0Ah) [reset = x0h]

Figure 51. IDAC Control Register0

7	6	5	4	3	2	1	0
ID[3:0]				DRDY MODE	IMAG[2:0]		
R-xh				R/W-0h	R/W-0h		

Legend: R/W = Read/Write; R = Read Only; -n = Reset value; -x = Variable

Table 28. IDAC Control Register0 field description

Bit	Domain	Type	Reset	Description
7:4	ID[3:0]	R	xh	Version identifier Read-only, factory programming bit; used for version identification.
3	DRDY MODE	R/W	0h	Data ready mode settings This bit setting DOUT/DRDY The function of the pins. DRDY In any setting of the mode bit, dedicated DRDY Pin continues to point This indicates that the data is ready and active low. 0: DOUT/DRDY The pin is used for data output only (default) . 1: DOUT/DRDY The pin is used for both data output and data transfer ready. Active low (1)
2:0	IMAG[2:0]	R/W	0h	IDAC excitation current amplitude MCT1248 has two current sources (IDACs) that can be used for sensor excitation. This IMAG controls the amplitude of the excitation current. The IDACs require the internal reference voltage source to be enabled. 000: Off (default) 001: 50 μA 010: 100 μA 011: 250 μA 100: 500 μA 101: 750 μA 110: 1000 μA 111: 1500 μA

It cannot be u sed in SDATAC mode IDAC1—IDAC Control Register 1 (offset=0Bh) [reset=FFh]

Figure 52. IDAC Control Register 1

7	6	5	4	3	2	1	0
I1DIR[3:0]				I2DIR[3:0]			
R/W-Fh				R/W-Fh			

Legend: R/W = Read/Write; R = Read Only; -n = Reset Value; -x = Variable

Table 29. IDAC Control register field description

Bit	Domain	Type	Reset	Description
7:4	I1DIR[3:0]	R/W	Fh	IDAC Excitation Current Output 1 These bits select the output pin of the first excitation current source. 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 10x0: IEXC1 10x1: IEXC2 11xx: Disconnect (default)
3:0	I2DIR[3:0]	R/W	Fh	IDAC Excitation Current Output 2 These bit select the output pins of the second excitation current source. 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 10x0: IEXC1 10x1: IEXC2 11xx: Disconnect (default)

GPIOCFG — GPIO Configuration Register (offset = 0Ch) [reset = 00h]

Figure 53. GPIO Configuration Register

7	6	5	4	3	2	1	0
IOCFG[7:0]							
R/W-00h							

Legend: R/W = Read/Write; R = Read Only; -n = Reset Value; -x = Variable

Table 30. GPIO Configuration register field description

Bit	Domain	Type	Reset	Description
7	IOCFG[7]	R/W	0h	GPIO[7] (AIN7) Pin configuration 0: GPIO[7] is not enabled (default) 1: GPIO[7] is applied to AIN7
6	IOCFG[6]	R/W	0h	GPIO[6] (AIN6) Pin Configuration 0: GPIO[6] Not enabled (default) 1: GPIO[6] is applied to AIN6
5	IOCFG[5]	R/W	0h	GPIO[5] (AIN5) Pin Configuration 0: GPIO[5] Not enabled (default) 1: GPIO[5] is applied to AIN5
4	IOCFG[4]	R/W	0h	GPIO[4] (AIN4) Pin Configuration 0: GPIO[4] Not enabled (default) 1: GPIO[4] is applied to AIN4
3	IOCFG[3]	R/W	0h	GPIO[3] (AIN3) Pin configuration 0: GPIO[3] is not enabled (default) 1: GPIO[3] is applied to AIN3
2	IOCFG[2]	R/W	0h	GPIO[2] (AIN2) Pin configuration 0: GPIO[2] is not enabled (default) 1: GPIO[2] is applied to AIN2
1	IOCFG[1]	R/W	0h	GPIO[1] (REFN0) Pin configuration 0: GPIO[1] is not enabled (default) 1: GPIO[1] is applied to REFN1
0	IOCFG[0]	R/W	0h	GPIO[0] (REFP0) Pin configuration 0: GPIO[0] is not enabled (default) 1: GPIO[0] is applied to REFP0

GPIODIR—GPIO Direction Register (offset = 0Dh) [reset = 00h]

Figure 54. GPIO Direction register

7	6	5	4	3	2	1	0
IODIR[7:0]							
R/W-00h							

Legend: R/W = Read/Write; R = Read Only; -n = Reset value; -x = Variable

Table 31. GPIO Direction Register Field Description

Bit	Domain	Type	Reset	Description
7	IODIR[7]	R/W	0h	GPIO[7] (AIN7) Pin direction WillGPIO[7] configured asGPIO input orGPIO output 0: GPIO[7] is for output (default) 1: GPIO[7] is the input
6	IODIR[6]	R/W	0h	GPIO[6] (AIN6) Pin direction WillGPIO[6] configured asGPIO input orGPIO output 0: GPIO[6] is for output (default) 1: GPIO[6] is the input
5	IODIR[5]	R/W	0h	GPIO[5] (AIN5) pin orientation Configure GPIO[5] as a GPIO input or GPIO output 0: GPIO[5] is an output (default) 1: GPIO[5] is the input
4	IODIR[4]	R/W	0h	GPIO[4] (AIN4) pin orientation Configure GPIO[4] as a GPIO input or GPIO output 0: GPIO[4] is an output (default) 1: GPIO[4] is the input
3	IODIR[3]	R/W	0h	GPIO[3] (AIN3) pin orientation Configure GPIO[3] as a GPIO input or GPIO output 0: GPIO[3] is an output (default) 1: GPIO[3] is the input
2	IODIR[2]	R/W	0h	GPIO[2] (AIN2) pin orientation Configure GPIO[2] as a GPIO input or GPIO output 0: GPIO[2] is an output (default) 1: GPIO[2] is the input
1	IODIR[1]	R/W	0h	GPIO[1] (REFN0) pin orientation Configure GPIO[1] as a GPIO input or GPIO output 0: GPIO[1] is an output (default) 1: GPIO[1] is the input
0	IODIR[0]	R/W	0h	GPIO[0] (REFP0) Pin Direction Configure GPIO[0] as a GPIO input or GPIO output 0: GPIO[0] is an output (default) 1: GPIO[0] is the input

GPIODAT—GPIO Data Register (offset = 0Eh) [reset = 00h]

Figure 55. GPIO Data registerr

7	6	5	4	3	2	1	0
IODAT[7:0]							
R/W-00h							

L Legend: R/W = Read/Write; R = Read Only; -n = Reset Value; -x = Variable

Table 31. GPIO Data register field description

Bit	Domain	Type	Reset	Description
7	IODAT[7]	R/W	0h	GPIO[7] (AIN7) Pin Data Configured as output, reads the value of a register configured as input, writes only to set the register value. 0: GPIO[7] is low (default) 1: GPIO[7] is high
6	IODAT[6]	R/W	0h	GPIO[6] (AIN6) Pin Data Configured as output, reads the value of a register configured as input, writes only to set the register value. 0: GPIO[6] is low (default) 1: GPIO[6] is high
5	IODAT[5]	R/W	0h	GPIO[5] (AIN5) pin data Configured as output, reads the value of a register configured as input, writes only to set the register value. 0: GPIO[5] is low (default) 1: GPIO[5] is high level
4	IODAT[4]	R/W	0h	GPIO[4] (AIN4) pin data Configured as output, reads the value of a register configured as input, writes only to set the register value. 0: GPIO[4] is low (default) 1: GPIO[4] is high
3	IODAT[3]	R/W	0h	GPIO[3] (AIN3) pin data Configured as output, reads the value of a register configured as input, writes only to set the register value. 0: GPIO[3] is low (default) 1: GPIO[3] is high
2	IODAT[2]	R/W	0h	GPIO[2] (AIN2) Pin data Configured as output, reads the value of a register configured as input, writes only to set the register value. 0: GPIO[2] is low (default) 1: GPIO[2] is high
1	IODAT[1]	R/W	0h	GPIO[1] (REFN0) pin data Configured as output, reads the value of a register configured as input, writes only to set the register value. 0: GPIO[1] is low (default) 1: GPIO[1] is high
0	IODAT[0]	R/W	0h	GPIO[0] (REFP0) pin data Configured as output, reads the value of a register configured as input, writes only to set the register value. 0: GPIO[0] is low (default) 1: GPIO[0] is high

Application and Implementation

The DADS1248 is a 24-bit ADC that offers many integrated features, making it easy to measure the most common sensor types, including a variety of temperature and bridge sensors. Key considerations when designing applications using these devices include connecting and configuring the serial interface, designing analog input filtering, establishing a suitable external reference voltage source for ratio measurements, and setting the common-mode input voltage for the internal PGA.

Serial Interface Connection

The serial interface connection principle of DADS1248 is shown in Figure 56.

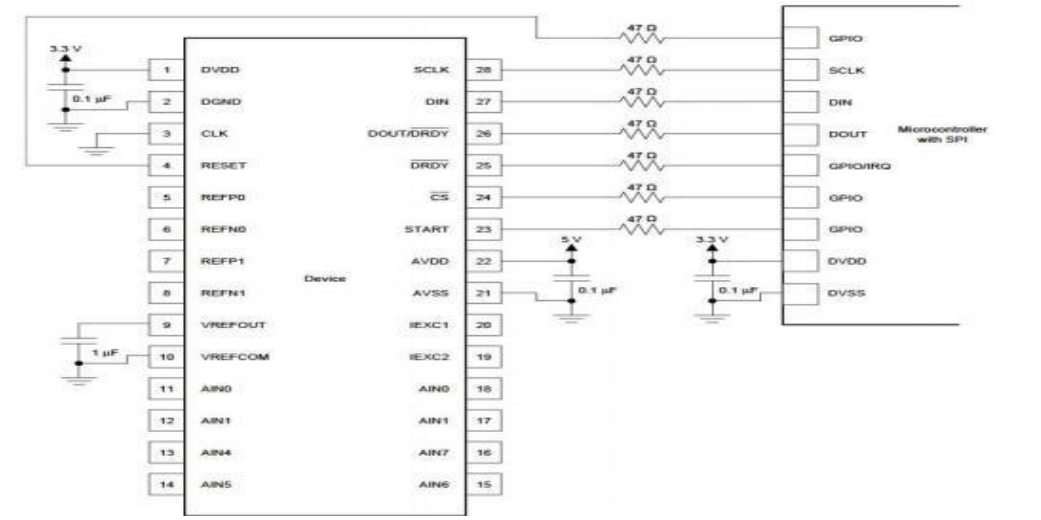

Figure 56. Serial interface connection

Most microcontroller SPI peripherals can work with the DADS1248. This interface operates in SPI mode 1, where CPOL=0 and CPHA=1. In SPI mode 1, SCLK is low and idle; data is sent or modified only on the rising edge of SCLK; data is latched or read by the master and slave on the falling edge of SCLK. We recommend connecting a 47-Ω resistor in series with all digital input and output pins (CS, SCLK, DIN, DOUT/DRDY, DRDY, RESET, and START). This resistor smooths abrupt transitions, suppresses overshoot, and provides some overvoltage protection. Care must be taken to meet all SPI timing requirements, as the additional resistor can interfere with bus capacitance on the digital signal lines.

Analog Input Filtering

Analog input filtering serves two purposes: first, to limit aliasing during the sampling process; and second, to reduce external noise in the measurement. Many sensor signals inherently have limited bandwidth; for example, the output rate of a thermocouple is finite. In such cases, when using a ΔΣADC, the sensor signal will not alias back into the passband. However, any noise picked up along the sensor wiring or application circuitry can potentially alias into the passband .

External Reference and Ratio Measurement

The full-scale range of the DADS1248 is defined by the reference voltage and the PGA gain (FSR = ±VREF/gain). An external reference can be used instead of the integrated 2.048V reference to adapt the FSR to specific system requirements. If VIN > 2.048V, an external reference must be used. For example, to measure signals up to 2.5V, an external 2.5V reference is required. Note that the input signal must be within the common-mode input range to be valid, and the reference input voltage must be between 0.5V and (AVDD - AVSS - 1V).

Establish an Appropriate Common-Mode Input Voltage

The DADS1248 is used to measure various types of signal configurations. However, it is important to correctly configure the device's inputs for the corresponding signal type. DADS1248 features an 8-input multiplexer. Each input can be independently selected as either the positive or negative input for ADC measurement. By using the 8-input multiplexer, users can measure four independent differential input channels. Users can also choose to measure seven channels, using one input as a fixed common input. Regardless of the analog input configuration, ensure that all inputs, including the common input, are within the common-mode input voltage range.

Isolated (or Floating) Sensor Input

Isolated sensors (sensors without a reference to ADC ground) must establish a common-mode voltage within the specified ADC input range. The common-mode voltage level is shifted by biasing with an external resistor, either by connecting the negative lead to ground (bipolar analog supply) or by connecting to a DC voltage (unipolar analog supply). A 2.048V reference output voltage can also be used to provide level shifting for floating sensor inputs.

Unused Inputs and Outputs

To minimize leakage current on analog inputs, unused analog inputs can be floated, connected to an intermediate power supply, or connected to AVDD. Connecting unused analog inputs to AVSS is also possible, but this will result in higher leakage current than the options mentioned above. Do not float unused digital inputs, as this may cause excessive power leakage current. Connect all unused digital inputs to the appropriate level, DVDD or DGND, including in power-down mode. If the DRDY output is not used, leave the off-pin unconnected or tie it to DVDD using a weak pull-up resistor.

Power Supply Recommendations

The device requires two power supplies: an analog power supply (AVDD, AVSS) and a digital power supply (DVDD, DGND). The analog power supply can be bipolar (e.g., AVDD=2.5V, AVSS=-2.5V) or unipolar (e.g., AVDD=3.3V, AVSS=0V) and is independent of the digital power supply. The digital power supply sets the digital I/O levels (except for GPIO levels, which are set by the analog power supply from AVDD to AVSS).

Power Supply Sequencing

The power supplies can be arranged in any order, but under no circumstances should any analog or digital input exceed its respective analog or digital power supply voltage limit. After all power supplies have stabilized, wait at least 216 tCLK cycles before communicating with the device to complete the power-on reset process.

Power Supply Decoupling

Proper power supply decoupling is crucial for optimal performance. AVDD, AVSS (when using a bipolar power supply), and DVDD must be decoupled with capacitors of at least 0.1 µF, as shown in Figure 57. Use low-impedance connections and place bypass capacitors as close as possible to the device's power supply pins. We recommend using multilayer ceramic chip capacitors (MLCCs) to provide power supply decoupling with low equivalent series resistance (ESR) and inductance (ESL) characteristics. For highly sensitive systems or systems in harsh, noisy environments, avoiding the use of vias to connect capacitors to device pins provides superior noise immunity. The use of multiple vias in parallel reduces overall inductance and facilitates connections to the ground plane. We recommend connecting analog and digital grounds together, as close as possible to the device.

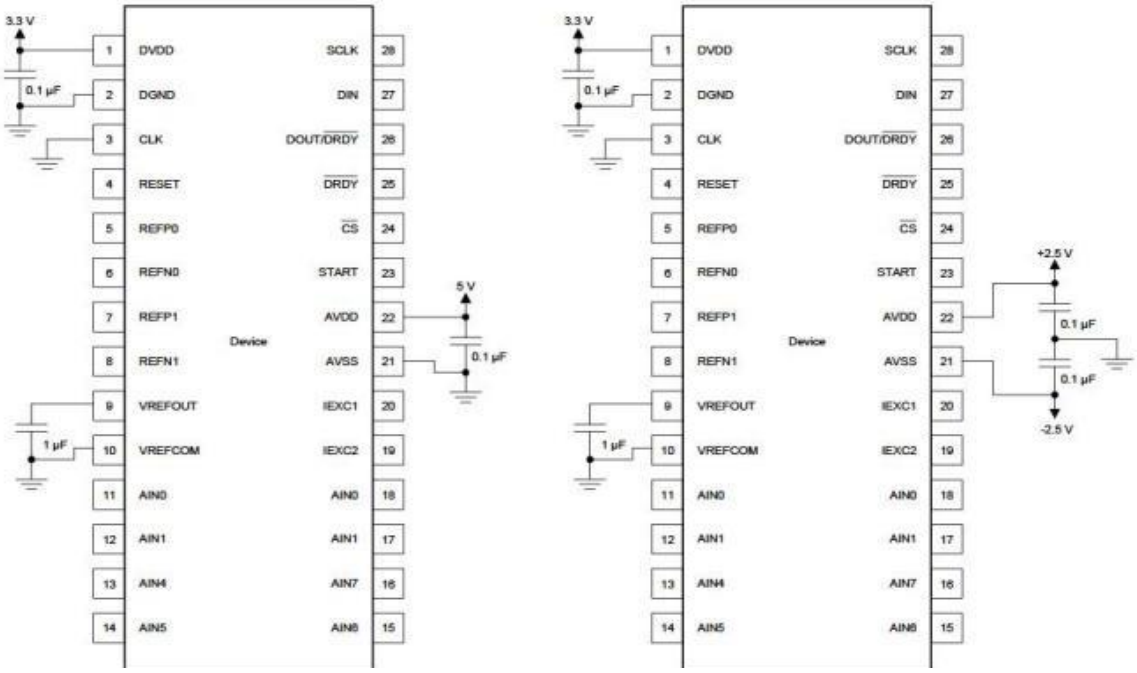

Figure 57. Power decoupling in unipolar and bipolar power supply operation

Layout Guide

We recommend using best design practices when laying out printed circuit boards (PCBs) for analog and digital components. This recommendation generally means separating analog components [such as ADCs, amplifiers, reference devices, digital-to-analog converters (DACs), and analog muxes] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators].

Layout Example

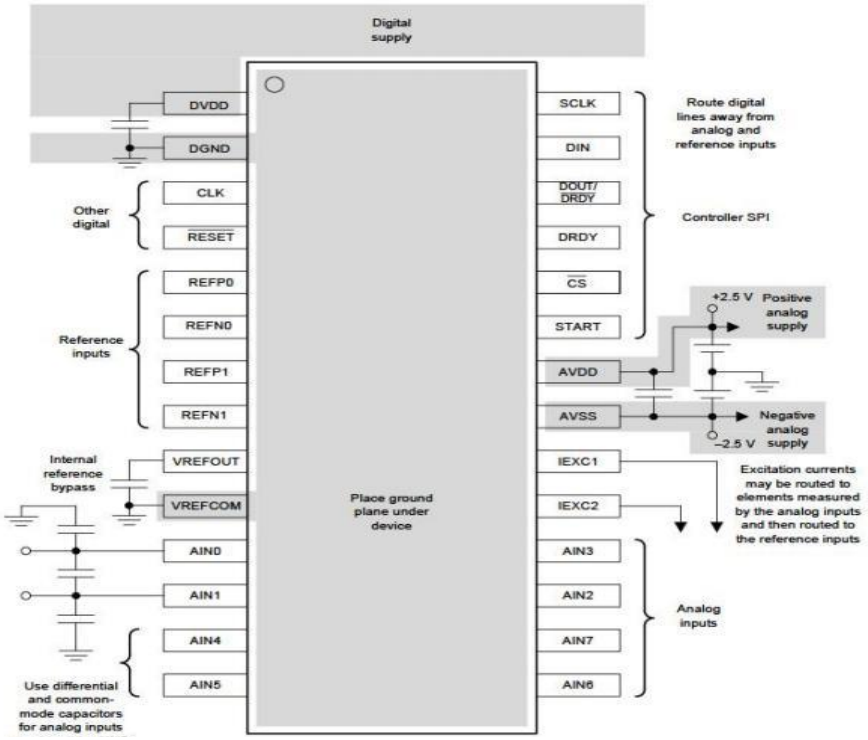

Figure 58. DADS1248 layout example

Device Ordering Information

Product Model	Temperature Range	Packaging Type	Package Quantity	RoHS
DADS1248	–40 °C to +85 °C	28-SSOP	1000/reel	Y