DADS1220/DADS1120, 4-Channel, 2-kSPS, Low-Power, 24-/16-Bit ADC with Integrated PGA and Reference

Features

- Low current consumption: as low as 120μA (typical) in duty cycle mode
- Wide power supply range: 2.3V to 5.5V
- Programmable gain: 1V/V to 128V/V
- Programmable data rate: up to 2kSPS
- Up to 20-bit effective resolution (1220)

  16-bit noise-free resolution (at 20 SPS) (1120)
- A single-cycle stable digital filter is used to achieve 50Hz and 60Hz harmonic suppression at 20SPS
- Two differential inputs or four single-ended inputs
- Dual-matched programmable current sources: 10 μA to 1.5mA (1220) / 50 μA to 1.5mA (1120)
- Integrated 2.048V reference voltage: drift 5ppm/℃ (typical)
- Integrated 2% precision oscillator
- Integrated temperature sensor: accuracy 0.5°C (typical)
- SPI-compatible interface (Mode 1)
- Package: 4.0mm × 4.0mm × 0.85mm ultra-thin quad flat without leads (QFN16L)

Applications

- Temperature sensor measurement:
  - Thermistor
  - thermocouple
  - Resistance temperature detector (RTD):

  2-wire, 3-wire, or 4-wire type
- Resistance bridge sensor measurement:
  - pressure sensor
  - stress gauge
  - Weighing instruments
- Portable instrument
- Industrial automation and process control

Product Description

The DADS1220/DADS1120 is a precision 24/16-bit analog-to-digital converter (ADC) that integrates features to reduce system cost and component count in small sensor signal measurement applications. The device features two differential inputs or four single-ended inputs via an input multiplexer (MUX), a low-noise programmable gain amplifier (PGA), two programmable drive current sources, a voltage reference, an oscillator, a low-side switch, and a precision temperature sensor.

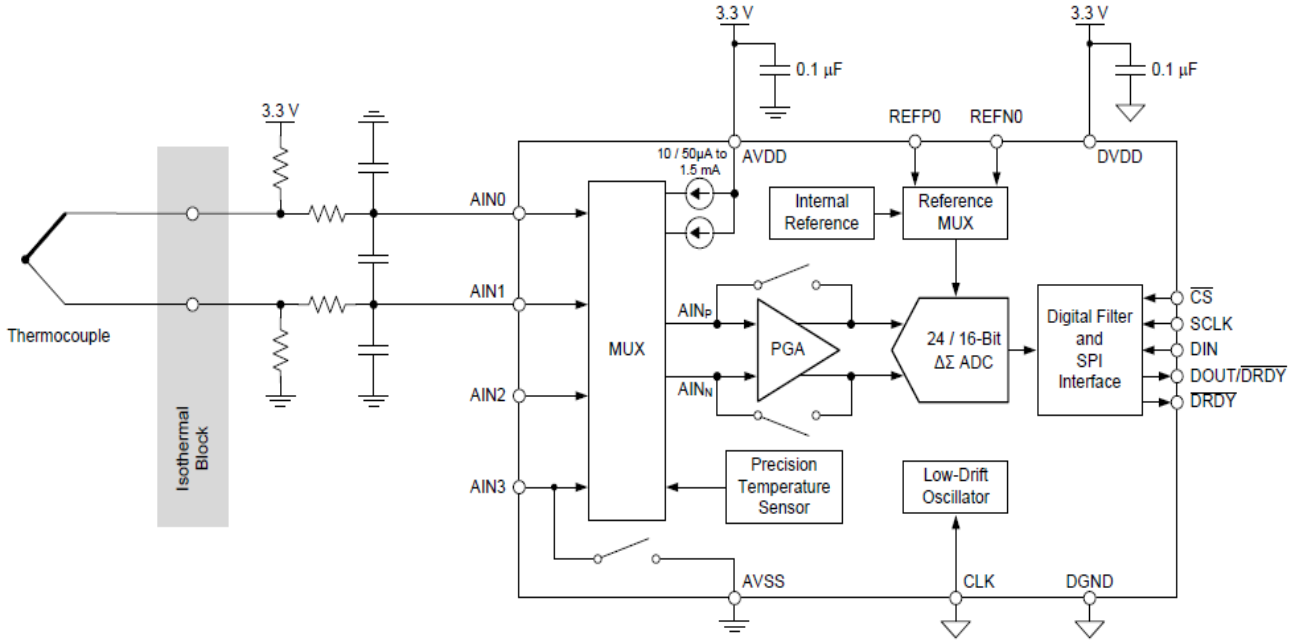
This device can perform conversions at sampling data rates up to 2000 samplings per second (SPS) and is stable within a single cycle. For industrial applications in noisy environments, the digital filter provides simultaneous 50Hz and 60Hz rejection at a sampling frequency of 20 SPS. The internal PGA provides up to 128V of gain. This PGA makes the chip ideal for small sensor signal measurement applications such as resistive temperature detectors (RTDs), thermocouples, thermistors, and resistive bridge sensors. The device supports the measurement of pseudo-differential or fully differential signals when using the PGA. Furthermore, this device can be configured to disable the internal PGA while still providing high input impedance and up to 4VV gain, enabling single-ended measurements.

Power consumption can be as low as 120uA in duty cycle mode with the PGA disabled. The device is available in a leadless QFN16L or Thin Small Outline (TSSOP)-16 package and is rated for operation from -40°C to +125°C.

Device Information:

Model	Packaging Type	Size (nominal value)
DADS1220	QFN16L	4.0mm x 4.0mm
	TSSOP-16	5.00mm x 4.40mm
DADS1120	QFN16L	4.0mm x 4.0mm
	TSSOP-16	5.00mm x 4.40mm

K-Type Thermocouple Measurement



Absolute Maximum Ratings

		Min	Max	Unit
power supply voltage	AVDD to AVSS	-0.3	7	V
	DVDD to DGND	-0.3	7	V
	AVSS to DGND	-2.8	0.3	V
Analog input voltage	AIN0/REFP1, AIN1, AIN2, AIN3/REFN1, REFP0, REFN0	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$,SCLK, DIN, DOUT/$\overline{DRDY}$, $\overline{DRDY}$, CLK	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, any pin except power supply pins	– 10	10	mA
Temperature	Junction temperature, T_J	-40	150	°C
	Storage, T_{stg}	-60	150	°C

Note: Exceeding the absolute maximum ratings listed above may result in permanent damage to the device. These are merely emphasized ratings and do not pertain to functional operation of the device beyond the specifications under these or any other conditions. Prolonged operation at absolute maximum ratings may affect the reliability of the device.

ESD ratings

		Value	Unit
$V_{(ESD)}$ electrostatic discharge	Human body discharge pattern (HBM), compliant with ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Component charging mode (CDM) conforms to JEDEC specification JESD22-C101 (2).	±500	

(1) JEDEC Documents JEP 155 specifies: 500V HBM Able to meet the standard Safe production under ESD control process.
(2) JEDEC Documents JEP 157 specifies: 250 V CDM Able to meet the standard Safe production under ESD control process.

Recommended Operating Conditions

Within the operating ambient temperature range (unless otherwise specified)

			Min	Typ	Max	Unit
Power supply						
	Single-pole analog power supply	AVDD to AVSS	2.3		5.5	V
		AVSS to DGND	-0.1	0	0.1	
	Bipolar analog power supply	AVDD to DGND	2.3	2.5	5.5	V
		AVSS to DGND	-2.75	-2.5	-2.3	
	Digital power supply	DVDD to DGND	2.3		5.5	V
Analog input (1)						
V_{IN}	Common-mode input voltage	$V_{IN} = V_{(AINP)} - V_{(AINN)}$ (2)	$-V_{ref}$ / gain		V_{ref} / gain	V
$V_{(AINx)}$	Absolute input voltage	PGA disabled, gain = 1 to 4	AVSS – 0.1		AVDD + 0.1	V
		PGA enabled, gain = 1 to 128	Please refer to Low Noise PGA part			
V_{CM}	Common-mode input voltage	PGA disabled, gain = 1 to 4	AVSS – 0.1		AVDD + 0.1	V
		PGA enabled, gain = 1 to 128	Please refer to the Low Noise PGA section.			
Reference voltage input (3)						
V_{ref}	Differential reference input voltage	$V_{ref} = V_{(REFPx)} - V_{(REFNx)}$	0.75	2.5	AVDD	V
$V_{(REFNx)}$	Absolute negative reference voltage		AVSS – 0.1		$V_{(REFPx)}$ – 0.75	V
$V_{(REFPx)}$	Absolute positive reference voltage		$V_{(REFNx)}$ + 0.75		AVDD + 0.1	V
External clock source						
$f_{(CLK)}$	external clock frequency		0.5	4.096	4.5	MHz
	Duty cycle		40%		60%	
Digital input						
	Input voltage		DGND		DVDD	V
Temperature range						
T_A	Operating ambient temperature		-40		125	℃

(1) AIN_P and AIN_N represent the positive and negative inputs of the PGA. AINx represents one of the four provided analog inputs. PGA disabled means that the low-noise PGA is turned off and bypassed. In this case, gain values of 1, 2 and 4 are still supported.

(2) Eliminate the effects of offset and gain errors. When PGA is enabled, the limit is ± [(AVDD – AVSS) – 0.4V] / Gain.

(3) REFPx and REFNx represent one of the two differential reference input pairs provided.

Thermal Performance Information

Thermal index (1)		DADS1220/DADS1120		Unit
		VQFN (RVA)	TSSOP (PW)	
		16- pin	16- pin	
$R_{\theta JA}$	Junction to ambient thermal resistance	43.4	99.5	℃/W
$R_{\theta JC(top)}$	Junction to the outer casing (top) thermal resistance	47.3	35.2	℃/W
$R_{\theta JB}$	Junction to circuit board thermal resistance	18.4	44.3	℃/W
ψ_{JT}	Characteristic parameters from tube junction to top	0.6	2.4	℃/W
ψ_{JB}	Junction to circuit board characteristic parameters	18.4	43.8	℃/W
$R_{\theta JC(bot)}$	Junction to the outer casing (bottom) thermal resistance	2.0	N/A	℃/W

(1) For detailed information on traditional and new thermal specifications, please refer to the application report "IC Package Thermal Specifications" (Document No.: SPRA953).

Electrical Characteristics

Minimum and maximum specification values apply to a temperature range of T_A =–40 °C to +125°C. Typical specification values were determined at T_A =25°C. All specification values were determined with AVDD = 3.3V, AVSS = 0V, DVDD = 3.3V, PGA enabled, DR = 20SPS, and external V_{ref}= 2.5V (unless otherwise noted). (1)

Parameter	Test Condition	Min	Typ	Max	Unit
Analog Input					
Absolute input current		Please refer to typical characteristics			
Differential input current		Please refer to typical characteristics			
System performance					
Resolution (no missing code)		24/16			Bit
DR Data transmission rate	Normal mode	20, 45 , 90 , 175 , 330 , 600 , 1000			SPS
	Duty cycle mode	5, 11.25 , 22.5 , 44 , 82.5 , 150 , 250			
	Turbo mode	40, 90 , 180 , 350 , 660 , 1200 , 2000			
Input reference noise		Please refer to the noise performance section.			
INL Integral nonlinearity	Gain = 1 to 128 , VCM = 0.5 AVDD , optimal condition (2)		20		ppm FSR
V_{IO} Input offset voltage)	PGA disabled, gain = 1 to 4, differential input.		±2		μ V
	Gain = 2 to 128, differential input		±2		
Offset Drift	PGA disabled, gain = 1 to 4		0.1	0.3	μ V/°C
	Gain = 1 to 128 , T_A = -40°C to +85°C (2)		0.1	0.3	
	Gain = 1 to 128		0.3	0.5	
Gain error	PGA disabled, gain = 1 to 4		0.2		
	Gain = 1 to 128, T_A = 25°C	-0.5	± 0.2	0.5	
Gain drift	PGA disabled, gain = 1 to 4		5		ppm/°C
	Gain = 1 to 128 (2)		5	20	
NMRR Normative suppression ratio (2)	50Hz 3%, DR = 20SPS, external CLK, 50/60 bits = 10	105			dB
	60Hz ±3%, DR = 20SPS, external CLK, 50/60 bits = 11	105			
	50Hz or 60Hz ±3%, DR=20SPS external CLK, 50/60 bits = 01	90			
CMRR Common-mode rejection ratio	Gain under DC conditions = 1	90	97		dB
	$f_{(CM)}$ = 50Hz, DR = 2000SPS (2)		116		
	$f_{(CM)}$ = 60Hz, DR = 2000SPS (2)		116		
PSRR Power supply rejection ratio	Under DC conditions, AVDD, Vcm = 0.5 AVDD, gain = 1	80	105		dB
	DVDD under DC conditions, Vcm = 0.5 AVDD, gain = 1 (2)	100	115		
Internal reference benchmark					
Initial accuracy	T_A = 25℃		2.048		V
Reference drift (2)	-45°C to 125°C		3	30	ppm/°C
Voltage reference input					
Reference input current	REFP0 = V_{ref}, REFN0 = AVSS		180		nA
Internal oscillator					
Internal oscillator accuracy	Normal mode	- 1	±0.6	2	%

(1) PGA Disabled indicates low noise PGA Power was lost and bypassed. Gain values are still supported in this situation. 1 , 2 and 4.
(2) Minimum and maximum values are ensured through design and characteristic analysis data.
(3) An internal voltage reference has been selected, the internal oscillator is enabled, IDAC is disabled, and the system is in continuous conversion mode. When an external reference is selected, the analog supply current typically increases by 70μA (normal mode, Turbo mode). When IDAC is enabled, the analog supply current typically increases by 190μA (excluding actual IDAC current).

Electrical Characteristics (continued)

Minimum and maximum specification values apply to a temperature range of T_A =–40 °C to +125°C. Typical specification values were determined at T_A =25°C. All specification values were determined with AVDD = 3.3V, AVSS = 0V, DVDD = 3.3V, PGA enabled, DR = 20SPS, and external V_{ref}= 2.5V (unless otherwise noted).

Parameter	Test Condition	Min	Typ	Max	Unit
Excitation Current Source (IDAC)					
Current setting		50, 100, 250, 500, 1000, 1500			µ A
Compliant voltage	All current settings			AVDD – 0.9	V
Accuracy	All current settings, per IDAC	- 3%	±1%	3%	
Current matching	Invalid for 10 µA settings		±0.3%		
Temperature drift	Each IDAC (invalid for 10 µA settings)		150		ppm/℃
Temperature drift matching	Invalid for 10 µA settings		20		ppm/℃
Temperature Sensor					
Convert resolution			14		Bits
Temperature resolution			0.03215		℃
Accuracy	T_A = 0°C to +75°C		±0.5		℃
	T_A = -40°C to +125°C		±0.1		
Relationship between accuracy and analog power supply voltage			0.1		℃/V
Low-Side Power Switch					
R_{ON} On resistance			3		Ω
Current flowing through the switch				30	mA
Digital Input/Output					
V_{IH} High-level input voltage		0.7 DVDD		DVDD	V
V_{IL} Low-level input voltage		DGND		0.3 DVDD	V
V_{OH} High-level output voltage	I_{OH} =3mA	0.8 DVDD			V
V_{OL} Low-level output voltage	I_{OL} = 3mA			0.2 DVDD	V
I_H Input leakage current, high level	V_{IH} = 5.5V	-10		10	µ A
I_L Input leakage current, low level	V_{IL} = DGND	-10		10	µ A
Power Supply					
I_{AVDD} Analog power supply current (3)	Power-off mode		0.05		µ A
	Duty cycle mode, PGA disabled		135		
	Duty cycle mode, gain = 1 to 16		160		
	Duty cycle mode, gain = 32		172		
	Duty cycle mode, gain = 64, 128		182		
	Normal mode, PGA disabled		342		
	Normal mode, gain = 1~16		448		
	Normal mode, gain = 32		499		
	Normal mode, gain = 64, 128		550		
	Turbo mode, PGA disabled		402		
	Turbo mode, gain = 1~16		613		
	Turbo mode, gain = 32		715		
	Turbo mode, gain = 64, 128		817		
I_{DVDD} Digital power supply current (3)	Power-off mode		1.3		µ A
	Duty cycle mode		44		
	Normal mode		43		
	Turbo mode		73		

P_D Power consumption (3)	Duty cycle mode, PGA disabled		0.5907		mW
	Normal mode, gain = 1~16		1.6203		
	Turbo mode, gain = 1 ~ 16		2.2638		

SPI Timing Requirements

Within the operating ambient temperature range, DVDD = 2.3V to 5.5V (unless otherwise specified).

		Min	Max	Unit
$t_{d(CSSC)}$ delay time, $\overline{CS}$ from falling edge to the first SCLK rising edge (1)		50		ns
$t_{d(SCCS)}$ delay time, finally SCLK falling edge to $\overline{CS}$ rising edge		25		ns
$t_{w(CSH)}$ pulse duration, $\overline{CS}$ is high level		50		ns
$t_{c(SC)}$	SCLK cycle	150		ns
$t_{w(SCH)}$	Pulse duration, SCLK is high level	60		ns
$t_{w(SCL)}$	Pulse duration, SCLK is low.	60		ns
$t_{su(DI)}$	Setup time: DIN is valid before the falling edge of SCLK.	50		ns
$t_{h(DI)}$	Hold time: DIN is valid after the falling edge of SCLK.	25		ns
SPI timeout (2)	Normal mode, duty cycle mode		13955	$t_{(MOD)}$
	Turbo mode		27910	

(1) When not sharing the bus with any other device, $\overline{CS}$ can be permanently connected to a low voltage level.

(2) For more information, please refer to the SPI timeout section. $t_{(MOD)} = 1/f_{(MOD)}$. When using the internal oscillator or a 4.096MHz external clock. Modulator frequency $f_{(MOD)}$ = 256kHz (Normal mode, duty cycle mode) and 512kHz (Turbo mode).

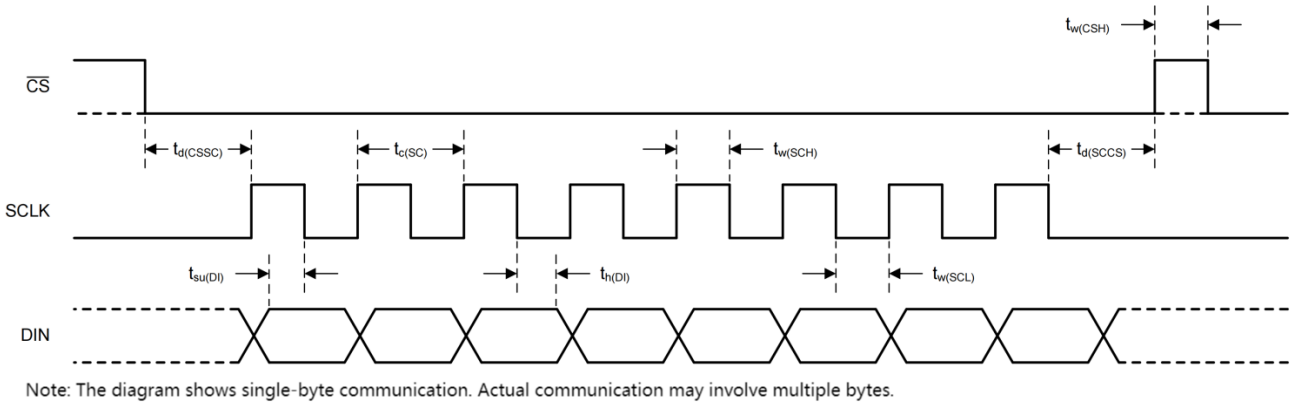
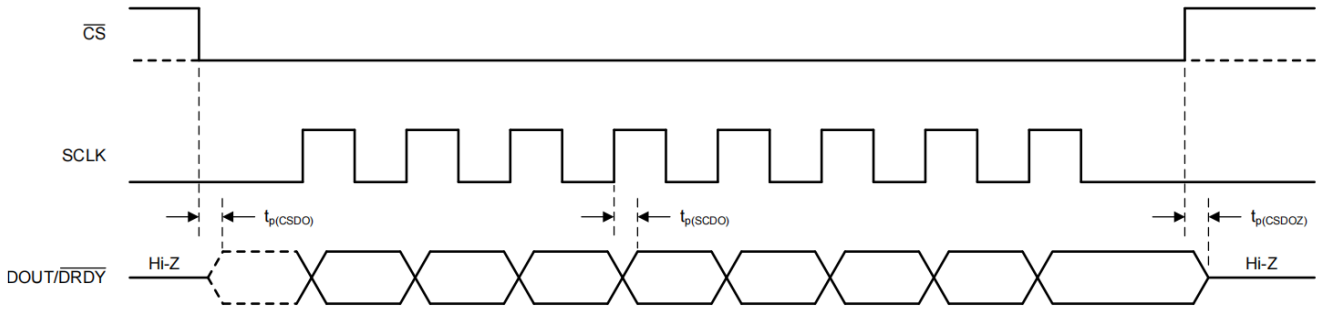


Figure 1. Serial interface timing requirements

SPI Switching Characteristics

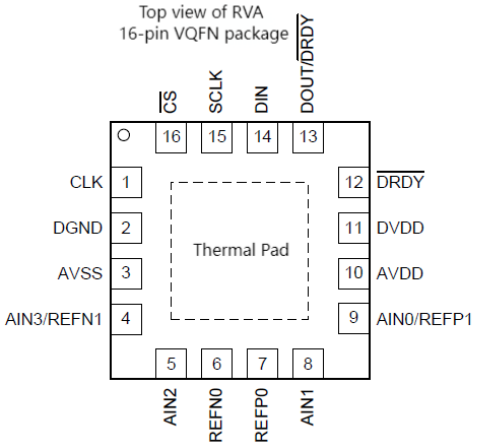
Within the operating ambient temperature range, DVDD = 2.3V to 5.5V (unless otherwise specified).

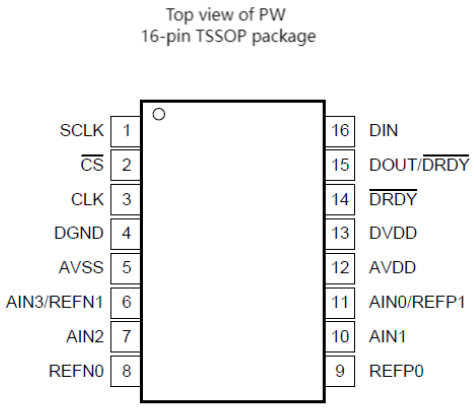
Parameter	Test conditions	Min	Typ	Max	Unit
tp (CSDO) propagation delay time, $\overline{CS}$ falling edge to DOUT drive	DOUT load = 20pF ‖ 10kΩ, and connected to DGND			50	ns
tp (SCDO) propagation delay time, $\overline{CS}$ rising edge to new valid DOUT	DOUT load = 20pF ‖ 10kΩ, and connected to DGND	0		25	ns
tp (CSDOZ) is the propagation delay time, $\overline{CS}$ with the rising edge reaching high impedance at DOUT	DOUT load = 20pF ‖ 10kΩ, and connected to DGND			50	ns



Note: The diagram shows single-byte communication. Actual communication may involve multiple bytes.

Figure 2. Characteristics of serial interface switch





Pin Function Table

Pin name	PIN No.		Function	Description
	RVA	PW		
AIN0/REFP1	9	11	Analog Input	Analog input 0 , positive reference input 1
AIN1	8	10	Analog Input	Analog input 1
AIN2	5	7	Analog Input	Analog input 2
AIN3/REFN1	4	6	Analog Input	Analog input 3, negative reference input 1. An internal low-side power switch is connected between AIN3/REFN1 and AVSS.
AVDD	10	12	Analog	Positive analog power supply
AVSS	3	5	Analog	Negative analog power supply
CLK	1	3	Digital input	External clock source pin. If this pin is not used, connect it to DGND.
$\overline{CS}$	16	2	Digital input	Chip select; active low. If not used, connect to DGND.
DGND	2	4	Digital	Digital grounding
DIN	14	16	Digital input	Serial data input
DOUT/$\overline{DRDY}$	13	15	Digital output	Serial data output in conjunction with data ready; active low.
$\overline{DRDY}$	12	14	Digital output	Data is ready, active low. If this pin is not used, leave it disconnected, or connect it to the DVDD via a weak pull-up resistor.
DVDD	11	13	Digital	Positive digital power supply
REFN0	6	8	Analog Input	Negative reference input 0
REFP0	7	9	Analog Input	Positive reference input 0
SCLK	15	1	Digital input	Serial clock input
Thermal pads		—	—	Thermal PowerPAD. Do not connect this pin, or connect it only to AVSS .

Noise Performance

A delta - sigma analog-to-digital converter (ADC) is based on the oversampling principle. The input signal to a delta - sigma ADC is sampled at a high frequency (modulator frequency), then filtered and decimated in the digital domain to generate a conversion result at the corresponding output data transfer rate. The ratio of the modulator frequency to the output data transfer rate is called the oversampling rate (OSR). By increasing the OSR and decreasing the output data transfer rate, the noise performance of the ADC can be optimized. That is, when the output data transfer rate decreases, obtaining a conversion result requires averaging more samples from the internal modulator, thus reducing the input reference noise. Increasing the gain also reduces the input reference noise, which is very effective when measuring low-amplitude signals.

ENOB=ln(Full-Scale Range/$V_{RMS\text{-}Noise}$)/ln(2)； Noise-Free Bits=ln(Full-Scale Range/ $_{VPP\text{-}Noise}$)/ln(2)； Full-Scale Range=2 · V_{ref} / Gain

ENOB (noise-free bit) conditions derived from root mean square (RMS) noise: A VDD=DVDD=3.3V, AVSS=0V, internal reference voltage=2.048V

Data transfer rate (SPS)	DADS1220 Gain (PGA Enabled, Normal Mode)							
	1	2	4	8	16	32	64	128
20	18.84 (16.51)	18.18 (16.32)	18.25 (15.86)	17.89 (16.15)	17.69 (15.86)	18.18 (16.32)	17.89 (15.86)	17.51 (15.62)
45	18.25 (16.15)	18.06 (16.15)	18.18 (16.15)	17.6 (15.42)	18.06 (15.86)	17.47 (15.42)	17.56 (15.42)	17.6 (15.23)
90	17.69 (15.62)	17.94 (15.86)	17.94 (15.86)	18(16)	17.43 (15.42)	17.79 (15.74)	17.4 (15.42)	16.25 (14.23)
175	17.79 (15.74)	17.64 (15.74)	17.51 (15.74)	17.43 (15.51)	17.4 (15.32)	17.18 (15.32)	16.69 (14.51)	16.2 (14.42)
330	17.89(16)	17.4(15)	17.03(15)	17.15(15)	17.51 (15.23)	16.71 (14.57)	16.12(14)	15.41 (13.51)
600	16.58 (14.74)	17.03 (15.15)	16.84 (14.74)	16.84 (15.15)	16.6 (14.74)	16.51 (14.74)	15.79 (13.93)	14.89 (12.91)
1000	16.49 (14.42)	16.27(14)	16.71(15)	16.15(14)	16.64(15)	16.1(14.42)	15.69 (13.42)	14.56 (12.66)
Data transfer rate (SPS)	**DADS1220 Gain (PGA Enabled, Turbo Mode)**							
	1	**2**	**4**	**8**	**16**	**32**	**64**	**128**
40	18 (15.74)	17.84 (15.86)	18.18 (16.15)	18.06 (16.15)	18.56 (16.51)	18.06 (16.32)	17.47 (15.42)	17.22 (15.42)
90	18.12(16)	17.84(16)	18.18 (15.86)	17.64 (15.86)	17.94 (15.74)	17.09 (15.07)	17(15)	16.47 (14.62)
180	18.06 (16.15)	17.51 (15.51)	17.6 (15.51)	17.32 (15.23)	17.29 (15.23)	17.47 (15.51)	16.94 (14.93)	16.01 (14.11)
350	17.43 (15.32)	17.32 (15.32)	17.43 (15.32)	17.56 (15.51)	17.06 (15.07)	16.94 (15.07)	16(13.8)	15.19 (13.07)
660	17.22 (15.23)	17.18 (15.23)	17.36 (15.62)	17.29(15)	17.36 (15.23)	16.36 (14.42)	15.84 (13.8)	15.07 (12 83)
1200	17.32 (15.15)	16.81 (14.74)	16.94 (15.15)	16.89 (14.74)	16.32 (14.42)	16.27 (14.15)	16.06 (14.15)	14.67 (12.55)
2000	16.49 (14.42)	16.43(15)	16.45 (14.42)	16.71(15)	16.18 (14.42)	16.04(14)	15.66 (13.68)	14.67 (12.66)

Data transfer rate (SPS)	DADS1220 Gain (PGA Off, Normal Mode)			Data transfer rate (SPS)	DADS1220 Gain (PGA Off, Turbo Mode)		
	1	2	4		1	2	4
20	18.06 (16.15)	18.06 (15.86)	17.56 (15.42)	20	17.69 (15.62)	17.89 (15.62)	18.25 (16.32)
45	17.89 (15.86)	18.25 (16.32)	17.64 (15.86)	45	18.32 (16.32)	17.94 (15.86)	17.94 (15.74)
90	17.89(16)	18.18 (16.51)	17.84 (15.51)	90	18.25 (16.15)	17.4 (15.51)	17.74 (15.74)
175	18.47 (16.51)	17.89 (15.86)	17.74 (15.51)	175	17.6 (15.51)	17.94 (15.74)	17.84 (15.86)
330	17.6 (15.62)	17.43 (15.62)	17.22 (15.23)	330	17.47 (15.62)	17.32 (15.62)	17.29 (15.23)
600	17.03 (14.74)	17(15.15)	17.29 (15.15)	600	16.74 (14.74)	17.32 (15.74)	17.18 (15.74)
1000	16.42 (14.42)	16.54(15)	17.18(15)	1000	16.64 (14.42)	16.67(15)	17(16)

The ENOB (noise-free bit) conditions derived from root mean square (RMS) noise are: A VDD = DVDD = 3.3V, AVSS = 0V, and the external reference voltage is 2.048V.

Data transfer rate (SPS)	DADS1220 Gain (PGA Enabled, Normal Mode)							
	1	2	4	8	16	32	64	128
20	20.06 (18.32)	19.47 (17.32)	19.06 (17.32)	19.18 (17.32)	19,47(17.32)	19.06(17)	18.64 (16.32)	17.79 (15.62)
45	19.84 (17.74)	19.64 (17.74)	19.06(17)	18.4 (16.74)	19.32(17)	18.84 (16.74)	18.32 (16.32)	17.47 (15.42)
90	19.64 (17.32)	19.18 (17.32)	18.32(17)	18.56 (16.51)	18.56 (16.15)	18.12 (16.15)	17.32 (15.07)	16.49 (14.42)
175	18.94(17)	18.84(17)	18.64(17)	18.94(17)	18.18 (16.15)	17.79 (15.86)	17.03 (15.15)	15.97 (14.11)
330	18.74 (17.74)	18.4 (16.51)	18.12(16)	17.89(16)	17.64 (15.62)	17.06(15)	16.34 (14.11)	15.5 (13.42)
600	18.12 (15.74)	17.94 (16.74)	17.74 (16.74)	17.15 (15.15)	17.22 (15.15)	16.64 (14.42)	16.58 (14.42)	15.07 (13.13)
1000	17.06(16)	17.03(16)	17.51(15)	16.84(15)	16.79(15)	16.6 (14.42)	15.49 (13.42)	14.79 (12.66)
Data transfer rate (SPS)	**DADS1220 Gain (PGA Enabled, Turbo Mode)**							
	1	**2**	**4**	**8**	**16**	**32**	**64**	**128**
40	19.47 (17.32)	19.84 (17.74)	19.32 (17.32)	19.06 (17.32)	18.64 (16.74)	19.32 (17.32)	18.4 (16.32)	17.6 (15.32)
90	19.64 (17.74)	19.47 (17.32)	19.32 (17.74)	19.06(17)	18.4 (16.32)	18.18 (15.86)	17.6 (15.62)	16.49 (14.51)
180	19.47(17)	19.47 (17.32)	18.94 (16.74)	18.94(17)	18.56 (16.51)	17.94 (15.74)	17(14.8)	15.99 (13.9)
350	19.06 (17.74)	19.06(17)	18.94 (17.74)	18.06 (16.15)	18.06 (15.86)	17.29 (15.15)	16.43 (14.51)	15.52 (13.65)
660	18.47 (16.51)	18.4(16)	18.32(16)	18.06(16)	17.89 (15.62)	16.92(15)	16.03(14)	15.03 (13.13)
1200	17.79 (16.74)	17.74 (16.74)	17.64 (15.74)	17.22 (15.15)	17.03 (15.15)	16.49 (14.42)	15.59 (13.39)	14.66 (12.64)
2000	18.06(16)	17(16)	17(15)	16.86(15)	17.09(15)	16.22(14)	15.51 (13.68)	14.63 (12.66)

Data transfer rate (SPS)	DADS1220 Gain (PGA Off, Normal Mode)			Data transfer rate (SPS)	DADS1220 Gain (PGA Off, Turbo Mode)		
	1	2	4		1	2	4
20	19.84 (18.32)	20.06 (17.74)	19.64 (17.32)	20	2.06 (17.74)	19.47 (17.32)	19.64 (17.74)
45	19.64 (17.32)	19.32 (17.32)	20.06 (17.74)	45	19.32 (17.32)	19.64 (17.32)	19.32(17)
90	19.18(17)	19.06 (17.32)	19.18(17)	90	19.47 (17.32)	19.47 (17.74)	19.64 (17.74)
175	19.32 (17.74)	18.64 (16.51)	19.18(17)	175	19.06(17)	18.94(17)	18.84(17)
330	18.18(16)	18.25 (16.51)	18.12 (16.51)	330	18.25 (16.51)	18.4 (16.51)	18.4 (16.51)
600	17.64 (15.74)	17.79 (15.74)	17.79 (16.74)	600	17.74 (15.74)	18 (15.74)	17.74 (16.74)
1000	17.69(15)	17.79(16)	18.47(16)	1000	17.43(16)	17.03(15)	17.6(16)

The ENOB (noise-free bit) conditions derived from root mean square (RMS) noise are: A VDD = DVDD = 3.3V, AVSS = 0V, and the reference voltage = 2.048V.

Data transfer rate (SPS)	DADS1120 Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
20	16(15)	16(15)	16(16)	16(16)	16(15)	16(15)	16(15)	16 (14.42)
45	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)
90	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)	16 (14.42)
175	16(15)	16(15)	16(15)	16(16)	16 (14.42)	16 (14.42)	16 (14.42)	15.86 (13.42)
330	16 (14.42)	16(15)	16 (14.42)	16(16)	16(15)	16 (14.42)	16 (14.42)	15.74 (13.19)
600	16(15)	16 (14.42)	16 (14.42)	16(15)	16 (14.42)	16(14)	16 (13.42)	15.32(13)
1000	16 (14.42)	16(15)	16(14)	16 (14.42)	16(14)	16(14)	16 (13.42)	15.07 (12.54)

Data transfer rate (SPS)	DADS1120, Noise (μVPP) Gain μVRMS (PGA Off)			Data transfer rate (SPS)	DADS1120, RMS noise ENOB gain (PGA off)		
	1	2	4		1	2	4
20	62.5(125)	31.25(125)	30(62.5)	20	16(15)	16(15)	16(16)
45	62.5(62.5)	31.25(125)	26.88 (62.5)	45	16(16)	16(15)	16(16)
90	62.5(125)	31.25 (62.5)	30.63(125)	90	16(15)	16(16)	16(15)
175	62.5(125)	31.25(125)	31.25 (62.5)	175	16(15)	16(15)	16(16)
330	62.5(125)	31.25(125)	32.5(125)	330	16(15)	16(15)	16(15)
600	62.5 (187.5)	38.13 (187.5)	32.5 (187.5)	600	16 (14.42)	16 (14.42)	16 (14.42)
1000	62.5 (187.5)	38.13 (187.5)	39.38 (187.5)	1000	16 (14.42)	16 (14.42)	16 (14.42)

Register Mapping

This device features four 8-bit configuration registers, accessible via a serial interface using the RREG and WREG commands. These configuration registers control the device's operating mode and can be switched at any time without data corruption. Upon power-up or reset, all registers are set to their default values (all 0). During power-down mode, all registers retain their values. The following table shows the register mapping for the configuration registers.

Configure Register Mapping

Register (hexadecimal)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00h	MUX[3:0]				GAIN[2:0]			PGA_BYPASS
01h	DR[2:0]			MODE[1:0]		CM	TS	BCS
02h	VREF[1:0]		50/60 [1:0]		PSW	IDAC[2:0]		
03h	I1MUX[2:0]			I2MUX[2:0]			DRDYM	0

Configuration Register 0 (Offset =00h) [Reset =00h]

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
MUX[3:0]				GAIN[2:0]			PGA_BYPASS
R/W-0h				R/W-0h			R/W-0h

LEGEND: R/W=Read/Write;-n=value after reset

Configuration Register 0 Field Description

Bit	Field	Type	Reset	Description
7:4	MUX[3:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. For the AINN=AVSS setting, the PGA must be disabled (PGA_BYPASS=1), and only gains of 1, 2, and 4 are available. 0000 : AINP=AIN0, AINN=AIN1(default) 0001 : AINP=AIN0, AINN=AIN2 0010 : AINP = AIN0, AINN = AIN3 0011 : AINP=AIN1, AINN=AIN2 0100 : AINP=AIN1, AINN=AIN3 0101 : AINP=AIN2, AINN=AIN3 0110 : AINP=AIN1, AINN=AIN0 0111 : AINP=AIN3, AINN=AIN2 1000 : AINP=AIN0, AINN=AIN2AVSS 1001 : AINP=AIN1, AINN=AVSS 1010 : AINP=AIN2, AINN=AVSS 1011 : AINP=AIN3, AINN=AVSS 1100 : ($V_{(REFPx)}$ –$V_{(REFNx)}$)/4 monitoring (bypass PG) 1101 : (AVDD–AVSS)/4 monitoring (bypass PGA) 1110 : Short AINP and AINN to (AVDD+AVSS)/2 1111 : Reserved
3:1	GAIN[2:0]	R/W	0h	**Gain Configuration** These bits are used to configure the device gain. Gains 1, 2, and 4 can be used without a PGA. In this case, the gain is obtained through a switched-capacitor structure. 000 : Gain = 1 (Default setting) 001 : Gain = 2 010 : Gain = 4 011 : Gain = 8 100 : Gain = 16 101 : Gain = 32 110 : Gain = 64 111 : Gain = 128
0	PGA_BYPASS	R/W	0h	**Disable and bypass internal low-noise PGA** Disabling the PGA reduces overall power consumption and extends the common-mode voltage range (VCM) to AVSS–0.1V to AVDD+0.1V. PGA can only be disabled for gains of 1, 2, and 4. Regardless of the PGA_BYPASS setting, PGA is always enabled for gain settings from 8 to 128. 0 : PGA is enabled (default setting) 1 : PGA has been disabled and bypassed

Configuration Register 1 (offset = 01h) [reset = 00h]

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DR [2:0]			MODE [1:0]		CM	TS	BCS
R/W-0h			R/W-0h		R/W-0h	R/W-0h	R/W-0h

Legend: R/W = Read/Write; -n = Value after reset

Configuration Register 1 Field Description

Bit	Field	Type	Reset	Description
7:5	DR[2:0]	R/W	0h	**Data rate** These bits control the data rate settings, depending on the selected operating mode. Table 1 lists the bit settings for Normal mode, Duty Cycle mode, and Turbo mode.
4:3	MODE[1:0]	R/W	0h	**Work mode** The operating modes of these bit control devices. 00 : Normal mode (256kHz modulator clock, default setting) 01 : Duty Cycle Mode (Internal Duty Cycle 1:4) 10 : Turbo Mode (512kHz modulator clock) 11 : Retain
2	CM	R/W	0h	**Switching modes** This bit is used to set the conversion mode for the device. 0 : Single-use mode (default setting) 1 : Continuous Conversion Mode
1	TS	R/W	0h	**Temperature sensor mode** This bit is used to enable the internal temperature sensor and to put the device into temperature sensor mode. When the temperature sensor mode is enabled, the settings of configuration register 0 will have no effect, and the device will use an internal reference for measurement. 0 : Disable temperature sensor (default setting) 1 : Enable temperature sensor
0	BCS	R/W	0h	**Burned out current source** This bit is used to control the 10 μA burnout current source. Burning out a current source can be used to detect sensor malfunctions (e.g., open circuits and short circuits). 0 : Current source off (default setting) 1 : Current source connected

Table 1. DR bit settings (1)

Normal mode	Duty cycle mode	TURBO model
000 = 20 SPS	000 = 5 SPS	000 = 40 SPS
001 = 45 SPS	001 = 11.25 SPS	001= 90 SPS
010 = 90 SPS	010 = 22.5 SPS	010 = 180 SPS
011 = 175 SPS	011 = 44 SPS	011 = 350 SPS
100 = 330 SPS	100 = 82.5 SPS	100 = 660 SPS
101 = 600 SPS	101 = 150 SPS	101 = 1200 SPS
110 = 1000SPS	110 = 250 SPS	110 = 2000 SPS
111 = Reserved	111 = Reserved	111 = Reserved

(1) The data rate provided is calculated using the internal oscillator or a 4.096MHz external clock. If an external clock with a frequency other than 4.096MHz is used, the data rate will be scaled proportionally to the external clock frequency.

Configuration Register 2 (offset = 02h) [reset =00h]

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VREF [1:0]		50/60[1:0]		PSW	IDAC [2:0]		
R/W-0h		R/W-0h		R/W-0h	R/W-0h		

Legend: R/W = Read/Write; -n = Value after reset

Configuration Register 2 Field Description

Bit	Fields	Type	Reset	Description
7:6	VREF [1:0]	R/W	0h	**Reference voltage selection** These bits are used to select the reference voltage source used for the conversion. 00: Select the 2.048V internal reference voltage (default setting) 01: Select the external reference voltage using dedicated REFP 0 and REFN 0 inputs. 10: Use AIN 0/ REFN 1 and AIN 3/ REFN 1 to select the external reference voltage 11: Analog power supply used as a reference (AVDD – AVSS)
5:4	50/60 [1:0]	R/W	0h	**FIR filter configuration** These bits are used to configure the filter coefficients for the internal FIR filter. In normal mode, these bits are used only with the 20 SPS setting; in duty cycle mode, these bits are used only with the 5 SPS setting. For all other data rates, these bits are set to 00 00: No 50 Hz or 60 Hz suppression (default setting) 01: Simultaneous suppression of 50 Hz and 60 Hz 10: Only suppresses 50 Hz 11: Only suppresses 60 Hz
3	PSW	R/W	0h	**Low-side power switch configuration** This bit is used to configure the behavior of the low-side switch connecting AIN 3/ REFN 1 and AVSS. 0: The switch is always off (default setting) 1: The switch will automatically close when the START/SYNC command is sent and automatically open when the POWERDOWN command is sent.
2:0	IDAC [2:0]	R/W	0h	**IDAC current setting** These bits are used to set the current for the IDAC 1 and IDAC 2 excitation current sources.
				000: Off (default setting) 001: Reserved 010: 50 µA 011: 100 µA 100: 250 µA 101: 500 µA 110: 1000 µA 111: 1500 µA

Configuration Register 3 (offset = 03h) [reset = 00h]

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
I1MUX[2:0]			I2MUX[2:0]			DRDYM	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

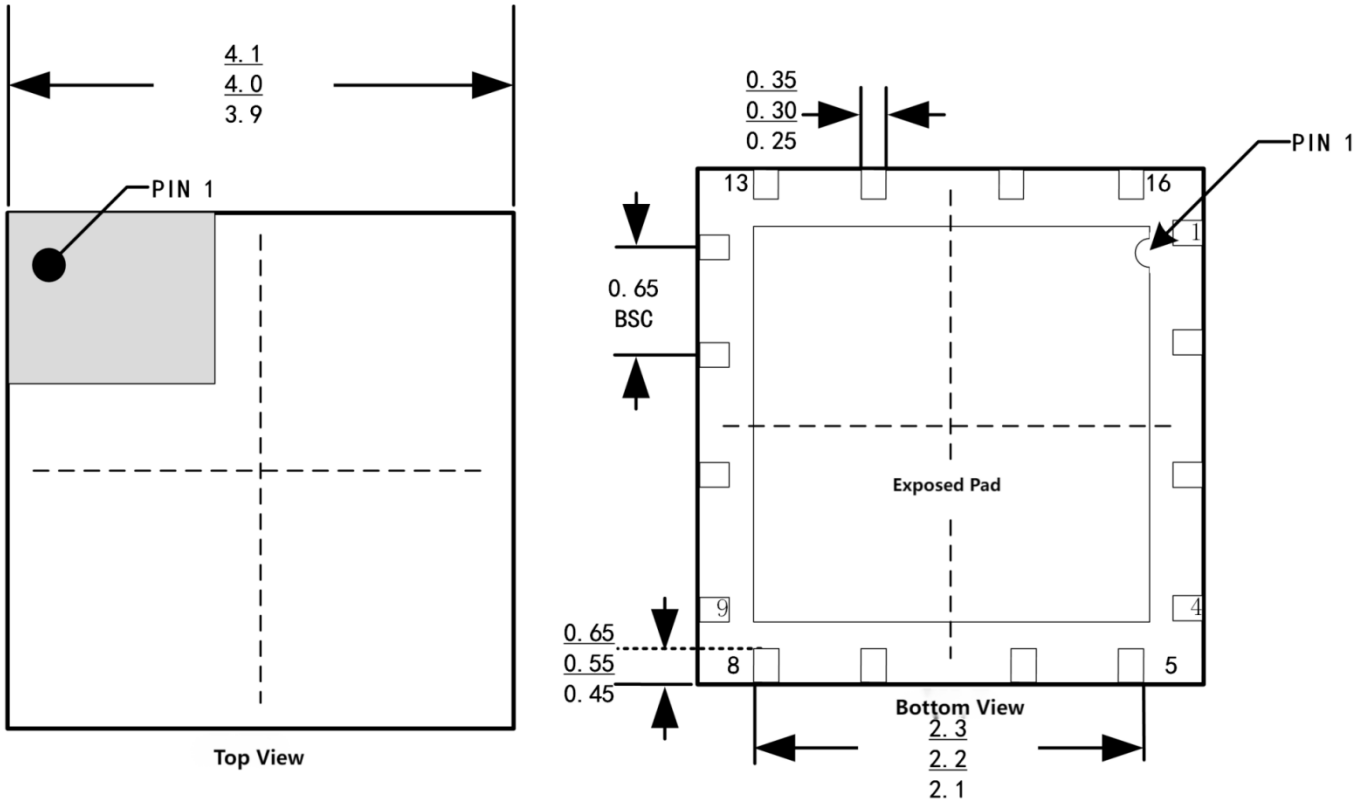
Legend: R/W = Read/Write; -n = Value after reset

Configuration Register 3 Field Description

Bit	Fields	Type	Reset	Description
7:5	I1MUX[2:0]	R/W	0h	**IDAC1 Router Configuration** These bits are used to select the channel that IDAC1 will route to. 000 : IDAC1 is disabled (default setting) 001 : IDAC1 is connected to AIN0/REFP1 010 : IDAC1 is connected to AIN1 011 : IDAC1 is connected to AIN2 100 : IDAC1 is connected to AIN3/REFN1 101 : IDAC1 is connected to REFP0 110 : IDAC1 is connected to REFN0 111 : Reserved
4:2	I2MUX[2:0]	R/W	0h	**IDAC2 Router Configuration** These bits are used to select the channel that IDAC2 will route to. 000 : IDAC2 is disabled (default setting) 001 : IDAC2 is connected to AIN0/REFP1 010 : IDAC2 is connected to AIN1 011 : IDAC2 is connected to AIN2 100 : IDAC2 is connected to AIN3/REFN1 101 : IDAC2 is connected to REFP0 110 : IDAC2 is connected to REFN0 111 : Reserved
1	DRDYM	R/W	0h	**DRDY mode** This bit controls the behavior of the DOUT/DRDY pin when new data is ready. 0 : Only the DRDY pin is used to indicate when data is ready (default setting). 1 : Simultaneously indicate data readiness via DOUT/DRDY and DRDY.
0	Reserved	R/W	0h	**Reserved** Always write as 0

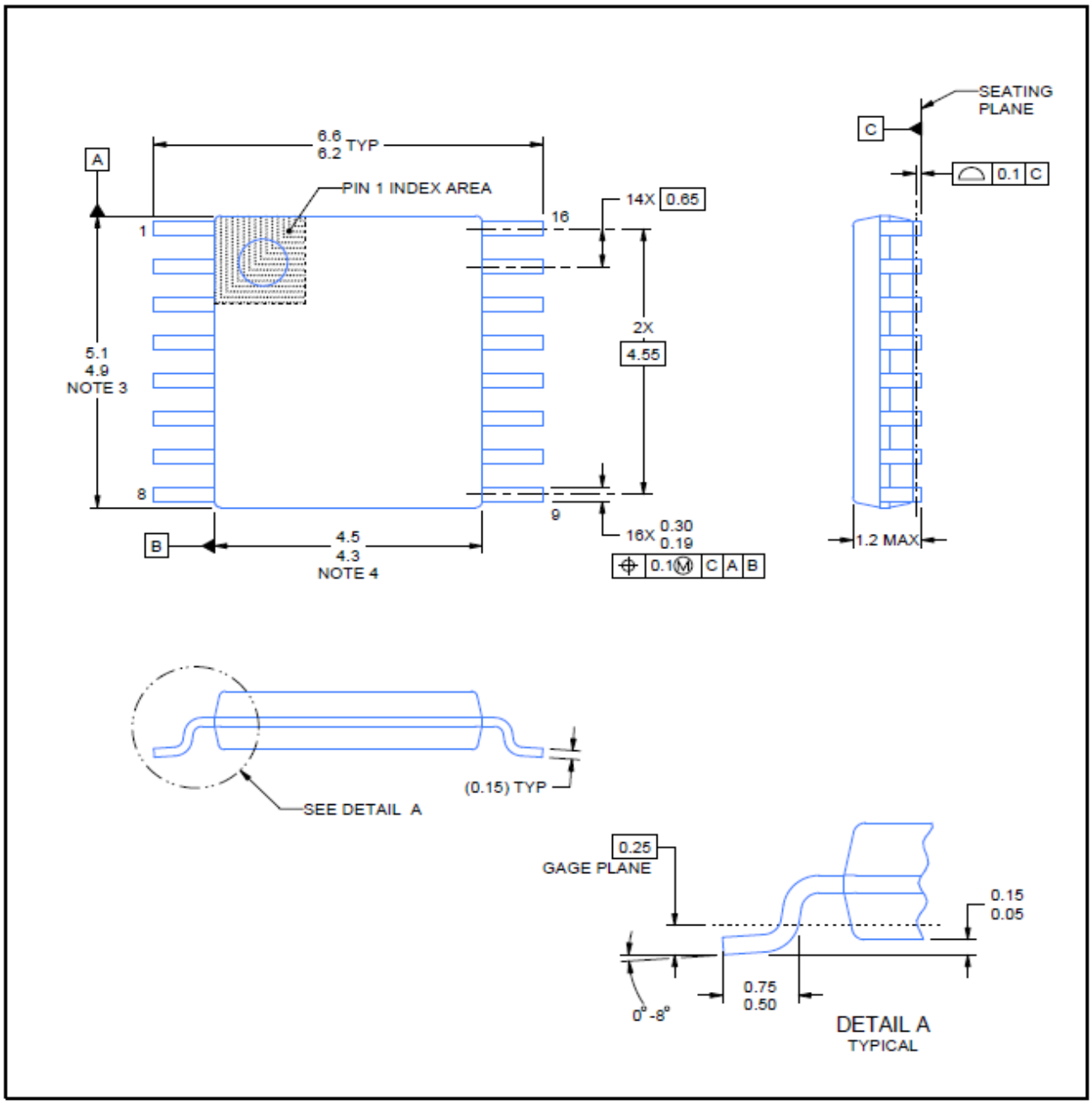
Outline Dimensions and Packaging

QFN16L package



Outline Dimensions and Packaging

TSSOP-16 package



Device Ordering Information List

Product Model	Temperature Range	Packaging Type	Package Quantity	RoHS
DADS1220QF	- 40°C to +125°C	QFN-16L	1,000/reel	Y
DADS1220TSP	- 40°C to +125°C	TSSOP-16	1,000/reel	Y
DADS1120QF	- 40°C to +125°C	VQF-16L	1,000/reel	Y
DADS1120TSP	- 40°C to +125°C	TSSOP-16	1,000/reel	Y