1. Features

- Wide power supply voltage: 2.5V to 5.5V
- Low current consumption: 150μA (continuous conversion mode)
- Programmable data transfer rates: 8SPS to 860SPS
- Single-cycle stability
- Internal low-drift voltage reference
- Internal oscillator
- Internal programmable gain amplifier
- SPI interface
- Four single-ended or two differential inputs
- Operating temperature range: -40°C to +125°C
- MSOP-10 package (3.00mm × 3.00mm)

2. Applications

- Portable instrument
- Battery voltage and current monitoring
- Temperature measurement system
- Consumer electronics
- Industrial automation and process control

3. Overview

DADS1118 is an I²C-compliant 16-bit high-precision, low-power analog-to-digital converter (ADC) in an MSOP-10 package. It features a low-drift voltage reference and oscillator. The DADS1118 also incorporates a programmable gain amplifier (PGA) and a digital comparator. These features, along with a wide operating supply voltage range, make the DADS1118 ideal for power- and space-constrained sensor measurement applications. The DADS1118 can perform conversions at data rates up to 860 samples per second (SPS). The PGA provides an input range from ±256mV to ±6.144V, enabling accurate measurements of both large and small signals. The DADS1118 features a single input multiplexer (MUX) for two differential input measurements or four single-ended input measurements. Undervoltage and overvoltage detection can be performed using digital comparators within the DADS1118. The DADS1118 can operate in both continuous conversion and single- shot modes. In single -use mode, these devices can automatically power off after a single conversion; thus significantly reducing power consumption during idle periods.

4. Device Packaging Information

Product Model	Packaging Type	Package Size
DADS1118	MSOP-10	3mm × 3mm

5. Functional Block Diagram

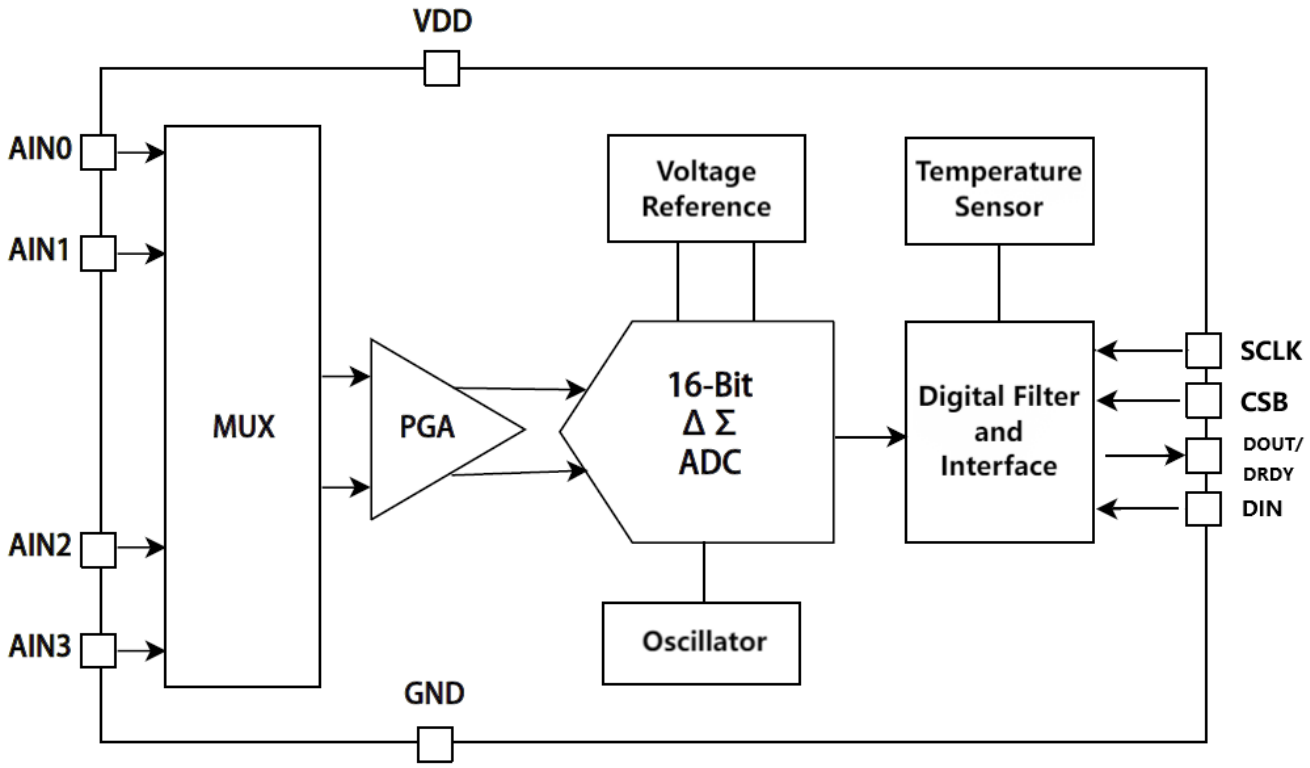

Figure 1. Functional Block Diagram

6. Pin Configuration and Functions

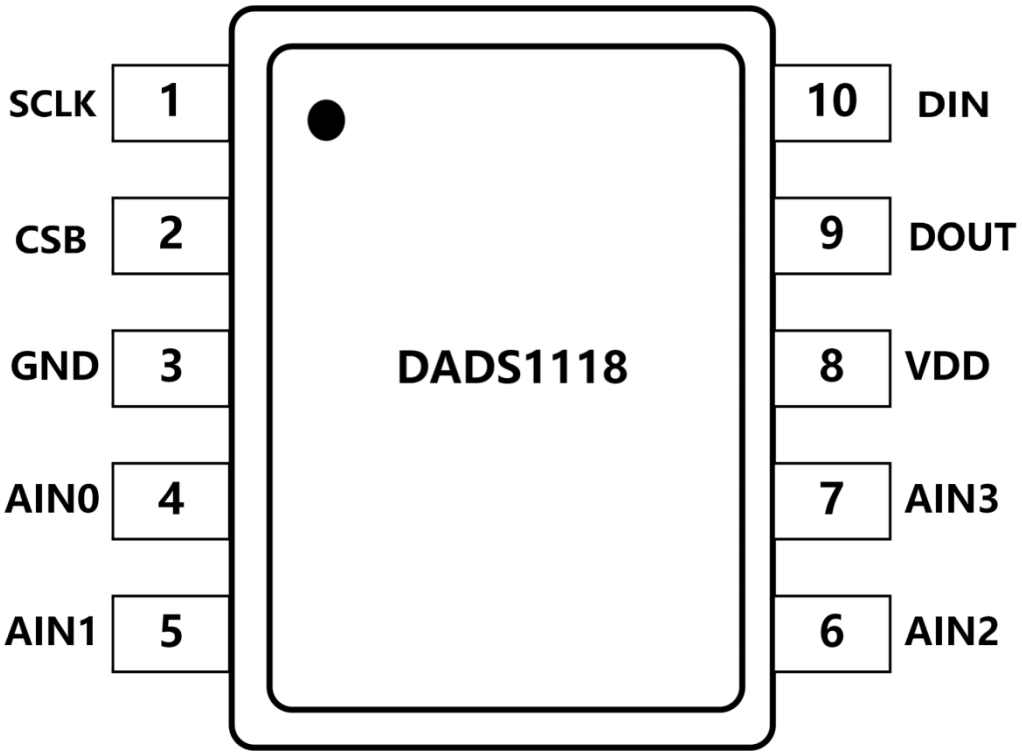

Figure 2. Pin Configuration

Pin Functions

Pin number	Symbol	Function
1	SCLK	SPI serial clock input
2	CSB	SPI chip select signal input
3	GND	Ground
4	AIN0	Analog input 0
5	AIN1	Analog input 1
6	AIN2	Analog input 2
7	AIN3	Analog input 3
8	VDD	Power supply
9	DOUT	The SPI serial data output can also be used as a DRDY indicator
10	DIN	SPI serial data input

7. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Temperature			
Operating temperature (T_A)	- 40	125	℃
Storage temperature (T_J)	- 40	150	℃
Junction temperature (T_{stg})	- 60	150	℃
Pressure resistance			
VDD	- 0.3	7	V
Analog Input	GND - 0.3	VDD + 0.3	V
Digital input	GND - 0.3	5.5	V
Current limiting			
Input current	- 10	1 0	mA
ESD			
HBM	4,000		V
CDM	1,000		V

Exceeding the listed absolute maximum ratings may cause permanent damage to the equipment. These are only pressure ratings and do not imply that the equipment will function properly under any conditions exceeding the recommended operating conditions. Prolonged exposure to absolute maximum ratings may affect the reliability of the equipment.

8. Electrical Characteristics

Under the conditions of VDD=3.3V, data rate=8SPS, and full-scale input voltage range (FSR)=±2.048V (unless otherwise specified). Maximum and minimum specifications apply to a temperature range of TA=-40°C to +125°C. Typical specifications apply to T_A = 25°C.

Parameter	Test conditions	Max	Typ	Min	Unit
Analog Input					
Common-mode input impedance	FSR = ±6.144V		22		MΩ
	FSR = ±4.096V, FSR = ±2.048V		16, 11.5		
	FSR = ±1.024V		23		
	FSR = ±0.512V, FSR = ±0.256V		26.6		
Differential input impedance	FSR = ±6.144V		16		MΩ
	FSR = ±4.096V		14		
	FSR = ±2.048V		6.8		
	FSR = ±1.024V		1.7		
	FSR = ±0.512V, ±0.256V		760, 520		kΩ
System performance					
Resolution (no missing bits)		16			Bits
Data rate		8, 16, 32, 64, 128, 250, 475, 860			SPS
Data rate error	All data rates	-10%		10%	
Output noise		See the noise performance section.			
INL Integral Nonlinearity	DR=8SPS, FSR=±2.048V			1	L SB
Offset error	FSR = ±2.048V, differential input	-3	±1	3	LSB
	FSR = ±2.048V, single-ended input		±3		LSB
Temperature drift offset	FSR = ±2.048V		0.005		LSB/°C
Long-term temperature drift	FSR=±2.048V, T_A =125°C,1000hrs		±1		LSB
Offset power supply suppression	FSR = ±2.048V, DC power supply variation		1		LSB/V
Offset matching	Matching between any two inputs		3		LSB
Gain error	FSR = ±2.048V, T_A = 25°C		0.02 %	0.15%	
Gain Temperature Drift	FSR = ±0.256V		7		ppm/°C
	FSR = ±2.048V		5	40	
	FSR = ±6.144V		5		
Long-term gain drift	FSR=±2.048V, T_A =125°C,1000hrs		±0.05		%
Gain power supply rejection			140		ppm/V
Gain Matching	Matching between any two gains		0.06 %	0.1 %	
Gain Channel Matching	Matching between any two channels		0.05 %	0.1 %	
Common-mode rejection ratio	At DC, FSR = ±0.256V		90		dB
	At DC, FSR = ±2.048V		100		
	At DC, FSR = ±6.144V		98		
	f_{CM} = 60Hz, DR = 8SPS		95		
	f_{CM} = 50Hz, DR = 8SPS		115		
Data Input/Output					
V_{IH}		0.7VDD		5.5	V
V_{IL}		GND		0.3VDD	V
V_{OL}	I_{OL} = 3mA	GND	0.15	0.3VDD	V
Input leakage current	GND < V_{DIG} < VDD	- 10		1 0	μA
Power supply					
I_{VDD} operating current	Power off mode, T_A = 25°C		0.5	2	μA
	Operating mode, T_A = 25°C		165	210	μA
P_D power consumption	VDD=5.0V		0.96		mW
	VDD=3.3V		0.6		mW

9. Timing Specifications

Beyond the operating ambient temperature range, VDD = 2.0V to 5.5V (unless otherwise specified) .

Parameter	Description	Quick Mode		Unit
		Min	Max	
t_{CSSC}	Delay time: from the falling edge of CS to the first rising edge of SCLK	100		ns
t_{SCCS}	Delay time: from the last falling edge of SCLK to the rising edge of CS			ns
t_{CSH}	CS high level duration			ns
t_{SCLK}	SCLK cycle			ns
t_{SPWH}	SCLK high level time			ns
t_{SPWL}	SCLK low level time			ns
t_{DIST}	Configure timing; DIN is valid before the falling edge of SCLK			ns
t_{DIHD}	Hold time, DIN is valid after the falling edge of SCLK			ns
t_{DOHD}	Hold time, invalid from the rising edge of SCLK to DOUT			ns

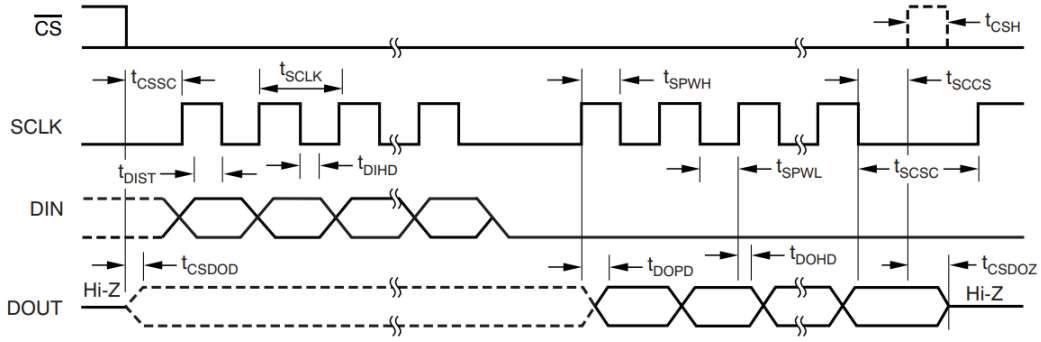

Figure 3. SPI Interface Timing

10. Working Principle

- **Overview**

The DADS1118 is a low-power 16-bit ΔΣ ADC that integrates a voltage reference, oscillator, programmable gain amplifier, and programmable digital comparator. The DADS1118 ADC core measures the differential signal V_{IN}, which is the difference between V_{AINP} and V_{AINN}. The converter core consists of a differential switched-capacitor ΔΣ modulator and a digital filter. This architecture results in very strong attenuation of any common-mode signal. The input signal is compared to an internal reference voltage. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage. The DADS1118 offers two available conversion modes: single-trigger conversion and continuous conversion. In single-trigger mode, the ADC performs a single conversion on the input signal upon request, stores the converted value in the internal conversion register, and then enters a power-off state. This mode is designed to provide significant energy savings for systems that require only periodic conversions or have long idle periods between conversions. In continuous conversion mode, the ADC automatically begins converting the input signal once the previous conversion is complete. The continuous conversion rate is equal to the programmed data rate. Data can be read at any time and always reflects the most recently completed conversion.

- **Multiplexer**

The DADS1118 has a built-in multiplexer that selects one of eight channels (four single-ended inputs and four differential inputs) as input for conversion through different configurations of the MUX[2:0] registers. When a single-ended signal is measured, the negative input of the ADC is connected to GND via a switch on the MUX. Refer to the description of MUX[2:0] in the register table for specific configuration information.

- **FSR and LSB**

The FSR is configured by the Config register PGA[2:0], and the LSBs corresponding to each range are as follows:

FSR	LSB
±6.144V	187.5μV
±4.096V	125μV
±2.048V	62.5μV
±1.024V	31.25μV
±0.512V	15.625μV
±0.256V	7.8125μV

The analog input voltage must not exceed the analog input voltage given in the absolute maximum rating. Therefore, when FSR>VDD+0.3V, the input will be clamped at VDD+0.3V, and the portion exceeding this voltage cannot be measured.

- **Reference voltage**

The DADS1118 integrates a low-temperature drift voltage reference, which only provides an internal voltage reference and cannot be output externally.

- **Oscillator**

The DADS1118 has a built-in 1MHz oscillator, and the chip's output data rate is proportional to the internal clock frequency.

- **Temperature sensor**

The DADS1118 integrates a high-precision temperature sensor. Temperature sensor mode is enabled by setting the TS_MODE bit in the configuration register to 1. Temperature data is presented as a 14-bit result, left-aligned in the 16-bit conversion result. Data output begins with the most significant byte (MSB), and when reading two data bytes, the first 14 bits represent the temperature measurement result. Each 14-bit least significant bit (LSB) corresponds to 0.03125°C. Negative numbers are represented in two's complement format, as shown in the table below.

Temperature (°C)	Digital output (two's complement)	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	FFFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001
0	00 0000 0000 0000	0000
-0.25	11 1111 1111 1000	3FF8
-25	11 1100 1110 0000	3CE0
-40	11 1011 0000 0000	3B00

- **Noise performance**

Δ-Σ ADCs are based on the oversampling principle, where the input signal is sampled at a high frequency, followed by filtering and extraction. The ratio of the sampling frequency to the output data rate is called the oversampling ratio (OSR). By increasing the oversampling ratio, the noise performance of the ADC can be optimized, which is very useful when measuring small signals.

Table 1. Root mean square and peak-to-peak noise (μVrms, μVpp) at VDD= 3.3V

Data Rate	FSR (Full Scale Range)					
(SPS)	±6.144V	±4.096V	±2.048V	±1.024V	±0.512V	±0.256V
8	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
1 6	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
3 2	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
6 4	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
1 28	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (12.35)
2 50	187.5 (252.09)	125 (148.28)	62.5 (84.03)	31.25 (39.54)	15.62 (16.06)	7.81 (18.53)
4 75	187.5 (266.92)	125 (227.38)	62.5 (79.08)	31.25 (56.84)	15.62 (32.13)	7.81 (25.95)
8 60	187.5 (430.06)	125 (266.93)	62.5 (118.63)	31.25 (64.26)	15.62 (40.78)	7.81 (35.83)

Table 2. Effective resolution and noise-free resolution at VDD=3.3V

Data Rate	FSR (Full Scale Range)					
(SPS)	±6.144V	±4.096V	±2.048V	±1.024V	±0.512V	±0.256V
8	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
1 6	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
3 2	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
6 4	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
1 28	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.33)
2 50	16 (15.57)	16 (15.75)	16 (15.57)	16 (15.66)	16 (15.96)	16 (14.75)
4 75	16 (15.49)	16 (15.13)	16 (15.66)	16 (15.13)	16 (14.95)	16 (14.26)
8 60	16 (14.8)	16 (14.9)	16 (15.07)	16 (14.95)	16 (14.61)	16 (13.8)

11. Data Format

The DADS1118 provides 16-bit binary data, and Table 4 summarizes the ideal output code values for different input signals.

Table 4. Output Codewords

Input	Output
≥+FS(2^{15}-1)/2^{15}	7FFFh
+FS/2^{15}	0001h
0	0000h
-FS/2^{15}	FFFFh
≤-FS	8000h

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12. Registers

Conversion Register [Reset = 0000h]

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R	0000h	16- bit conversion result

The 16-bit conversion register stores the result of the previous conversion, represented in two's complement format. Upon power-on, the conversion register is cleared to 0 and remains at 0 until the first conversion is complete.

Configuration Register [Reset = 058 Bh]

Bit	Field	Type	Reset	Description
15	SS	R/W	1h	When writing: writing 0 has no effect in any state; writing 1 in power-down mode will initiate a new comparison. When reading: always returns 0.
14:12	MUX[2:0]	R/W	0h	00: AINP = AIN0 and AINN = AIN1 (default) 01: AINP = AIN0 and AINN = AIN3 10: AINP = AIN1 and AINN = AIN3 11: AINP = AIN2 and AINN = AIN3 100: AINP = AIN0 and AINN = GND 101: AINP = AIN1 and AINN = GND 110: AINP = AIN2 and AINN = GND 111: AINP = AIN3 and AINN = GND
11:9	PGA[2:0]	R/W	2h	000: FSR = ±6.144 V 001: FSR = ±4.096 V 010: FSR = ±2.048 V (default) 011: FSR = ±1.024 V 100: FSR = ±0.512 V 101: FSR = ±0.256 V 110: FSR = ±0.256 V 111: FSR = ±0.256 V
8	MODE	R/W	1h	0: Continuous working mode 1: Single-use or power-down mode (default)
7:5	DR[2:0]	R/W	4h	00: 8 SPS 01: 16 SPS 10: 32 SPS 11: 64 SPS 100: 128 SPS (default) 101: 250 SPS 110: 475 SPS 111: 860 SPS
4	TS_MODE	R/W	0h	0: Ordinary ADC mode (default) 1: Temperature sensor mode
3	PULL_UP_EN	R/W	1h	0: No pull-up resistor 1: It has a pull-up resistor, approximately 400K Ω (default)
2:1	NOP[1:0]	R/W	1h	01: Data is valid. Write the current 16-bit data to the register Other: Invalid data packet, ignore the current 16 bits data
0	Reserved	R	1h	Reserved. Read 1

13. Applications

Most microcontrollers' SPI peripherals can work with the DADS1118. This interface operates in SPI mode 1 (CPOL=0, CPHA=1). In this mode, the SCLK clock signal remains low in the idle state, and data is only triggered or changed on the rising edge of SCLK; the master and slave devices latch or read data on the falling edge of SCLK.

It is recommended to connect a 50Ω resistor in series with each digital pin path to provide short-circuit protection. However, special attention should be paid to ensure that all SPI timing requirements are still met, as these additional series resistors and bus parasitic capacitances on the digital signal lines can cause signal distortion.

The DADS1118 's fully differential input interface is ideal for connecting differential signal sources with low to medium source impedance, such as thermocouples and thermistors. Although the device can read fully differential signals, its inputs cannot withstand negative voltages due to ESD protection diodes on each pin. These diodes conduct to protect the device from ESD damage when the input voltage exceeds the supply voltage or falls below ground.

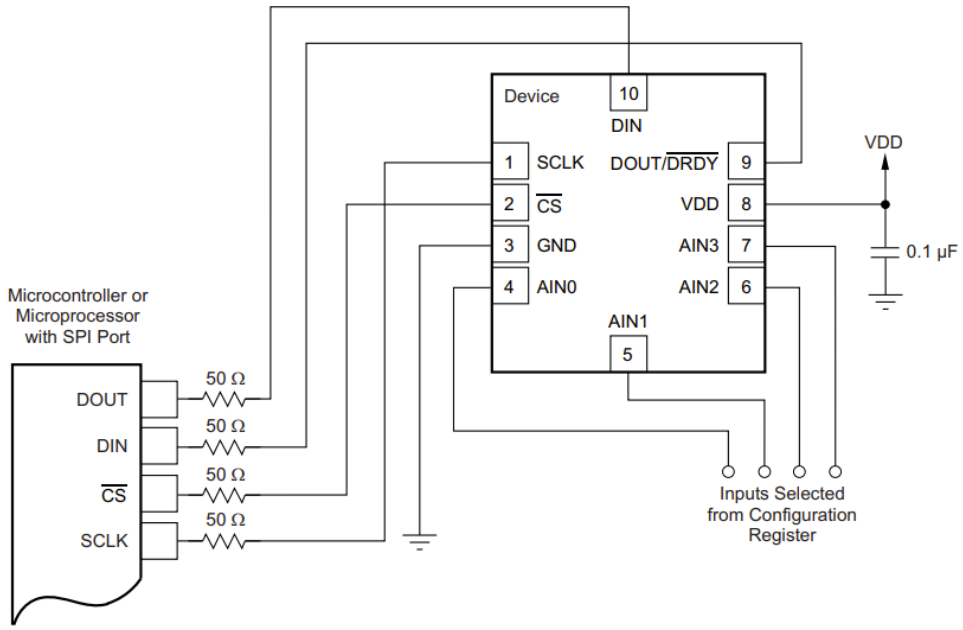
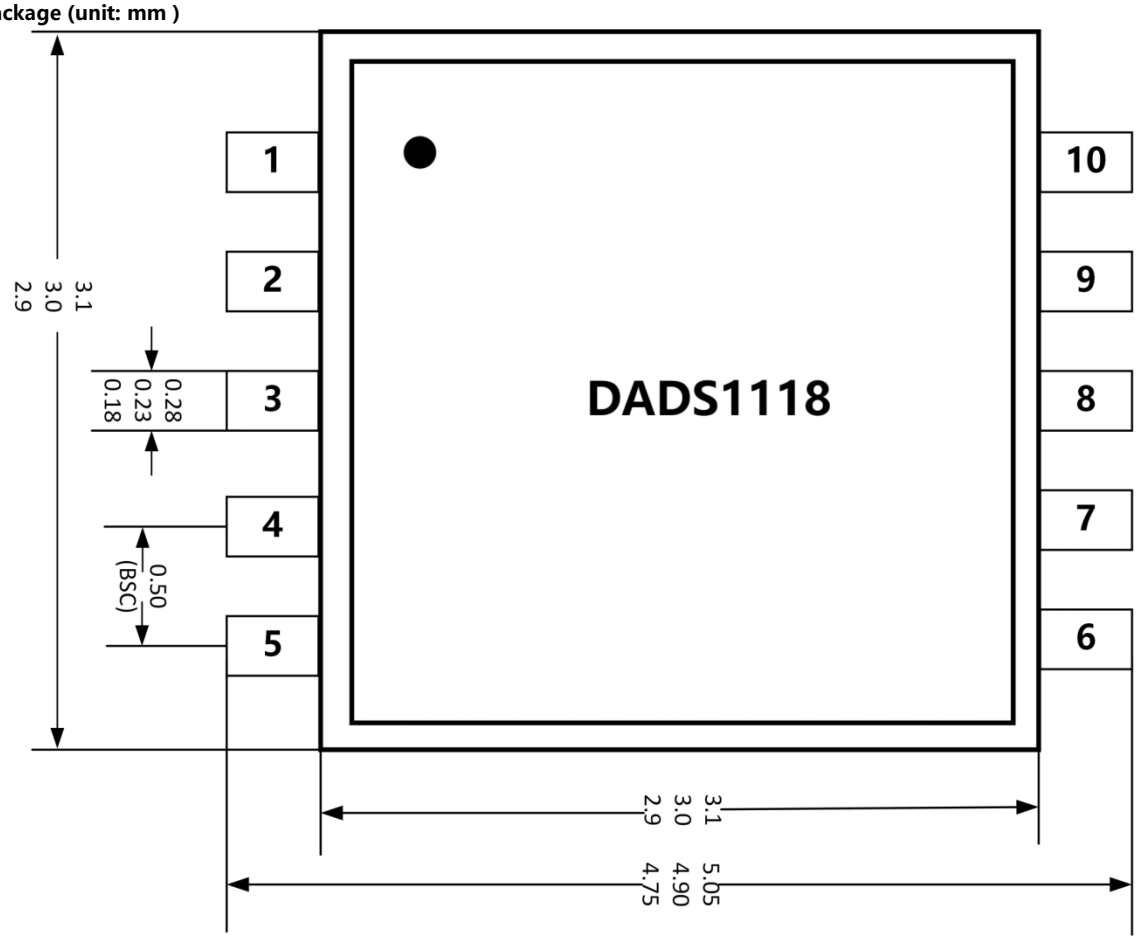


Figure 4. Typical Connections

14. Package Dimensions and Structure

MSOP-10 package (unit: mm)



15. Device Ordering Information

Model	Temperature Range	Packaging Type	Package Quantity
DADS1118MS	-40 ℃ ~125 ℃	MSOP-10	4,000/reel