1. Features

- Wide power supply voltage : 2.5V to 5.5V
- Low current consumption : 150μA (continuous conversion mode)
- Programmable data transfer rates : 8SPS to 860SPS
- Single-cycle stability
- Internal low-drift voltage reference
- Internal oscillator
- Internal programmable gain amplifier
- I²C interface : can be configured with 2 addresses
- Four single-ended or two differential inputs
- Operating temperature range: -40°C to +125°C
- M SOP-10 package (3.00mm × 3.00mm)

2. Applications

- Portable instrument
- Battery voltage and current monitoring
- Temperature measurement system
- Consumer electronics
- Industrial automation and process control

3. Overview

The DADS1115 is an I²C-compliant 16 -bit high-precision, low-power analog-to-digital converter (ADC) in an MSOP-10 package.

The DADS1115 incorporates a low-drift voltage reference and oscillator. It also features a programmable gain amplifier (PGA) and a digital comparator. These characteristics, combined with a wide operating supply voltage range, make the DADS1115 ideal for power- and space-constrained sensor measurement applications. The DADS1115 can perform conversions at data rates up to 860 samples per second (SPS). The PGA provides an input range from ±256mV to ±6.144V, enabling accurate measurements of both large and small signals. The DADS1115 features a single-input multiplexer (MUX) for two differential input measurements or four single-ended input measurements. Undervoltage and overvoltage detection can be performed using digital comparators within the DADS1115. The DADS1115 can operate in both continuous conversion and single- shot modes. In single -use mode, these devices can automatically power off after a single conversion; thus significantly reducing power consumption during idle periods.

4. Device packaging information

Product Model	Packaging Type	Package Size
DADS1115	M SOP-10	3mm × 3mm

5. Functional Block Diagram

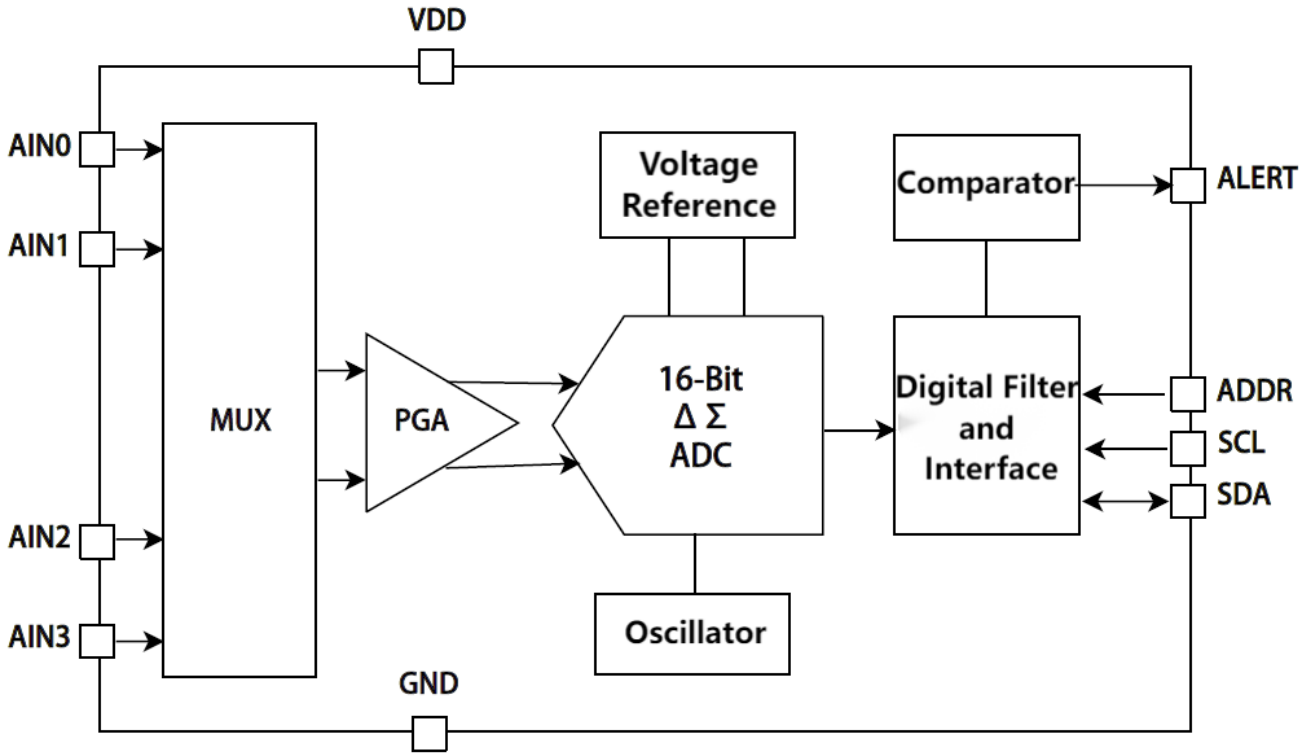

Figure 1. Functional Block Diagram

6. Pin Configuration and Functions

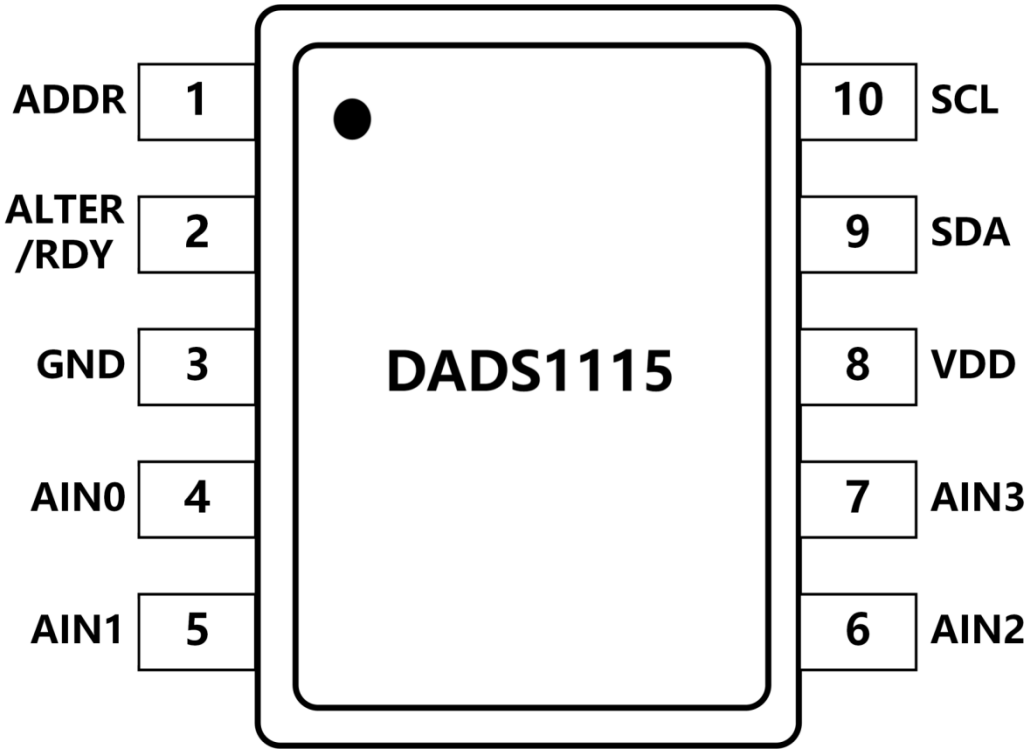

Figure 2. Pin Configuration

Pin Functions

Pin No.	Symbol	Function
1	ADDR	I² C select from address
2	ALTER/RDY	The comparator output or conversion is ready
3	GND	Ground
4	AIN0	Analog input 0
5	AIN1	Analog input 1
6	AIN2	Analog input 2
7	AIN3	Analog input 3
8	VDD	Power supply
9	SDA	I²C data
10	SCL	I²C clock

7. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Temperature			
Operating temperature (T_A)	- 40	125	℃
Storage temperature (T_J)	- 40	150	℃
Junction temperature (T_{stg})	- 60	150	℃
Pressure resistance			
VDD	- 0.3	7	V
Analog Input	GND - 0.3	VDD + 0.3	V
Numeric input	GND - 0.3	5.5	V
Traffic limiting			
Input current	- 10	10	m A
ESD			
HBM	4,000		V
CDM	1,000		V

Exceeding the listed absolute maximum ratings may cause permanent damage to the equipment. These are only pressure ratings and do not imply that the equipment will function properly under any conditions exceeding the recommended operating conditions. Prolonged exposure to absolute maximum ratings may affect the reliability of the equipment.

8. Electrical Characteristics

Under the conditions of VDD=3.3V, data rate=8SPS, and full-scale input voltage range (FSR)=±2.048V (unless otherwise specified). Maximum and minimum specifications apply to a temperature range of T_A=-40°C to +125°C. Typical specifications apply to T_A - 25°C.

Parameter	Test conditions		Max	Typ	Min	Unit
Analog Input						
Common-mode input impedance	FSR = ±6.144V			22		MΩ
	FSR = ±4.096V, FSR = ±2.048V			16, 11.5		
	FSR = ±1.024V			23		
	FSR = ±0.512V, FSR = ±0.256V			26.6		
Differential input impedance	FSR = ±6.144V			16		MΩ
	FSR = ±4.096V			14		
	FSR = ±2.048V			6.8		
	FSR = ±1.024V			1.7		
	FSR = ±0.512V, ±0.256V			76 0 , 520		kΩ
System Performance						
Resolution (no missing bits)			16			Bits
Data rate			8, 16, 32, 64, 128, 250, 475, 860			SPS
Data rate error	All data rates		-10%		10%	
Output noise			See the noise performance section.			
INL Integral Nonlinearity	DR=8SPS, FSR=±2.048V				1	LSB
Offset error	FSR = ±2.048V, differential input		-3	±1	3	LSB
	FSR = ±2.048V, single-ended input			±3		LSB
Temperature drift offset	FSR = ±2.048V			0.005		LSB/°C
long-term temperature drift	FSR=±2.048V, T_A =125°C,1000hrs			±1		LSB
Offset power supply suppression	FSR = ±2.048V, DC power supply variation			1		LSB/V
Offset matching	Matching between any two inputs			3		LSB
Gain error	FSR = ±2.048V, T_A =25°C			0.02 %	0.15%	
Gain Temperature Drift	FSR = ±0.256V			7		ppm/°C
	FSR = ±2.048V			5	4 0	
	FSR = ±6.144V			5		
Long-term gain drift	FSR=±2.048V, T_A =125°C,1000hrs			±0.05		%
Gain power supply rejection				14 0		ppm/V
Gain Matching	Matching between any two gains			0.06 %	0.1 %	
Gain Channel Matching	Matching between any two channels			0.05 %	0.1 %	
Common-mode rejection ratio	At DC, FSR = ±0.256V			90		dB
	At DC, FSR = ±2.048V			1 0 0		
	At DC, FSR = ±6.144V			98		
	f_{CM} = 60Hz, DR = 8SPS			95		
	f_{CM} = 50Hz, DR = 8SPS			115		
Data Input/Output						
V_{IH}			0.7VDD		5.5	V
V_{IL}			GND		0.3VDD	V
VOL	IOL = 3mA		GND	0.15	0.3VDD	V
Input leakage current	GND < V_{DIG} < VDD		- 10		1 0	μA
Power Supply						
I_{VDD} operating current	Power off mode	T_A = 25°C		0.5	2	μA
	Operating mode	T_A = 25°C		165	21 0	μA

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P_D power consumption	VDD=5.0V		0.96		mW
	VDD=3.3V		0.6		mW

9. Timing Specifications

Beyond the operating ambient temperature range, VDD = 2.0V to 5.5V (unless otherwise specified) .

Parameter	Description	Quick Mode		Unit
		Min	Max	
f_{SCL}	SCL clock frequency	0.01	0.4	ns
t_{BUF}	Bus idle time between START and STOP states	600		ns
t_{HDSTA}	The hold time for the START signal. After this period, the first clock is generated.	600		ns
t_{SUSTA}	START creation time	600		ns
t_{SUSTO}	STOP establishment time	600		ns
t_{HDDAT}	Data retention time	0		ns
t_{SUDAT}	Data creation time	100		ns
t_{LOW}	Low level time of SCL clock pin	1,300		ns
t_{HIGH}	High-level time of SCL clock pin	600		ns
t_F	Fall time of SDA and SCL signals (1)		300	ns
t_R	Rise time of SDA and SCL signals (1)		300	ns

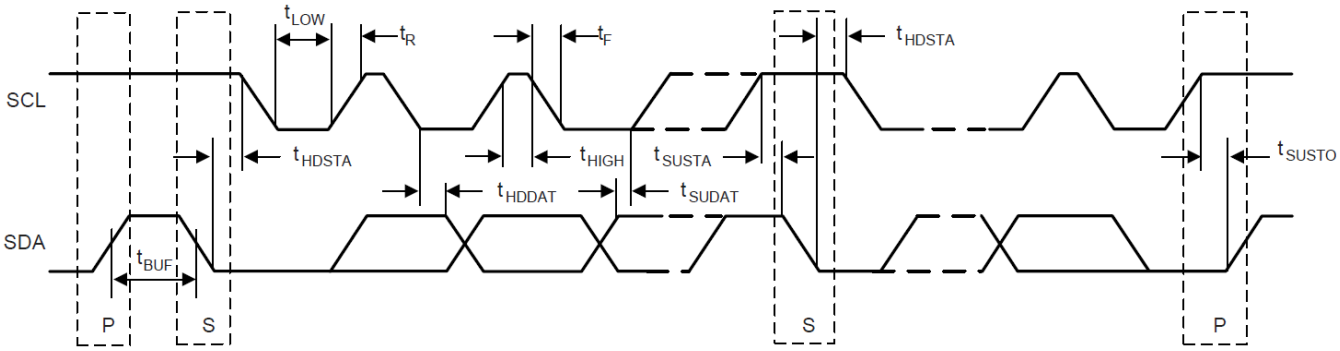


Figure 3. I²C Interface Timing

10. Working Principle

- **Overview**

The DADS1115 is a low-power 16-bit ΔΣ ADC that integrates a voltage reference, oscillator, programmable gain amplifier, and programmable digital comparator. The DADS1115 ADC core measures the differential signal V_{IN}, which is the difference between V_{AINP} and V_{AINN}. The converter core consists of a differential switched-capacitor ΔΣ modulator and a digital filter. This architecture results in very strong attenuation of any common-mode signal. The input signal is compared to an internal reference voltage. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage. The DADS1115 offers two available conversion modes: single-trigger conversion and continuous conversion. In single-trigger mode, the ADC performs a single conversion on the input signal upon request, stores the converted value in the internal conversion register, and then enters a power-off state. This mode is designed to provide significant energy savings for systems that require only periodic conversions or have long idle periods between conversions. In continuous conversion mode, the ADC automatically begins converting the input signal once the previous conversion is complete. The continuous conversion rate is equal to the programmed data rate. Data can be read at any time and always reflects the most recently completed conversion.

- **Multiplexer**

The DADS1115 has a built-in multiplexer that selects one of eight channels (four single-ended inputs and four differential inputs) as input for conversion through different configurations of the MUX[2:0] registers. When a single-ended signal is measured, the negative input of the ADC is connected to GND via a switch on the MUX. Refer to the description of MUX[2:0] in the register table for specific configuration information.

- **FSR and LSB**

The FSR is configured by the Config register PGA[2:0], and the LSBs corresponding to each range are as follows:

FSR	LSB
±6.144V	187.5μV
±4.096V	125μV
±2.048V	62.5μV
±1.024V	31.25μV
±0.512V	15.625μV
±0.256V	7.8125μV

The analog input voltage must not exceed the analog input voltage given in the absolute maximum rating. Therefore, when FSR>VDD+0.3V, the input will be clamped at VDD+0.3V, and the portion exceeding this voltage cannot be measured.

- **Reference voltage**

The DADS1115 integrates a low-temperature drift voltage reference, which only provides an internal voltage reference and cannot be output externally.

- **Oscillator**

The DADS1115 has a built-in 1MHz oscillator, and the chip's output data rate is proportional to the internal clock frequency.

- **Data rate**

The DADS1115 provides a programmable data rate, which can be configured via the Config registers DR[2:0].

- **Digital comparator**

The DADS1115 incorporates a programmable digital comparator that compares the input conversion result with an internally preset value, triggering an alarm upon meeting specific conditions and responding via the ALERT/RDY pin. The COMP_MODE bit in the Config register configures the comparator as either a regular comparator or a window comparator. In regular comparator mode, the ALERT/RDY pin generates a set response (default low) when the converted data exceeds the limit set in the Hi_thresh register. The set response is canceled only when the converted data falls below the limit set in the Lo_thresh register. In window comparator mode, the ALERT/RDY pin generates a set response when the converted data exceeds or falls below the value in the Hi_thresh register. The polarity of the set response level can be configured via the COMP_POL bit in the Config register. In both regular and window comparator modes, the comparator output can be latched by configuring the COMP_LAT bit in the Config register. This latch can only be cleared by reading the Conversion register. The comparator can also be configured to generate a set response

only when multiple consecutive readings exceed the comparator threshold. The number of times the threshold is exceeded is set by the COMP_QUE[1:0] bits in the Config register. The COMP_QUE[1:0] bits can also disable the comparator function and place the ALERT/RDY pins in a high-impedance state.

- **Switching ready pins**

The ALERT/RDY pin can also be configured as a conversion-ready pin. Setting the most significant bit of the Hi_thresh register to 1 and the most significant bit of the Lo_thresh register to 0 configures the ALERT/RDY pin as a conversion-ready pin. To use the conversion-ready pin function, the COMP_QUE[1:0] bits must be set to any two-bit value other than 0b11. In this mode, the COMP_MODE and COMP_LAT bits no longer control any function. In single-conversion mode, if the COMP_POL bit is set to 0, the ALERT/RDY pin goes low after the conversion; if the COMP_POL bit is set to 1, the ALERT/RDY pin goes high after the conversion. In continuous conversion mode, if the COMP_POL bit is set to 0, a low level of approximately 8μs is provided on the ALERT/RDY pin at the end of each conversion; if the COMP_POL bit is set to 1, as shown in Figure 4, a high level of approximately 8μs is provided on the ALERT/RDY pin at the end of each conversion.

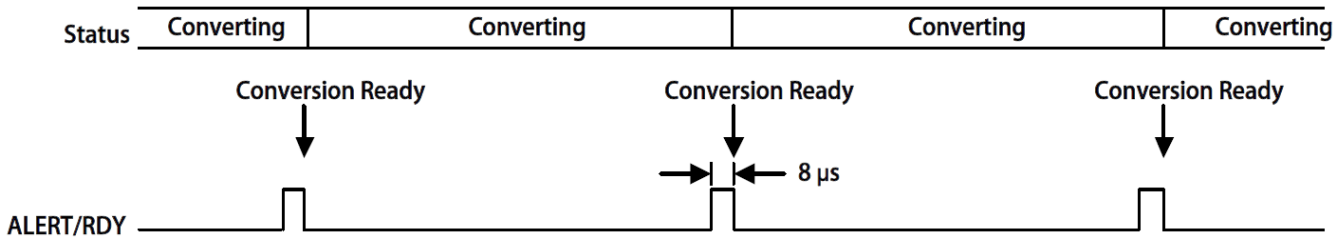


Figure 4. Transition ready pulse during continuous transition (COMP_POL=1)

- **Noise performance**

Δ-Σ ADCs are based on the oversampling principle, where the input signal is sampled at a high frequency, followed by filtering and extraction. The ratio of the sampling frequency to the output data rate is called the oversampling ratio (OSR). By increasing the oversampling ratio, the noise performance of the ADC can be optimized, which is very useful when measuring small signals.

Table 1. Root mean square and peak-to-peak noise (μVrms, μVpp) at VDD= 3.3V

Data rate (SPS)	FSR (Full Scale Range)					
	±6.144V	±4.096V	±2.048V	±1.024V	±0.512V	±0.256V
8	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
1 6	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
3 2	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
6 4	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
1 28	187.5 (187.5)	125 (125) 62.5	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (12.35)
2 50	187.5 (252.09)	125 (148.28)	62.5 (84.03)	31.25 (39.54)	15.62 (16.06)	7.81 (18.53)
4 75	187.5 (266.92)	125 (227.38)	62.5 (79.08)	31.25 (56.84)	15.62 (32.13)	7.81 (25.95)
8 60	187.5 (430.06)	125 (266.93)	62.5 (118.63)	31.25 (64.26)	15.62 (40.78)	7.81 (35.83)

Table 2. Effective resolution and noise-free resolution at VDD=3.3V

Data rate (SPS)	FSR (Full Scale Range)					
	±6.144V	±4.096V	±2.048V	±1.024V	±0.512V	±0.256V
8	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
1 6	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
3 2	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
6 4	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
1 28	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.33)
2 50	16 (15.57)	16 (15.75)	16 (15.57)	16 (15.66)	16 (15.96)	16 (14.75)
4 75	16 (15.49)	16 (15.13)	16 (15.66)	16 (15.13)	16 (14.95)	16 (14.26)
8 60	16 (14.8)	16 (14.9)	16 (15.07)	16 (14.95)	16 (14.61)	16 (13.8)

11. Functions and Modes

- **Reset**

The DADS1115 resets upon power-on, setting all bits in the Config register to their default values. After the reset, it enters power-down mode, where the chip interface and digital module are active but do not perform data conversion. It can also be reset via the I²C reset command. When the chip receives the general call reset (06h) command, it performs an internal reset, which has the same effect as a power-on reset.

- **Switching modes**

The DADS1115 has two conversion modes: single conversion mode and continuous conversion mode, and the operating mode can be selected via the MODE bit in the Config register.

Single Conversion Mode – When the MODE bit in the Config register is 1, the chip enters power-down mode, where it can still respond to commands. The chip remains in power-down mode until the OS bit in the Config register is written to 1. When the OS bit is set to 1, the chip starts up within approximately 30μs, automatically clearing the OS bit to 0 and beginning a single conversion. After the AD data conversion is complete, the chip re-enters power-down mode. Writing a 1 to the OS bit while conversion is in progress has no effect. To switch to continuous conversion mode, a 0 must be written to the MODE bit in the Config register.

Continuous Conversion Mode – When the MODE bit in the Config register is 0, the chip enters continuous conversion mode. After one A/D conversion is completed, the chip places the conversion result into the Conversion register and immediately begins the next conversion. To switch to single-conversion mode, write 1 to the MODE bit in the Config register.

12. Digital Interface

The DADS1115 uses the I²C protocol for communication. If the I²C bus remains idle for more than 30ms, it will time out.

- **I²C address selection**

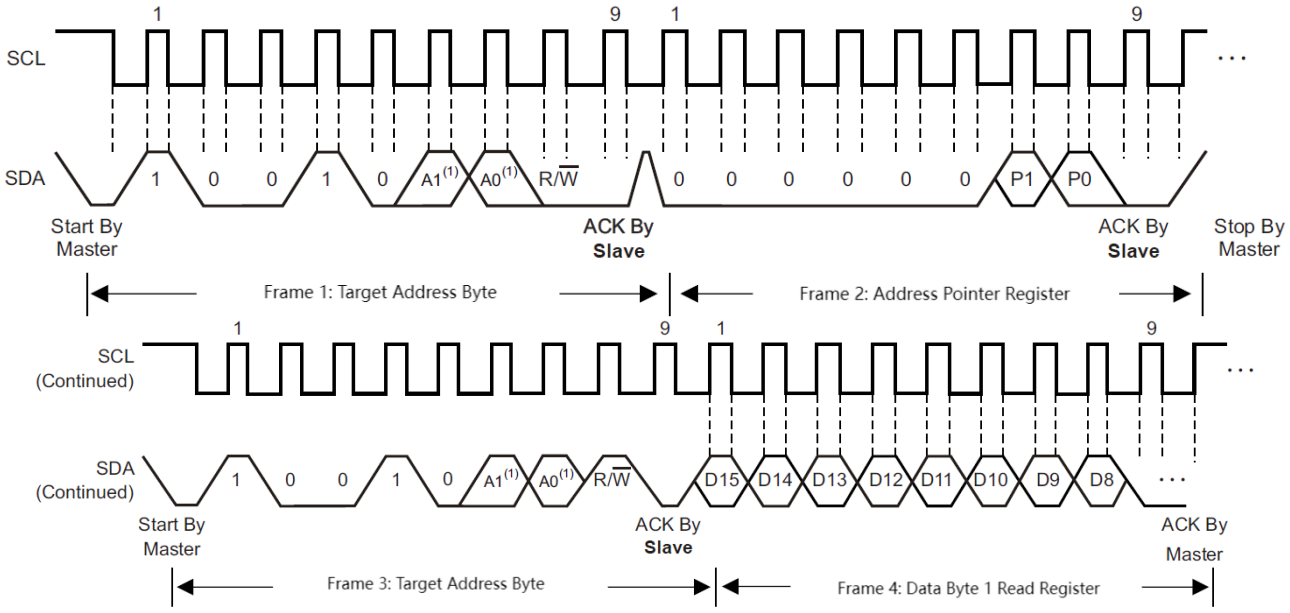
The ADDR pin of the DADS1115 is used to configure the I²C address and can be connected to GND, VDD, SDA, and SCL. The corresponding addresses are shown in the table below.

Table 3. ADDR Address Selection

ADDR connection	SLAVE address
GND	1001000
VDD	1001001

- **I²C timings**

Timing Diagram for Reading



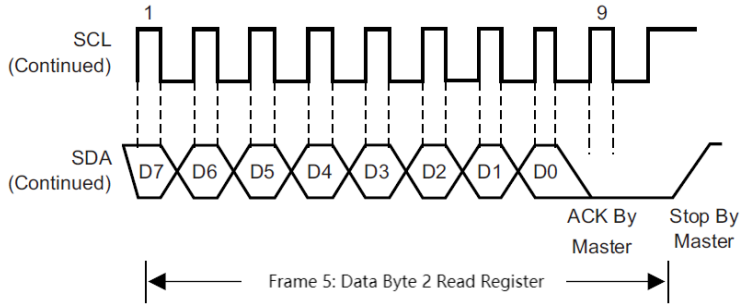


Figure 5. Reading Timing Diagram

Timing Diagram for Write

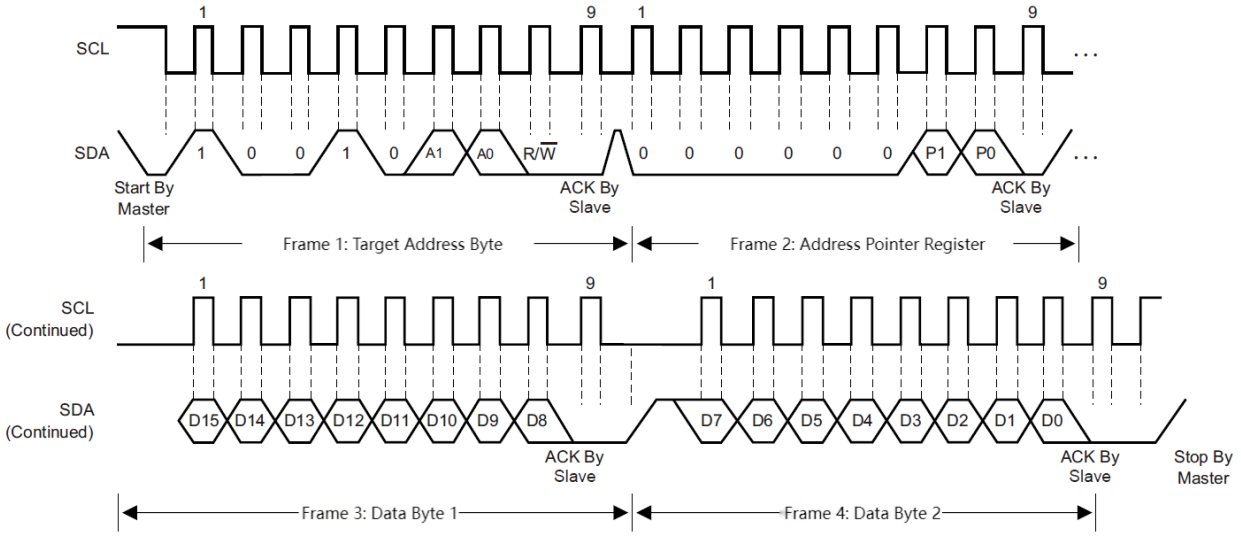


Figure 6. Write timing diagram

13. Data Format

The DADS1115 provides 16-bit binary data, and Table 4 summarizes the ideal output code values for different input signals.

Table 4. Output Codewords

Input	Output
≥+FS(2 15 -1)/2 15	7FFFh
+FS/2 15	0001h
0	0000h
-FS/2 15	FFFFh
≤-FS	8000h

14. Registers

- **ADDRESS**

Bit	Name	Access type	Reset	Description
7:2	Reserved	W	0h	Only 0h can be written
1:0	P[1:0]	W	0h	Register address 00: CONVERSION 01: CONFIG 10: Lo_THRESH 11: Hi_THRESH

- **CONVERSION**

Bit	Name	Access type	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion data

- **CONFIG**

Bit	Name	Access type	Reset	Description
	OS	R/W	1h	This bit can only be written in power-off mode; writing in conversion mode is invalid. When writing: 0: Invalid 1: Initiate a single conversion (in power failure mode) When reading: 0: The chip is performing a conversion. 1: The chip did not perform the conversion.
14:12	MUX[2:0]	R/W	0h	Input multiplexer configuration 000: AINP = AIN0, AINN = AIN1 (default value) 001: AINP = AIN0, AINN = AIN3 010: AINP = AIN1, AINN = AIN3 011: AINP = AIN2, AINN = AIN3 100: AINP = AIN0, AINN = GND 101: AINP = AIN1, AINN = GND 110: AINP = AIN2, AINN = GND 111: AINP = AIN3, AINN = GND
11:9	PGA[2:0]	R/W	2h	Programmable gain amplifier configuration 000: FSR = ±6.144V 001: FSR = ±4.096V 010: FSR = ±2.048V (default value) 011: FSR = ±1.024V 100: FSR = ±0.512V 101: FSR = ±0.256V 110: FSR = ±0.256V 111: FSR = ±0.256V
8	MODE	R/W	1h	Chip operating mode 0: Continuous conversion mode 1: Single conversion mode or power failure mode (default)

Bit	Name	Access type	Reset	Description
7:5	DR[2:0]	R/W	4h	Data rate configuration 000: 8 SPS 001: 16 SPS 010: 32 SPS 011: 64 SPS 100: 128 SPS (default value) 101: 250 SPS 110: 475 SPS 111: 860 SPS
4	COMP_MODE	R/W	0h	Comparator pattern 0: Standard comparator (default value) 1: Window Comparator
3	COMP_POL	R/W	0h	Comparator polarity 0: Low-level response (default) 1: High-level response
2	COMP_LAT	R/W	0h	Comparator output latch configuration 0: The ALERT/RDY pin is not latched after being set (default value). 1: The ALERT/RDY pin is latched after being set. To release the set state, the ADC conversion result must be read.
1:0	COMP_QUE[1:0]	R/W	3h	When set to 11, the comparator is disabled, and the ALERT/RDY pin is set to a high-impedance state. When set to other values, the ALERT/RDY pin and comparator functions are enabled, and the setting value determines the number of consecutive transitions that occur before the upper and lower thresholds are set on the ALERT/RDY pin. 00: Post-conversion bit 01: Position after two conversions 10: Post-conversion bit 11: Disable the comparator and set the ALERT/RDY pin to high impedance (default value).

THRESH

Bit	Name	Access type	Reset	Description
15:00	Lo_thresh[15:0]	R/W	8000h	Comparator low threshold
15:00	Hi_thresh[15:0]	R/W	7FFFh	Comparator high threshold

15. Application

The following describes a typical application example of the DADS1115, with a typical connection shown in Figure 7. The chip communicates with the host via the I²C interface . The host provides a clock signal on the SCL pin, and data is transmitted using the SDA pin. The first byte sent by the host is the chip address, and the second byte is the register address. The third and fourth bytes sent by the host are written into the registers indicated by the register address pointer bits P[1:0]. The timing diagrams for read and write operations are shown in Figures 5 and 6, respectively.

The following example illustrates how to set up continuous conversion mode and read data:

1. Write to the Config register
- First byte: 0b10010000 (The first 7 bits are the I²C address, and the last bit R/W is set low)
- Second byte: 0b00000001 (Config register address)
- Third byte: 0b10000100 (MSB of the Config register data)
- Fourth byte: 0b10000011 (LSB of the Config register data)

2. Switch the Address Pointer to the Conversion register.
- First byte: 0b10010000 (The first 7 bits are the I²C address, and the last bit is R/W set low)
- Second byte: 0b00000000 (switch to Conversion register address)

3. Read the Conversion register
- First byte: 0b10010001 (first 7 bits are I²C address, last bit R/W is set high)
- Second byte: The MSB of the Conversion register returned by the chip
- Third byte: The LSB of the Conversion register returned by the chip

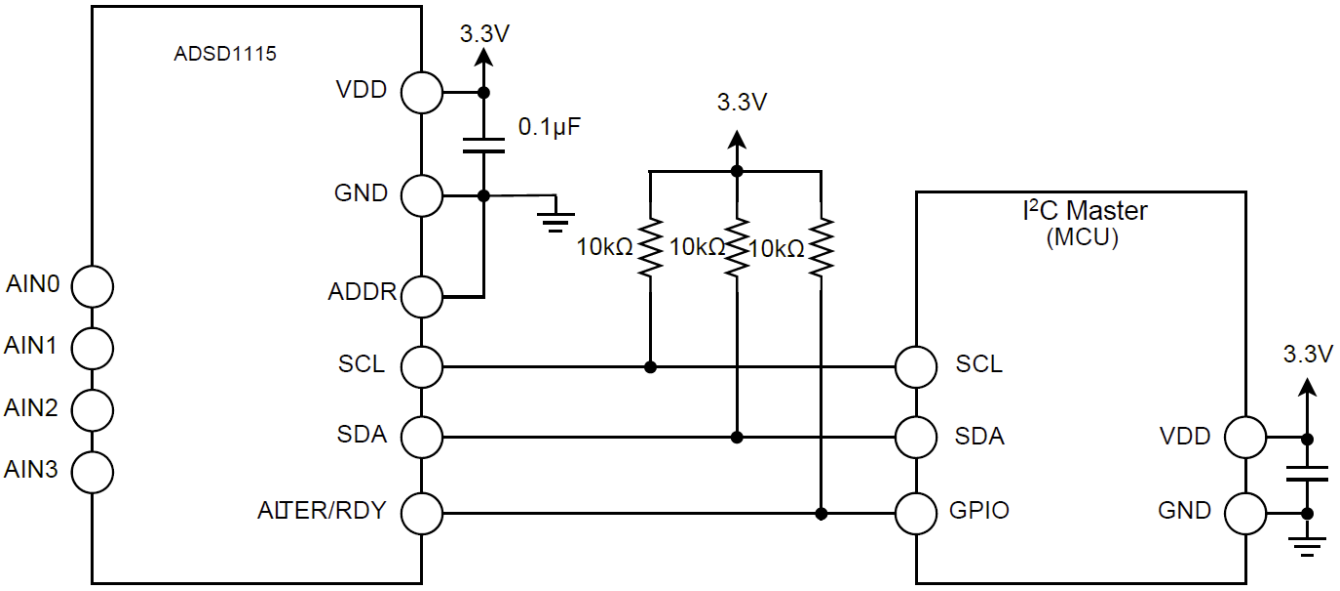
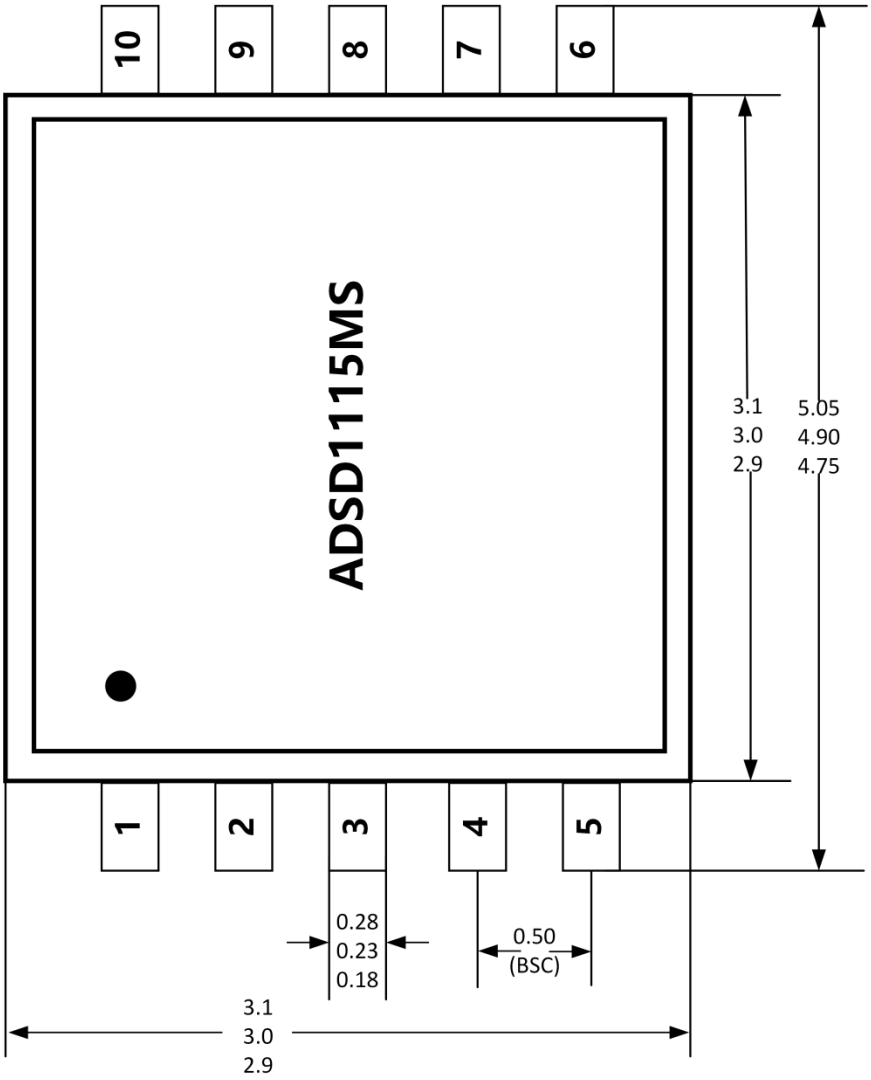


Figure 7. Typical Connections

16. Package Size and Structure

MSOP-10 package (unit: mm)



17. Package Dimensions and Structure

Model	Temperature Range	Packaging Type	Package
DADS1115	-40 ℃ ~125 ℃	MSOP-10	4,000/reel