DAD9957　High-Speed, 14 Bits DAC

Features

- Power supply: 1.8V and 3.3V
- Internal system clock: 1 GSPS (up to 400 MHz analog output)
- Built-in 1 GSPS 14-bit DAC
- Input data rate: 250 MSPS
- Output phase noise: ≤ -124dBc /Hz (1kHz offset, 400MHz carrier)
- Narrowband SFDR: >80 dB
- Eight programmable profile registers support shift keying inverse sinc correction filters.
- Reference clock frequency multiplication function
- Internal oscillator, supporting single-crystal operation
- Power saving function controlled by software/hardware
- Integrated RAM
- Phase modulation function
- Multi-chip synchronization
- Easy interface with BlackfinSPORT
- Configurable interpolation factor from 4 to 252 times
- Gain Control DAC
- The internal frequency divider supports reference frequencies up to 2GHz.
- Package: 100-pin TQFP_EP

Applications

- HFC data, telephony, and video modems
- Wireless base station transmission
- Broadband communication transmission
- VoIP

Product Description

The DAD9957 can function as an I/Q modulator and upconverter in a variety of high-end communication systems. Internally, the DAD9957 integrates a high-speed direct digital frequency synthesizer (DDS), a high-speed 14-bit digital-to-analog converter (DAC), clock multiplier circuitry, digital filters, and other DSP functions. This chip provides baseband upconversion for data transmission in wired or wireless communication systems, offering excellent performance in terms of speed, power consumption, and spectral performance. The chip supports 16-bit serial input I/Q baseband data and can be programmed to function as a single-frequency sine wave source or in interpolation DAC mode. The chip utilizes an internal oscillator, a high-speed divide-by-two circuit, and a low-noise phase-locked loop (PLL) to achieve a high-speed internal sampling clock.

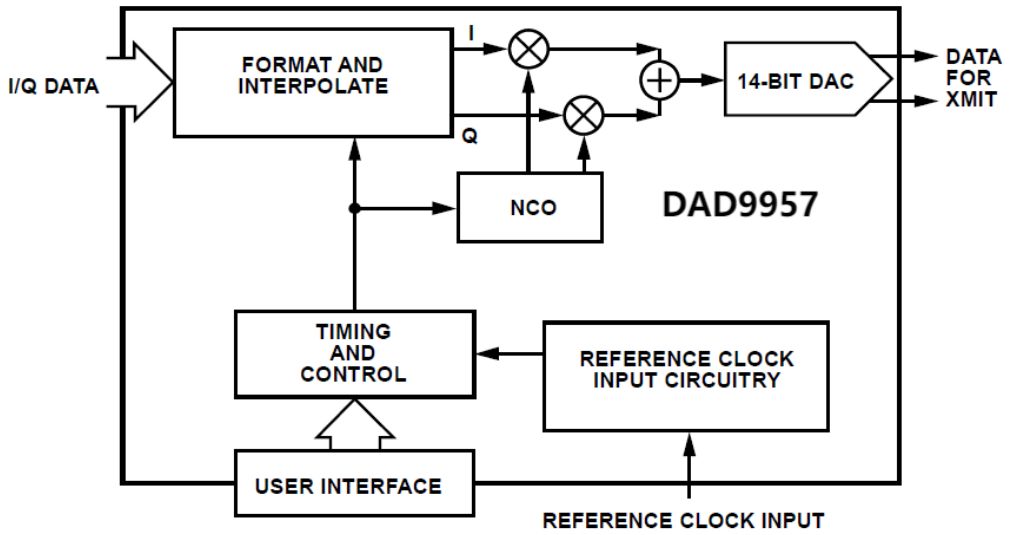

Figure 1. Functional block diagram of DAD99

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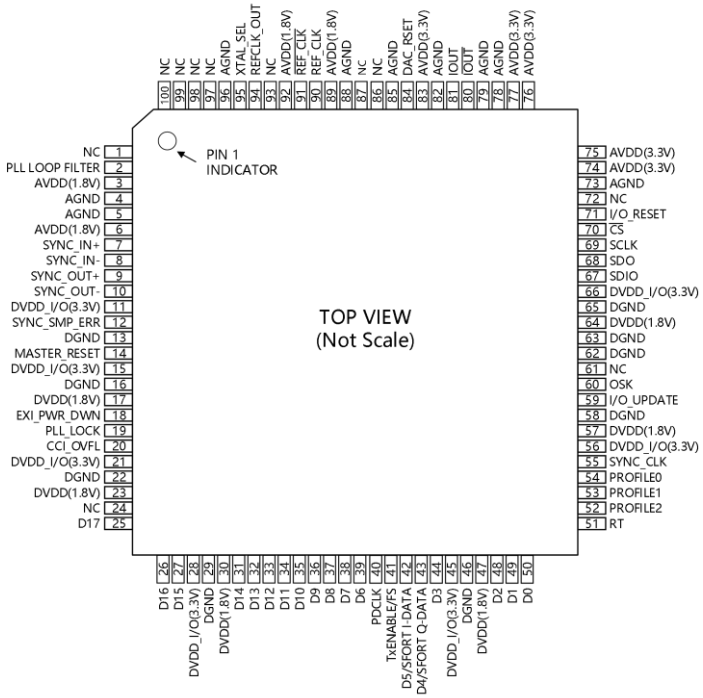
Electrical characteristics

Unless otherwise specified, A_{VDD} (1.8V) and D_{VDD} (1.8V) = 1.8V±5%, A_{VDD} (3.3V) = 3.3V±5%, D_{VDD}_I/O (3.3V) = 3.3V±5%, T = 25°C, RSET = 10kΩ, I_{OUT} = 20mA, external reference clock frequency = 1000MHz and REFCLK multiplier disabled.

Parameter	Test conditions	Mini	Typ	Max	Unit
REF_CLK input characteristics					
Frequency range					
REFCLK multiplier	Disable	60		1000	MHz
	Enable	3.2		60	MHz
Maximum REFCLK input divider frequency	Full temperature range	1500	1900		MHz
Minimum REFCLK input divider frequency	Full temperature range		25	35	MHz
external crystal			25		MHz
Input capacitor			3.2		pF
Input impedance (differential)			2.9		kΩ
Input impedance (single-ended)			1.45		kΩ
Duty cycle	REFCLK Multiplier Disabled	45		55	%
	REFCLK Multiplier Enable	40		60	%
REF_CLK input level	Single-ended	50		1000	mV pp
	Difference	100		2000	mV pp
REFCLK Multiplier VCO Gain Characteristics					
V_{CO} gain (kV) (cInput frequency)	V_{CO0} range setting		432		MHz/V
	V_{CO1} range setting		505		MHz/V
	V_{CO2} range setting		560		MHz/V
	V_{CO3} range setting		754		MHz/V
	V_{CO4} range setting		785		MHz/V
	V_{CO5} range setting		853		MHz/V
REFCLK_OUT feature					
Maximum capacitive load			20		pF
Maximum frequency			25		MHz
DAC output characteristics					
Full-scale output current		8.5	20	31.5	mA
Gain error		-10		10	%FS
Output offset				3.4	uA
Differential nonlinearity			0.9		LSB
Integral nonlinearity			1.7		LSB
Output capacitor			4.5		pF
Residual phase noise	The offset is 1kHz and A_{OUT} is 20MHz				
REFCLK multiplier	Disable		-150		dBc/Hz
	Enable, 20x		-141		dBc/Hz
	Enable, 100x		-139		dBc/Hz
AC output voltage range		-0.5		0.5	V
Spurious-free dynamic range (SFDR single-frequency modulation)					
F_{OUT} = 20.1MHz			- 69		dBc
F_{OUT} = 98.6MHz			- 68		dBc
F_{OUT} = 201.1MHz			- 64		dBc
F_{OUT} = 397.8MHz			- 55		dBc
Noise spectral density (NSD)					
Single-frequency modulation					
F_{OUT} = 20.1MHz			-166		dBm/Hz
F_{OUT} = 98.6MHz			-160		dBm/Hz
F_{OUT} = 201.1MHz			-155		dBm/Hz
F_{OUT} = 397.8MHz			-150		dBm/Hz
Intermodulation distortion (IMD)	I/Q rate = 62.2 MSPS; 16x interpolation				
F_{OUT} = 25MHz			-81		dBc
F_{OUT} = 50MHz			-76		dBc
F_{OUT} = 100MHz			-71		dBc

Modulator characteristics			
Input data			
Error vector magnitude	2.5Msymbols/sQPSK, 4x oversampling	0.58	%
	270.8333 ksymbols/s, GMSK, 32x oversampling	0.79	%
	2.5 Msymbols/s, 256-QAM, 4x oversampling	0.38	%
WCDMA-FDD(TM1), 3.84MHz bandwidth and 5MHz channel spacing			
Adjacent channel leakage ratio (ACLR)	IF=143.88MHz	-76	dBc
Carrier feedthrough		-77	dBc
Serial port timing characteristics			
Maximum SCLK frequency		70	Mbps
Minimum SCLK pulse width	Low	4.5	ns
	High	4.5	ns
SCLK Maximum rise/fall time		2.2	ns
Shortest data setup time to SCLK		6	ns
Minimum data retention time to SCLK		0	ns
Longest data validity time in read mode		11	ns
I/O_UPDATE/PROFILE<2:0>/RT Timing Characteristics			
Shortest pulse width	High	1	SYNC_CLK cycle
Shortest setup time to SYNC_CLK		1.78	ns
Minimum hold time to SYNC_CLK		0	ns
I/Q Input Timing Characteristics			
PDCLK maximum frequency		250	MHz
Shortest I/Q data setup time to PDCLK		1.7	ns
Shortest I/Q data hold time to PDCLK		0	ns
Shortest TxEnable creation time to PDCLK		1.7	ns
Minimum TxEnable retention time to PDCLK		0	ns
Other timing characteristics			
Wake-up time			
Quick recovery mode		8	SYSCLK cycle
Deep sleep mode		153	us
Shortest reset pulse width (high level)		5	SYSCLK cycle
Data latency (pipeline latency)			
Single-frequency or Profile mode data latency			
Frequency, phase, and amplitude to DAC output	Match Delay Enable	91	SYSCLK cycle
Frequency and phase to DAC output	Matching delay disabled	79	SYSCLK cycle
SYSCLK cycle			
Voltage			
Logic 1		2.0	V
Logic 0		0.8	V
Current			
Logic 1		93 123	uA
Logic 0		39 51	uA
Input capacitor		2.3	pF
XTAL_SEL input			
Logic 1 Voltage		1.25	V
Logic 0 voltage		0.6	V
Input capacitor		2.3	pF
CMOS logic output	1mA load		
Voltage			
Logic 1		2.8	V
Logic 0		0.4	V

Power supply current				
DVDD_I/O (3.3V) pin power consumption	QDUC mode		18	mA
DVDD (1.8V) pin power consumption	QDUC mode		615	mA
AVDD (3.3V) pin power consumption	QDUC mode		29	mA
AVDD (1.8V) pin power consumption	QDUC mode		109	mA
Power consumption				
Single-frequency mode			810	mW
Continuous modulation 8x interpolation		1415	1820	mW
Inverse Sinc filter power consumption		155	208	mW
Deep sleep mode		15	30	mW



Pin Function Table

Pin name	PIN number	Function	Description
NC	1/24/61/72/86/87/93/97 to 100		No connection. Device pins are allowed to float.
PLL_LOOP_FILTER	2	Input	PLL loop filter compensation.
A_{VDD} (1.8V)	3, 6, 89, 92	Input	Analog core VDD. 1.8 V analog power supply.
A_{VDD} (3.3V)	74, 75, 76, 77, 83	Input	Analog DAC VDD. 3.3 V analog power supply.
D_{VDD} (1.8V)	17, 23, 30, 47, 57, 64	Input	Digital core VDD. 1.8 V digital power supply.
D_{VDD}_I/O (3.3V)	11, 15, 21, 28, 45, 56, 66	Input	Digital input/output VDD. 3.3 V digital power supply.
A_{GND}	4, 5, 73, 78, 79, 82, 85, 88, 96	Input	Analog ground
D_{GND}	13, 16, 22, 29, 46, 58, 62, 63, 65	Input	Digital ground
SYNC_IN+	7	Input	Synchronization signal, digital input (rising edge valid). The external host's synchronization signal synchronizes the internal subclocks.
SYNC_IN-	8	Input	Synchronization signal, digital input (falling edge active). The external host's synchronization signal synchronizes the internal subclocks.
SYNC_OUT+	9	Output	Synchronization signal, digital output (rising edge valid). The internal device's subclock synchronization signal synchronizes with the external slave device.
SYNC_OUT-	10	Output	Synchronization signal, digital output (falling edge active). The internal device's subclock synchronization signal synchronizes with the external slave device.
SYNC_SMP_ERR	12	Output	Synchronization sampling error, digital output (active high). A high level on this pin indicates that the chip has not received a valid SYNC_IN+/SYNC_IN synchronization signal.
MASTER_RESET	14	Input	Host reset, digital input (active high). This pin clears all memory elements to 0 and sets registers to their default values.
EXT_PWR_DWN	18	Input	External power-saving mode, digital input (active high). A high level on this pin enables the currently programmed power-saving operation mode. If not used, it should be grounded.
PLL_LOCK	19	Output	PLL Lock-in, Digital Output (Active High). A high level on this pin indicates that the clock multiplier PLL has locked the reference clock input.

CCI_OVFL	20	Output	CCI Overflow Digital Output, Active High. A high level on this pin indicates that the CCI filter has overflowed. This pin will remain high until the CCI overflow condition is cleared.
D<17:0>	25, 26, 27, 31, 32, 33, 34, 35, 36, 37, 38, 39, 42, 43, 44, 48, 49, 50	Input/ Output	Parallel data input bus (active high). These pins provide interleaved 18-bit digital I and Q vectors to the modulator for up-conversion. They can also be used as GPIO ports in Blackfin interface mode.
SPORT I-DATA	42	Input	In Blackfin interface mode, this pin serves as an I-channel serial data input.
SPORT Q-DATA	43	Input	In Blackfin interface mode, this pin serves as the Q-channel data serial input.
PDCLK	40	Output	Parallel data clock, digital output (clock).
TxENABLE /FS	41	Input	Send enable, digital input (active high). FS input: In Blackfin interface mode, this pin is used as the FS input to receive the RFS output signal from Blackfin.
RT	51	Input	RAM flip-flop, digital input (active high). This pin provides control for the RAM amplitude adjustment function. When using this function, a high level scans the amplitude from the start RAM address to the end address. A low level scans the amplitude from the end RAM address to the start address. If not used, it should be grounded or connected to a power supply.
PROFILE<2:0>	52, 53, 54	Input	Profile selection pins, digital inputs (active high). These pins are used to select one of the eight phase/frequency characteristics (single tone or carrier tone) of the DDS core. By changing the state of one of these pins, all current I/O buffer contents can be transferred to the corresponding register. To change the state, the signal on the SYNC_CLK pin needs to be referenced to establish the signal.
SYNC_CLK	55	Output	Output system clock/4, digital output (clock). The I/O_UPDATE and PROFILE<2:0> pin signals are based on this signal.
I/O_UPDATE	59	Input/ Output	Input/output update; digital input or output (active high), depending on the internal I/O update valid bit. A high level on this pin indicates that the contents of the I/O buffer will be transferred to the corresponding internal register.
OSK	60	Input	Output shift keying, digital input (active high). This pin controls the OSK function when using OSK (manual or automatic). When OSK is not in use, this pin is connected to a high level.
SDIO	67	Input/ Output	Serial data input/output, digital input/output (active high). Depending on the configuration, this pin supports both unidirectional and bidirectional (default) modes. In bidirectional serial port mode, this pin can be used for both serial data input and output. In unidirectional mode, only data input is supported.
SDO	68	Output	Serial data output, digital output (active high). This pin is only valid in unidirectional serial data mode for data output. In bidirectional mode, this pin is inactive and should be left floating.
SCLK	69	Input	Serial data clock. Digital clock (write operation on rising edge, read operation on falling edge). This pin provides the serial data clock that controls the data path. Chip write operations use the rising edge, and readback operations use the falling edge.
CS	70	Input	Chip select, digital input (active low). A low level on this pin enables the chip to detect the rising/falling edge of the serial clock. A high level on this pin enables the chip to ignore the serial data input.
I/O_RESET	71	Input	Input/output reset, digital input (active high). When this pin goes high during a communication cycle failure, it does not reset the entire device; instead, it resets the serial port controller's state machine and clears any I/O buffers written since the last I/O update. When not in use, this pin should be grounded to prevent accidental resets.
I_{OUT}	80	Output	Open-source DAC complementary output current source. Analog output, current mode. Connected to AGND via a 50 Ω resistor.
I_{OUT}	81	Output	Open-source DAC output current source. Analog output, current mode. Connected to AGND via a 50 Ω resistor.
DAC_RSET	84	Output	Analog reference pin. This pin is programmed to provide the full-scale reference current for the DAC output. Connect it to AGND via a 10kΩ resistor.
REF_CLK	90	Input	Reference clock input. Analog input.
REF_CLK	91	Input	Complementary reference clock input. Analog input.
REFCLK_OUT	94	Output	Reference clock output. Analog output.
XTAL_SEL	95	Input	Crystal selection.

Serial I/O timing diagram

The following four diagrams provide some basic examples illustrating the timing relationships between various control signals of a serial I/O port. Most bits in the register diagram are not transferred to their internal destination address before the I/O update is set, a fact not reflected in the timing diagrams below.

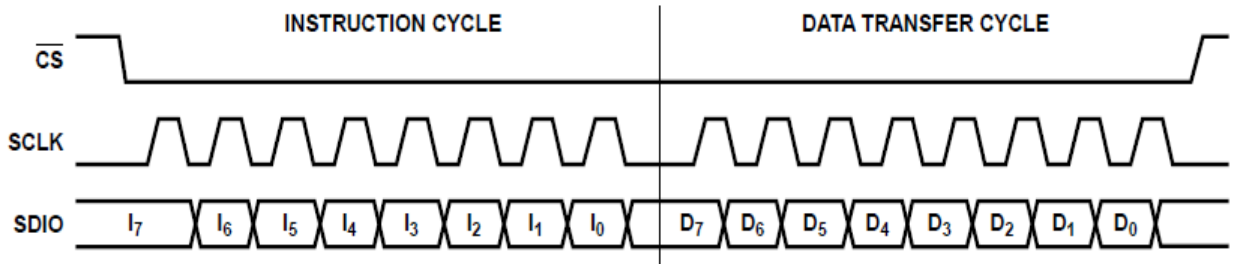


Figure 1. Serial port write timing – clock idle is low

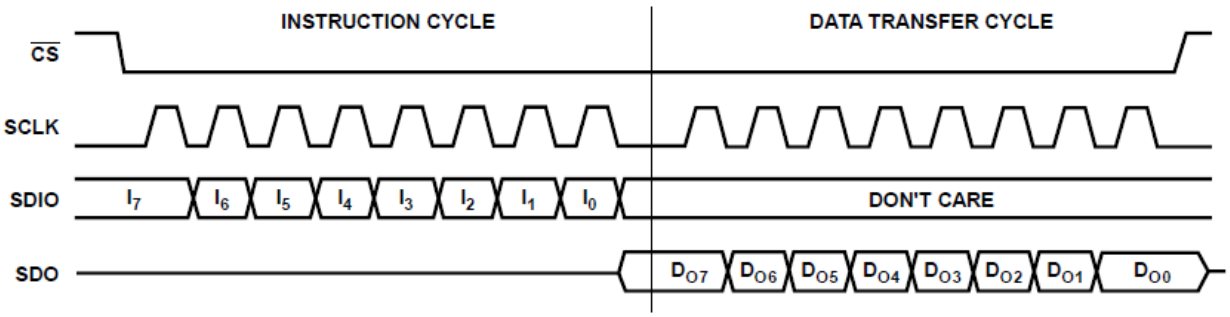


Figure 2. Three-wire serial port read timing – clock idle is low

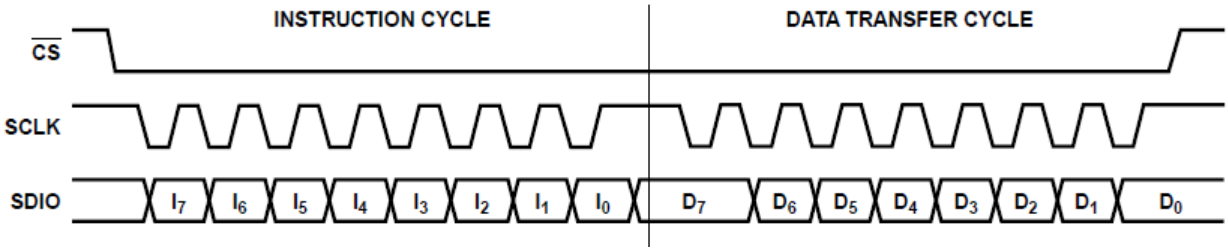


Figure 3. Serial port write timing – clock idle is high

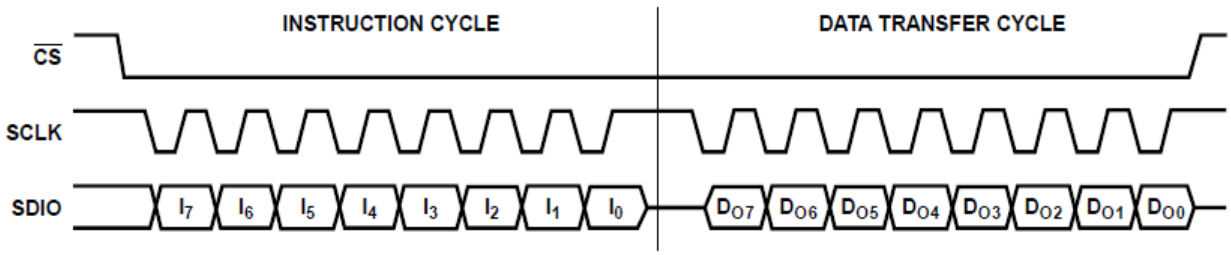


Figure 4. Two-wire serial port read timing – clock idle is high

Register mapping

Please note that the maximum number in each register bit field column is the MSB, and the minimum number is the LSB of that register, as shown in the table below.

Register name and address	Bit address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default value
CFR1 - Control Function Register 1(0x00)	31:24	RAM Enable	open circuit		RAM playback destination	open circuit		Work mode		0x00
	23:16	Manual OSK external control	Inverse Sinc filter enable	CCI Reset	open circuit				Select DDS sine wave output	0x00
	15:8	open circuit		Automatic zeroing phase accumu-lator	open circuit	Zero-phase accumu-lator	Loading ARR@ I/O updates	OSK Enable	Select Automatic OSK	0x00
	7:0	Digital part off	DAC power failure	REFCLK input power failure	Auxiliary DAC off	External shutdown control	Automatic shutdown enable	SDIO only Input	LSB priority	0x00
CFR2 - Control Function Register 2(0x01)	31:24	Blackfin interface mode is valid.	Blackfin bit order	Blackfin Early Frame Sync Enable	open circuit				Use the Profile register as an ASF source	0x00
	23:16	Internal I/O update is valid	SYNC_CLK Enable	open circuit					Read valid FTW	0x40
	15:8	I/O update rate control		PDCLK Rate Control	Data format	PDCLK Enable	PDCLK reverse	TXEnable reverse	Q Priority data pairing	0x08
	7:0	Delayed matching Enable	The data allocator retains the last value.	Synchroni zation Timing Verificatio n disabled	open circuit					0x20
CFR3 - Control Function Register 3(0x02)	31:24	open circuit		DRV0[1:0]		open circuit	V_{CO} SEL<2:0>			0x1F
	23:16	open circuit		ICP[2:0]			open circuit			0x3F
	15:8	REFCLK Crossover Bypass	REFCLK Input Crossover Reset B	open circuit					PLL Enable	0x40
	7:0	N[6:0]							open circuit	0x00
Auxiliary DAC Control Register (0x03)	31:24	open circuit								0x00
	23:16	open circuit								0x00
	15:8	open circuit								0x7F
	7:0	FSC[7:0]								0x7F

I/O update rate register (0x04)	31:24	I/O update rate [31:24]			0xFF
	23:16	I/O update rate [23:16]			0xFF
	15:8	I/O update rate [15:8]			0xFF
	7:0	I/O update rate [7:0]			0xFF
RAM segment Register 0 (0x05)	47:40	RAM address step rate 0 < 15:8 >			
	39:32	RAM address step rate 0 < 7:0 >			
	31:24	RAM end address 0<9:2>			
	23:16	RAM end address 0<1:0>	open circuit		
	15:8	RAM start address 0<9:2>			
	7:0	RAM starting address 0<1:0>	open circuit	RAM playback mode 0<2:0>	
RAM segment Register 1 (0x06)	47:40	RAM address step rate 1 <15:8>			
	39:32	RAM address step rate 1 <7:0>			
	31:24	RAM end address 1<9:2>			
	23:16	RAM end address 1<1:0>	open circuit		
	15:8	RAM start address 1<9:2>			
	7:0	RAM start address 1<1:0>	open circuit	RAM playback mode 1<2:0>	
Amplitude scaling factor (ASF) Register (0x09)	31:24	Amplitude slope ratio <15:8>			0x00
	23:16	Amplitude slope ratio <7:0>			0x00
	15:8	Amplitude scaling factor <13:6>			0x00
	7:0	Synchronization state preset value <5:0>	open circuit		0x00

Register name and address	Bit address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default value
Multi-chip synchronization register (0x0A)	31:24	Synchronous verification delay <3:0>			Synchronous receiver enable	Synchronizer enable	Synchronizer polarity		open circuit	0x00
	23:16	Synchronization state preset value <5:0>					open circuit			0x00
	15:8	Synchronizer delay <4:0>				open circuit				0x00
	7:0	Synchronization receiver delay <4:0>				open circuit				0x00
Profile0 Register - Single Tone (0x0E)	63:56	open circuit		Amplitude scaling factor <13:8>						N/A
	55:48	Amplitude scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile0 Register QDUC (0x0E)	63:56	CCI interpolation rate <7:2>						Spectrum Inversion	Anti-CCI bypass	N/A
	55:48	Output scaling factor								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile1 Register - Single Tone (0x0F)	63:56	open circuit		Amplitude scaling factor <13:8>						N/A
	55:48	Amplitude scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile 1 Register QDUC (0x0F)	63:56	CCI interpolation rate <7:2>						Spectrum Inversion	Anti-CCI bypass	N/A
	55:48	Output scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile2 Register - Monotone (0x10)	63:56	open circuit		Amplitude scaling factor <13:8>						N/A
	55:48	Amplitude scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A

Register name and address	Bit address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default value
Profile 2 Register QDUC (0x10)	63:56	CCI interpolation rate <7:2>						Spectrum Inversion	Anti-CCI bypass	N/A
	55:48	Output scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile3 Register - Single Tone (0x11)	63:56	open circuit		Amplitude scaling factor <13:8>						N/A
	55:48	Amplitude scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile 3 Register QDUC (0x11)	63:56	CCI interpolation rate <7:2>						Spectrum Inversion	Anti-CCI bypass	0x00
	55:48	Output scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile4 Register - Monotone (0x12)	63:56	open circuit			Amplitude scaling factor <13:8>					N/A
	55:48	Amplitude scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile 4 Register QDUC (0x12)	63:56	CCI interpolation rate <7:2>						Spectrum Inversion	Anti-CCI bypass	N/A
	55:48	Output scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile5 Register - Single Tone (0x13)	63:56	open circuit		Amplitude scaling factor <13:8>						N/A
	55:48	Amplitude scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A

Register name and address	Bit address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default value
Profile 5 Register QDUC (0x13)	63:56	CCI interpolation rate <7:2>						Spectrum Inversion	Anti-CCI bypass	N/A
	55:48	Output scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile6 Register - Single Tone (0x14)	63:56	open circuit		Amplitude scaling factor <13:8>						N/A
	55:48	Amplitude scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile 6 Register - QDUC (0x14)	63:56	CCI interpolation rate <7:2>						Spectrum Inversion	Anti-CCI bypass	N/A
	55:48	Output scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile7 Register - Single Tone (0x15)	63:56	open circuit		Amplitude scaling factor <13:8>						N/A
	55:48	Amplitude scaling factor <7:0>								N/A
	47:40	Phase offset word <15:8>								N/A
	39:32	Phase offset word <7:0>								N/A
	31:24	Frequency tuning word <31:24>								N/A
	23:16	Frequency tuning word <23:16>								N/A
	15:8	Frequency tuning word <15:8>								N/A
	7:0	Frequency tuning word <7:0>								N/A
Profile7 Register - QDUC (0x15)	63:56	CCI interpolation rate <7:2>						Spectrum Inversion	Anti-CCI bypass	
	55:48	Output scaling factor <7:0>								
	47:40	Phase offset word <15:8>								
	39:32	Phase offset word <7:0>								
	31:24	Frequency tuning word <31:24>								
	23:16	Frequency tuning word <23:16>								
	15:8	Frequency tuning word <15:8>								
	7:0	Frequency tuning word <7:0>								
RAM register (0x16) GPIO configuration register (0x18) GPIO Data Register (0x19)	63:56	RAM word <31:0>								
	55:48	GPIO Configuration <15:0>								
	47:40	GPIO data <15:0>								

Register bit function description

The serial I/O port registers range from 0 to 25 (hexadecimal: 0x00 to 0x19), totaling 26 registers. However, six of these registers are unused, leaving only 20 usable registers. The unused registers are 7, 8, 11 through 13, and 23 (0x07 to 0x08, 0x0B to 0x0D, and 0x17). The number of bytes allocated to each register varies. That is, registers have different depths, and their byte capacity depends on specific functional requirements. Furthermore, registers are primarily named according to their function. Sometimes, registers are named based on ease of memorization. For example, the register at serial address 0x00 is named Control Function Register 1, represented as the easily memorable CFR1. The following section details the function of each bit in the chip register map. When multiple bits work together to implement a specific function, the entire bit group is treated as a single binary word and described collectively. This section is organized according to the register's serial address order. Each subheading is followed by a description of the function of each bit in that specific register. The specific location of a bit in a register is indicated by <A> or <A:B>, where A and B are bit numbers. The <A:B> notation specifies the range of bits from the most significant bit to the least significant bit. For example, <5:2> indicates bits 5 to 2, where bit 0 represents the register's LSB. Unless otherwise specified, programmed bits are not transferred to the internal destination location until an I/O update is set or the profile is changed.

Control Function Register 1 (CFR1) - Address 0x00. This register is allocated four bytes.

Bit	Pin Name	Description
31	RAM Enable	0 : Disable RAM playback (default). 1 : Enable RAM playback.
30:29	Open circuit	
28	RAM playback destination	It is only valid when CFR1<31>=1. 0 : RAM playback data is routed to the baseband adjustment multiplier (default). 1 : RAM playback data is routed to the baseband I/Q data path.
27:26	Open circuit	
25:24	Work mode	00 : Quadrature modulation mode (default). 01: Monotone mode. 1x: DAC interpolation mode.
23	Manual OSK external control	Only valid when CFR1<9:8>=10b. 0 : OSK pin disabled (default). 1 : OSK pin enabled for manual OSK control.
22	Inverse Sinc filter enable	0 : The inverse sinc filter is bypassed (default). 1: The inverse sinc filter is enabled.
21	CCI cleared	The serial I/O port controller will automatically clear this bit to 0. This operation requires several internal clock cycles to complete, during which time data applied to the CCI input by the baseband signal chain will be ignored. Forcing the input to all zeros clears the CCI data path, after which the CCI accumulator will be reset. 0 : The CCI filter is working normally (default). 1 : Enables asynchronous reset of the accumulator in the CCI filter.
20:17	open circuit	
16	Select DDS sine output	Only valid when CFR1<25:24>=01b. 0 : Select DDS cosine output (default). 1 : Select DDS sine output.
15:14	Open circuit	
13	Automatic phase reset	0 : The DDS phase accumulator is working normally (default).
12	Open circuit	
11	Clear phase accumulator	0 : The DDS phase accumulator is working normally (default). 1 : The DDS phase accumulator is asynchronously and statically reset.
1 0	Loading ARR@I/O updates	0 : OSK amplitude ramp rate timer is working normally (default). 1 : The OSK amplitude ramp rate timer is reloaded each time I/O_UPDATE is set or the profile is changed.
9	OSK (Output Shift Keying) Enable	0 : OSK disabled (default). 1 : OSK enabled.
8	Select Automatic OSK	Only valid when CFR1<9>=1. 0: Manual OSK enable (default). 1 : Automatic OSK enable.
7	Digital part off	This bit takes effect without I/O updates. 0 : Digital core clock signal is enabled (default). 1 : Digital core clock signal is disabled.
6	DAC shutdown	0 : DAC clock signal and bias circuit are enabled (default). 1 : DAC clock signal and bias circuit are disabled.
5	REFCLK input off	This bit takes effect without I/O updates. 0 : REFCLK input circuit and PLL are enabled (default). 1 : REFCLK input circuit and PLL are disabled.
4	Auxiliary DAC shutdown	0 : Auxiliary DAC clock signal and bias circuit are enabled (default). 1 : Auxiliary DAC clock signal and bias circuit are disabled.
3	External shutdown control	0 : The EXT_PWR_DWN pin is set to operate in full power mode (default). 1 : Setting the EXT_PWR_DWN pin enables fast recovery power saving mode operation.

2	Automatic shutdown enable	It is invalid when CFR1<25:24>=01b. 0 : Disable shutdown (default). 1 : When the TxEnable pin is logic 0 , the baseband signal processing chain will clear residual data, and the clock will automatically stop. When the TxENABLE pin is logic 1, the clock will restart.
1	SDIO input only	0 : Configures the SDIO pin for bidirectional operation; two-wire serial programming mode (default). 1: Configure the serial data I/O pin (SDIO) as an input pin only, in a three-wire serial programming mode.
0	LSB priority	0 : Configure the serial I/O port to MSB priority format (default). 1 : Configure the serial I/O port to LSB priority format.

Control Function Register 2 (CFR2) at address 0x01 (this register is allocated four bytes).

Bit	Pin Name	Description
31	Blackfin interface mode is valid.	Only valid when CFR1<25:24>=00b (quadrature modulation mode). 0 : Pin D<17:0> is configured as an 18-bit parallel port (default). 1 : Pins D<5:4> are configured as dual serial ports compatible with the Blackfin serial interface. Pins D<17:6> and D<3:0> become 16-bit GPIO ports.
30	Blackfin bit order	It is only valid when CFR2<31>=1. 0 : Dual serial port (BFI) configured with MSB priority (default). 1 : Dual serial port (BFI) configured with LSB priority.
29	Blackfin Early Frame Synchronization Enable	It is only valid when CFR2<31>=1. 0 : Dual Serial Port (BFI) configured for Blackfin late frame synchronization (default). 1 : Dual Serial Port (BFI) configured for Blackfin early frame synchronization.
28:25	open circuit	
24	Use the Profile register as an ASF source	Only valid when CFR1<25:24>=01b (single-frequency modulation mode) and CFR1<9>=0 (OSK disabled). 0 : Amplitude scaling factor is bypassed (unity gain). 1 : The profile register is valid and determines the amplitude scaling factor.
23	Internal I/O update is valid	This bit takes effect without I/O updates. 0 : Serial I/O programming is synchronized with the external I/O_UPDATE pin being set, which is configured as an input pin (default). 1 : Serial I/O programming is synchronized with internally generated I/O update signals (interna signals are generated on the I/O_UPDATE pin configured as an output pin).
22	Enable SYNC_CLK	0 : SYNC_CLK pin disabled; static logic 0 output. 1 : The SYNCCLK pin generates a 1/4fSYSCLK clock signal, used to synchronize the serial I/O ports (default).
21:17	Open circuit	
16	Read valid FTW	0 : The serial I/O port read operation of the FTW register reads the contents of the FTW register (default). 1 : The serial I/O port read operation of the FTW register reads the actual 32-bit control word on the input DDS phase accumulator.
15:14	I/O update rate control	Only valid when CFR2<23>=1. Sets the prescaler value for the reference I/O update timer: 00=1 division (default), 01=2 division, 10=4 division, 11=8 division.
13	PDCLK rate control	It is only valid when CFR2<31>=0 and CFR1<25:24>=00b. 0 : PDCLK operates at the input data rate (default). 1 : PDCLK operates at % of the input data rate; this helps maintain consistency between the I/Q words on the parallel data port and the internal clocks of the baseband signal processing chain.
12	Data format	0 : Data words applied to pins D<17:0> are encoded in two's complement binary format (default). 1: Data words applied to pins D<17:0> are encoded in offset binary format.
11	PDCLK Enable	0 : The PDCLK pin is disabled and forced to static logic 0 ; the internal clock signal will run continuously to provide timing for the data distributor. 1 : An internal PDCLK signal appears on the PDCLK pin (default).
10	PDCLK inversion	0 : PDCLK normal polarity; Q data is related to logic 1; I data is related to logic 0 (default). 1 : PDCLK reverse polarity.

9	TxEnable invert	0 : TxENABLE normal polarity; logic 0 indicates standby state, while logic 1 indicates transmission state (default). 1 : TxENABLE reverses polarity; logic 0 indicates transmission state, while logic 1 indicates standby state.
8	Q-priority data pairing	0 : I/Q data pairs are transmitted in I data first, followed by Q data (default). 1 : I/Q data pairs are transmitted in Q data priority, followed by I data.
7	Match Delay Enable	0 : DDS amplitude, phase and frequency changes are applied synchronously and output in the listed order (default). 1 : Synchronous output of DDS amplitude, phase and frequency changes.
6	The data allocator retains the last value.	It is invalid when CFR1<25:24>=01b. 0 : When the TxENABLE pin is in a logic false state, the data distributor ignores the input data and internally forces the baseband signal path to zero (default). 1 : When the TxENABLE pin is in a logic false state, the data distributor ignores the input data and internally forces the retention of the last value received on the baseband signal path.
5	Synchronous timing verification disabled	0 : Enables setup and hold verification circuitry to perform measurements; measurement results appear on the SYNC_SMP_ERR pin; if this pin is logic 1, it indicates that setup/hold verification may be in progress; while logic 0 indicates that setup/hold verification has not been detected; the measurement results will be latched and held until this bit is set to logic 1. 1 : Reset the setup and hold verification measurement circuit, forcing the SYNC_SMP_ERR pin to Input static logic 0 state (default); the measurement circuit is disabled until this bit returns to logic 0 state.
4:0	Open circuit	

Control Function Register 3 (CFR3) at address 0x02 (this register is allocated four bytes).

Bit	Pin Name	Description
31:30	Open circuit	
29:28	DRVO	Controls the REFCLK_OUT pin; the default value is 01b.
27	Open circuit	
26:24	VCO SEL	Select the frequency band for REFCLK PLL VCO; the default value is 111b.
23:22	Open circuit	
21:19	ICP	Select the charge pump current value in REFCLK PLL; the default value is 111b.
18:16	Open circuit	
15	REFCLK Input frequency divider bypass	0 : Select the input divider (default). 1 : The input divider is bypassed.
14	REFCLK Input frequency divider reset B	0 : The input divider is reset. 1 : The input divider is working normally (default).
13:9	Open circuit	
8	PLL Enable	0 : REFCLK PLL is bypassed (default). 1 : REFCLK PLL is enabled.
7:1	N	This 7-digit number is the division modulus of the REFCLK PLL feedback divider, with a default value of 0000000b.
0	Open circuit	

The auxiliary DAC control register is located at address 0x03 (this register is allocated four bytes).

Bit	Pin Name	Description
31:8	Open circuit	
7:0	FSC	This 8-bit number is used to control the full-scale output current of the main DAC; the default value is 0XFF.

The I/O update rate register is located at address 0x04 (this register is allocated four bytes. This register is effective without I/O updates.)

Bit	Pin Name	Description
31: 0	I/O update rate	Valid only when CFR2[23]=1. This 32-bit number controls the automatic /O update rate, with a default value of 0xFFFFFFFF.

RAM segment register 0 has an address of 0x05 and is allocated six bytes. This register takes effect without I/O updates. It is only valid when CFR1<31> = 1 and the RT pin is in a logic 0 to logic 1 transition.

Bit	Pin Name	Description
47:32	RAM address step rate	This 16-bit control RAM state machine sets the step rate within a specified RAM address range.
31:22	RAM end address	This 10-bit number determines the end address of the RAM state machine.
21:16	open circuit	
15:6	RAM start address	This 10-bit number determines the starting address of the RAM state machine.
5:3	open circuit	
2:0	RAM playback mode 0	This 3-digit number determines the playback mode of the RAM state machine.

RAM segment register 1 has an address of 0x06 and is allocated six bytes. This register is only valid when CFR1<31> = 1 and the RT pin is in a logic 1 to logic 0 transition.

Bit	Pin Name	Description
47:32	RAM address step rate 1	This 16-bit control RAM state machine sets the step rate within a specified RAM address range.
31:22	RAM end address 1	This 10-bit number determines the end address of the RAM state machine.
21:16	open circuit	
15:6	RAM start address 1	This 10-bit number determines the starting address of the RAM state machine.
5:3	open circuit	
2:0	RAM playback mode 1	This 3-digit number determines the playback mode of the RAM state machine.

The Amplitude Scale Factor (ASF) register has an address of 0x09 and is allocated four bytes. This register is only valid when CFR1<9> = 1.

Bit	Pin Name	Description
31:16	Amplitude slope	Valid only when CFR1<8>=1. This 16-bit number controls the rate at which the OSK controller updates the DDS amplitude change.
15:2		If CFR1<8>=0 and CFR1<23>=0, then this 14-digit number is the amplitude scaling factor of the DDS. If CFR1<8>=0 and CFR1<23>=1, then when the OSK pin is logic 1, this 14-bit number is the amplitude scaling factor of DDS. If CFR1<8>=1, then this 14-digit number sets the upper limit of the maximum allowable amplitude scaling factor of the DDS.
1:0	Amplitude step size	This is only valid when CFR1<8>=1. This 2-digit number controls the step size of the DDS amplitude variation (see Table 4).

The address of the multi-chip synchronization register is 0x0A, and this register is allocated four bytes.

Bit	Pin Name	Description
31:28	Synchronous verification delay	The default value is 0000b. This 4-digit number sets the timing skew (approximately 150 ps increment) between the SYSCLK and delayed SYNC_IN signals of the synchronization verification module in the synchronization receiver.
27	Synchronous receiver enable	0 : Synchronous clock receiver disabled (default). 1: Synchronous clock receiver enabled.
26	Synchronizer enable	0 : Synchronous clock generator disabled (default). 1: Synchronous clock generator enabled.
25	Synchronizer polarity	0 : The synchronous clock generator is synchronized with the rising edge of the system clock (default). 1: The synchronous clock generator is synchronized with the falling edge of the system clock.
24	Open circuit	
23:18	Synchronization state preset value	The default value is 000000b. This 6-bit number represents the assumed state when the internal clock generator receives a synchronization pulse.
17:16	Open circuit	
15:11	Output Synchronizer Delay	The default value is 00000b. This 5-digit number sets the output delay of the synchronization generator (in increments of approximately 150 ps).
10:8	Open circuit	
7:3	Input synchronization receiver delay	The default value is 00000b. This 5-digit number sets the synchronization receiver input delay (in increments of approximately 150 ps).
2:0	Open circuit	0 = Normal operation (default). 1 = Phase detector disabled.

Profile Register

The device profile uses eight consecutive serial I/O addresses (0x0E to 0x15). These eight profile registers are divided into single-frequency modulation (DDS) profile and QDUC profile, depending on the device operating mode specified by CFR1<25:24>. During operation, the valid profile register is determined using the external PROFILE<2:0> pins. Single-frequency modulation profile controls: DDS frequency (32-bit), DDS phase offset (16-bit), and DDS amplitude adjustment (14-bit). QDUC profile controls: DDS frequency (32-bit), DDS phase offset (16-bit), output amplitude adjustment (8-bit), CCI filter interpolation factor, inverse CCI bypass, and spectrum inversion. The QDUC profile is also selectively applicable to DAC interpolation operating mode: only output adjustment, CCI filter interpolation factor, and inverse CCI bypass apply; all other parts (DDS frequency, output amplitude adjustment, and spectrum inversion) are ignored.

The Profile<7:0> register has single-frequency modulation addresses from 0x0E to 0x15 and is allocated eight bytes.

Bit	Pin Name	Description
63:62	open circuit	
61:48	Amplitude scaling factor	This 14-bit control controls the DDS output amplitude.
47:32	Phase offset word	This 16-bit number controls the DDS phase offset.
31:0	Frequency tuning word	This 32-bit control controls the DDS frequency.

Profile<7:0> register — QDUC — addresses 0x0E to 0x15, and this register is allocated eight bytes.

Bit	Pin Name	Description
63:58	CCI interpolation rate	This 6-bit is the rate interpolation factor for the CCI filter.
57	Spectrum Inversion	0 : The modulator output adopts the following format: I(t) × cos(ct) – Q(t) × sin(ct). 1 : The modulator output adopts the following format: I(t) × cos(ct) + Q(t) × sin(ct).
56	Anti-CCI bypass	0 : Inverse CCI filter enabled. 1: Inverse CCI filter bypassed.
55:48	Output scaling factor	This 8-bit controls the output amplitude.
47:32	Phase offset word	This 16-bit controls the DDS phase offset.
31:0	Frequency tuning word	This 32-bit controls the DDS frequency.

RAM register — address 0x16, and this register is allocated four bytes.

Bit	Pin Name	Description
31:0	RAM word	The 32-bit word written to RAM is defined by the start and end addresses of RAM segment register 0 or RAM segment register 1.

GPIO Configuration Register — Address 0x18, and this register is allocated two bytes.

Bit	Pin Name	Description
15:0	GPIO Configuration	See Table 5 for details.

GPIO data register — address 0x19, and this register is allocated two bytes.

Bit	Pin Name	Description
15:0	GPIO Configuration	Read or write the contents of the GPIO-based configuration registers. See Table 5 for details.

Table 3 REFCLK_OUT Buffer Control

CFR3<29:28>	REFCLK_OUT buffer
00	Disable
01	Low output current
10	Output current
11	High output current

Table 4 VCO Range Bit Settings

VCO SEL position (CFR3<26:24>)	VCO range
000	VCO0
001	VCO1
010	VCO2
011	VCO3
100	VCO4
101	VCO5
110	PLL bypassed
111	PLL bypassed

Table 5 PLL charge pump current

CFR3<29:28>	REFCLK_OUT buffer
000	212
0 01	237
0 10	262
0 11	287
1 00	312
101	337
110	363
111	387

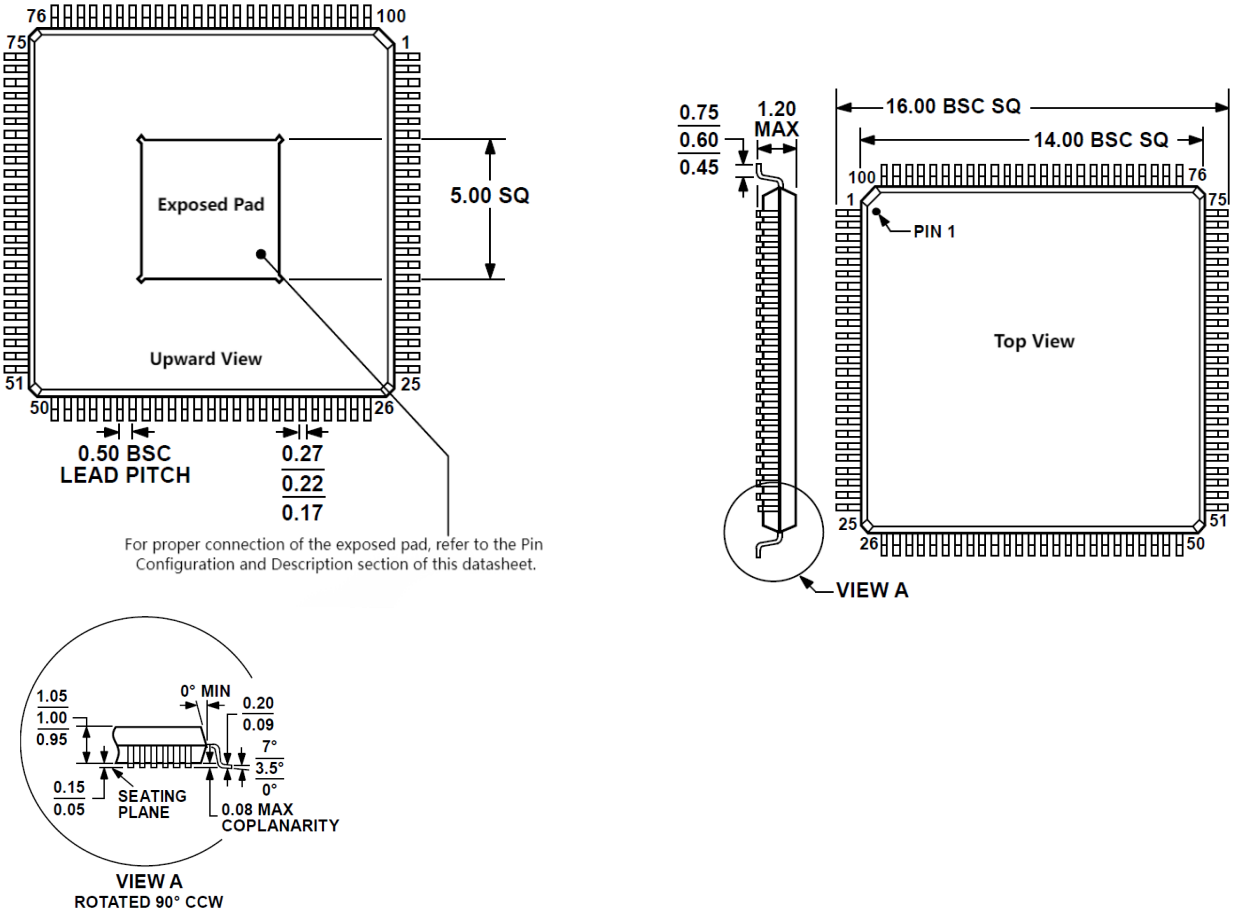
Table 6 OSK Amplitude Step Size

ASF<1:0>	Amplitude step size
00	1
01	2
10	4
11	8

Table 7 GPIO Pins and Configuration and Data Register Bits

Pin marking	Configuration bit	Data bits
D17	15	15
D16	14	14
D15	13	13
D14	12	12
D13	11	11
D12	10	10
D11	9	9
D10	8	8
D9	7	7
D8	6	6
D7	5	5
D6	4	4
D3	3	3
D2	2	2
D1	1	1
D0	0	0

Outline dimensions and packaging



100-pin exposed pad, ultra-thin quad flat package [TQFP_EP](SV-100-4) Dimensions (unit: mm)

YMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.19	--	0.27
b1	0.18	0.20	0.23
c	0.13	--	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	--	15.35
e	0.50 BSC		

Device ordering information

Product Model	Temperature range	Packaging	Package	RoHS
DAD9957	-40°C to +85°C	TQFP-100	90/tray	Y