

Characteristics

- High dynamic range, dual DAC
- Low noise and intermodulation distortion
- Single-carrier W-CDMA ACLR = 80dBc (61.44MHz intermediate frequency)
- The innovative switching output stage enables usable outputs exceeding the Nyquist frequency.
- LVDS inputs operate in dual-port or optional interleaved single-port mode.
- be programmed from 8.6mA to 31.7mA full scale.
- The auxiliary 10-bit current DAC has source current/sink current capability to eliminate external current. Disequilibrium Zero
- Internally integrated 1.2V precision reference source
- Operating power supply: 1.8V ~ 3.3V
- Power consumption: 320 mW
- Small size, lead-free, 72-pin QFN package

Application Areas

- Wireless infrastructure: WCDMA, CDMA2000, TD-SCDMA, WiMAX
- Broadband communication: LMDS/MMDS, point-to-point
- Instrumentation: Radio frequency (RF) signal generators, arbitrary waveform generators

Overview

The DAD9783 features high dynamic range, 16-bit resolution, dual-channel digital-to-analog converter (DAC), and sampling rates up to 500 MSPS. These devices are well-suited for direct conversion transmission applications, including gain and offset compensation, and can be seamlessly integrated with analog quadrature modulators.

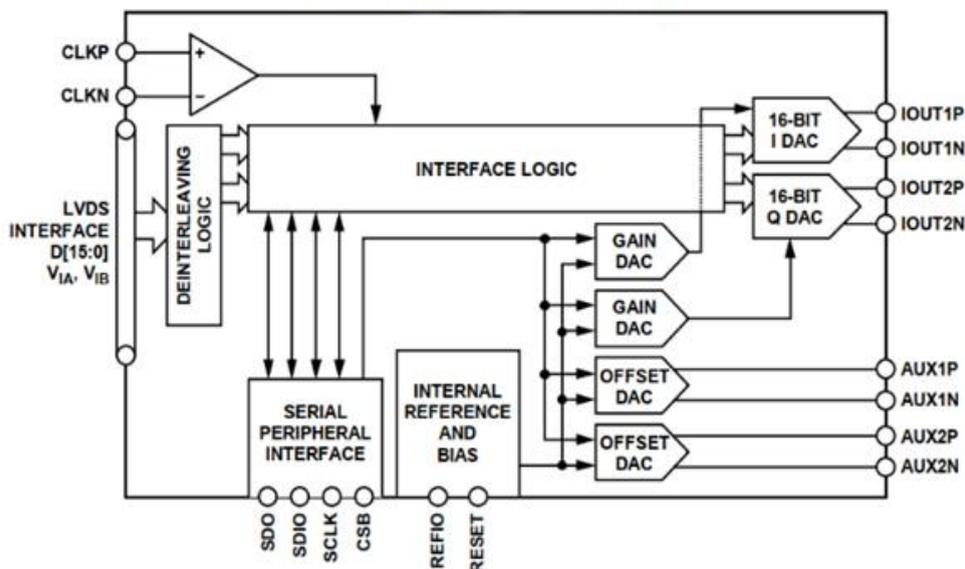
The proprietary dynamic output architecture can shift energy from the fundamental frequency to the image frequency, enabling analog outputs to be synthesized even above the Nyquist frequency.

Full programmability is available via the Serial Peripheral Interface (SPI) port, and some pin-programmable features are also provided for controllerless applications.

Product Features

1. Utilizing low noise and intermodulation distortion (IMD) characteristics enable high-quality synthesis of broadband signals.
2. Proprietary switch outputs can enhance dynamic performance.
3. Programmable current output and dual auxiliary DACs provide both flexibility and enhanced system functionality.

Functional Block Diagram



DAD9783 Dual-Channel, 16-Bit, 500 MSPS DAC with LVDS Interface

DC Characteristics

Unless otherwise noted, T_{min} to T_{max} , $AVDD33=3.3V$, $DVDD33=3.3V$, $AVDD18=1.8V$, $DVDD18=1.8V$, $I_{outfs} = 20mA$, maximum sampling rate.

Table 1.

Parameter	Min	Typ	Max	Unit
Resolution		16		Bits
Accuracy				
Differential nonlinearity (DNL)		± 2		LSB
Integral nonlinearity (INL)		± 4		LSB
Main DAC output				
Offset error	-0.001	0	+0.001	% FSR
Gain error (internal reference)		± 2		% FSR
Full-scale output current	8.66	20.2	31.66	mA
Output compliance voltage range	-1.0		+1.0	V
Output impedance		10		M Ω
Consistency				
DAC temperature drift				
Offset		0.04		ppm / $^{\circ}C$
Gain		100		ppm / $^{\circ}C$
Reference voltage		30		ppm / $^{\circ}C$
Auxiliary DAC output				
Resolution		10		Bits
Full-scale output current	-2		+2	mA
Output compliance range (Source)	0		1.6	mA
Output compliance range (Sink)	0.8		1.6	V
Output impedance		1		M Ω
Consistency				
Reference				
Internal reference voltage		1.2		V
Output impedance		5		k Ω
Analog power supply				
AVDD 33	3.13	3.3	3.47	V
CVDD 18	1.70	1.8	1.90	V
Digital power supply				
D VDD 33	3.13	3.3	3.47	V
D VDD 18	1.70	1.8	1.90	V
Power consumption				
fDAC = 500 MSPS, IF = 20 MHz		V \times I	V \times I	mW
fDAC = 500 MSPS, IF = 10 MHz			450	mW
Power-off mode		3	35	mW
Current				
A VDD 33		55	58	mA
C VDD 18		34	38	mA
DVDD 33		13	15	mA
DVDD 18		68	85	mA

DAD9783 Dual-Channel, 16-Bit, 500 MSPS DAC with LVDS Interface

Digital Specifications

Unless otherwise noted, T_{min} to T_{max} , AVDD33=3.3V, DVDD33=3.3V, AVDD18=1.8V, DVDD18=1.8V, Ioutfs =20mA maximum sampling rate.

Table 2.

Parameter	Min	Typ	Max	Unit
DAC clock inputs (CLKP, CLKN)				
Differential peak-to-peak voltage (CLKP - CLKN)	400	800	1,600	mV
Common mode voltage	300	400	500	mV
Maximum clock rate	500			MSPS
DAC clock to analog output data delay			7	Cycles
Serial peripheral interface				
Maximum clock frequency (SCLK) 40MHz			40	MHZ
Minimum pulse width high			12.5	ns
Low minimum pulse width			12.5	ns
Setup time, SDI to SCLK (tDS)	2.0			ns
Hold time, SDI to SCLK (tDH)	0.2			ns
Data valid, SDO to SCLK (tDV)	23			ns
Setup time, CSB to SCLK (tDCSB)		1.4		ns
Serial peripheral interface logic levels				
Input logic high 2.0 V	2.0			V
Low input logic			0.8	V
Serial peripheral interface logic levels				
Input voltage range, VIA or VIB 800 1600	800		1,600	mV
Input the difference threshold, WIDTH - 100 + 100	-100	20	+100	mV
Input differential hysteresis, WIDTHH to WIDTHL	80		120	Ω
Input differential input impedance	500			MSPS
Maximum LVDS input rate (per DAC)				

DAD9783 Dual-Channel, 16-Bit, 500 MSPS DAC with LVDS Interface

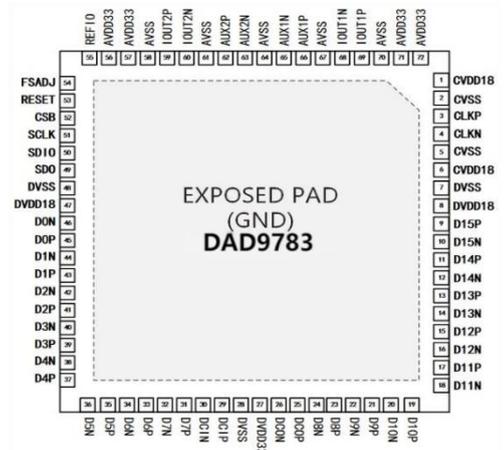
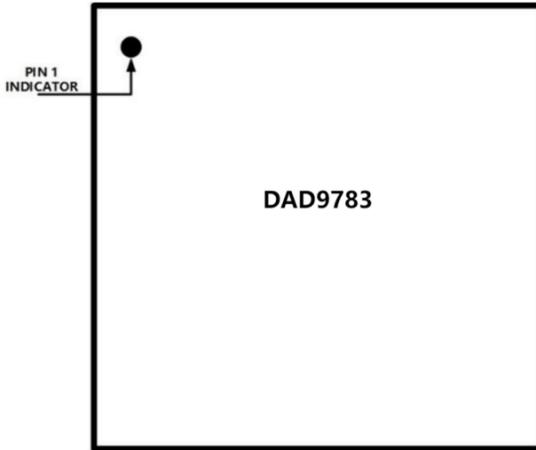
AC Specifications

Unless otherwise noted, T_{min} to T_{max} , AVDD33=3.3V, DVDD33=3.3V, AVDD18=1.8V, DVDD18=1.8V, Ioutfs = 20mA maximum sampling rate.

Table 3.

Parameter	Min	Typ	Max	Unit
Spurious-free dynamic range (SFDR)				
fDAC = 500 MSPS, IF = 20 MHz		81		dBc
fDAC = 500 MSPS, IF = 120 MHz		67.5		dBc
fDAC = 500 MSPS, IF = 380MHz (mixed mode)		62		dBc
fDAC = 500 MSPS, IF = 480MHz (mixed mode)		60		dBc
Second-order intermodulation distortion (IMD)				
fDAC = 500 MSPS, IF = 20 MHz		85.2		dBc
fDAC = 500 MSPS, IF = 120 MHz		79		dBc
fDAC = 500 MSPS, IF = 380MHz (mixed mode)		65		dBc
fDAC = 500 MSPS, IF = 480MHz (mixed mode)		66.5		dBc
Noise spectral density (NSD)				
fDAC = 500 MSPS, IF = 40 MHz		-165		dBc
fDAC = 500 MSPS, IF = 120 MHz		-157		dBc
fDAC = 500 MSPS, IF = 380MHz (mixed mode)		-154		dBc
fDAC = 500 MSPS, IF = 480MHz (mixed mode)		-153		dBc
Neighboring channel leakage ratio (NSD)				
single carrier				
fDAC = 491.52MSPS, IF = 20 MHz		-82		dBc
fDAC = 491.52MSPS, IF = 80 MHz		-81		dBc
fDAC = 491.52MSPS, IF = 411.52MHz		-69		dBc
fDAC = 491.52MSPS, IF = 471.52MHz		-70		dBc

Pin Definitions and Function Descriptions

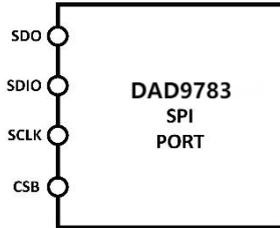


Pin No.	Symbol	Description
1, 6	CVDD18	Clock power supply voltage (1.8V)
2, 5	CVSS	Clock power circuit
3, 4	CLKP, CLKN	Differential DAC sampling clock input
7, 28, 48	DVSS	Digital ground
8,47	DVDD18	Digital power supply voltage (1.8V)
9 to 24, 32 to 46	D15P, D15N to D0P, D0N	LVDS data input, D15 is the MSB, D0 is the LSB
25, 26	DCOP, DCON	Differential data clock output, DAC sampling clock
27	DVDD33	Digital input and output pad ring voltage (3.3V)
29, 30	DCIP, DCIN	Differential data clock input aligned with input digital
49	SDO	Serial data output
50	SDIO	Serial data input (4-wire mode) or bidirectional serial data line (3-wire mode)
51	SCLK	Serial clock input
52	CSB	Serial clock input
53	RESET	Active-low chip select input
54	FS ADJ	Reset (active high)
55	REFIO	Full-scale current output adjustment
56, 57, 71, 72	AVDD33	Analog reference input/output (1.2V nominal)
58, 61, 64, 67, 70	AVSS	Analog power supply voltage
59	IOOUT2P	Analog ground
60	IOOUT2N	DAC current output: When all data bits are 1, it generates a full-scale current.
62, 63	AUX2P, AUX2N	The DAC uses complementary current output, which generates a full-scale current when all data bits are 0.
65, 66	AUX1P, AUX1N	Differential auxiliary DAC current output (channel 2)
68	IOOUT2N	Differential auxiliary DAC current output (channel 1)
69	IOOUT2P	The DAC uses complementary current output, which generates a full-scale current when all data bits are 0. DAC current output: When all data bits are 1, it generates a full-scale current.

Working Principle

The DAD9783 is suitable for both wired and wireless communication applications. Its dual- DAC architecture facilitates connection to quadrature modulators in single-sideband transmitter designs. Furthermore, its high-speed characteristics allow for wider bandwidth and the synthesis of more carriers, and further features and options can be implemented through SPI serial software programming.

Serial Peripheral Interface



The Serial Peripheral Interface (SPI) port is a flexible synchronous serial communication port that can connect to more peripheral devices such as microcontrollers. This port is compatible with most synchronous transmission formats, including SPI and SSR protocols.

Users can read and write to the DAD9783 via the SPI port and access all configuration registers. It supports single-byte and multi-byte data transmission, as well as high-order and low-order order transmission modes. Serial data input and output can be implemented through bidirectional SDIO pins or two single-phase SDIO/SDO pins. The serial port's operating mode is controlled by register bit 0x00[7:6], and the configuration takes effect immediately after writing the last bit of this register.

General Operation of Serial Interface

The DAD9783's SPI communication consists of two phases. The first phase is the instruction cycle (writing the instruction byte to the device), synchronized with the first eight rising edges of SCLK. The instruction byte provides the serial port controller with information about the data transmission cycle (and the second phase of the communication cycle), specifying whether the upcoming data transmission is a read or write operation, and the address of the start register for the first byte in the data transmission. The first eight rising edges of SCLK in each communication cycle are used to write the instruction byte to the device.

When the CSB pin changes from logic high to logic low, the serial port timing is reset to the initial state of the instruction cycle. The first eight rising edges of SCLK from this state represent the instruction bit of the current I/O operation. The remaining SCLK edges are used for the second phase of the communication cycle. The second phase is where the actual data transmission occurs between the device and the system controller. One or more data bytes can be transmitted during the second phase of the communication cycle.

Data Format

The instruction bytes for the SPI port are shown in the table below:

MSB				LSB			
B7	B6	B5	B4	B3	B2	B1	B0
R/W	N1	N0	A4	A3	A2	A1	A0

R/W: Bit 7 of the instruction byte determines whether a read or write operation is performed after the instruction byte write cycle. 1 indicates a read operation, and 0 indicates a write operation.

N[1:0]: Defines the number of bytes transmitted.

00: Transmit one byte

11: Transmit 4 bytes

A4~A0: Bits 4 to 0 of the instruction byte determine the data transmission phase of the communication cycle.

The address of the register to be accessed. For multi-byte transfers, this address is the end address in MSB mode. In LSB mode, this is the start byte address.

Serial Port (SPI) Pin Function Description

SCLK, the serial clock pin, is used to synchronize data input/output devices and run the internal state machine. SCLK supports a frequency of 40MHz. All data input occurs on the rising edge of SCLK, and output occurs on the falling edge of SCLK.

The **CSB** chip select pin is active low and is used to start and select one communication cycle. When the chip select is high, the SDIO pin enters a high-impedance state. The chip select signal should remain low throughout the entire SPI communication.

SDIO is a bidirectional data port; both writing to and reading from device registers must be performed through this pin. Data input is always done through this pin. After power-on reset, this pin defaults to bidirectional operation.

SDO is the data output port for reading data from the device registers. Its enable is controlled by bit 7 of register 0x00. When this bit is set to 0, SDO has no data output and is in a high-impedance state.

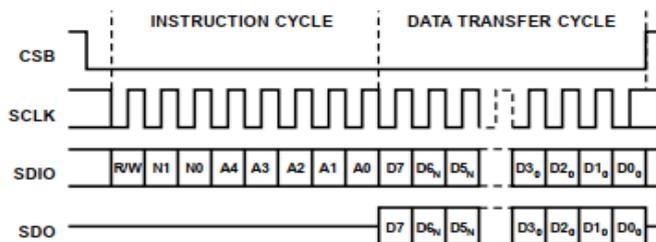
Serial Interface Options

The DAD9783's SPI port supports both MSB (Most Big Byte) and LSB (Least Big Byte) data formats. This function is controlled by **LSB_FIRST** (bit 6 of register 0x00). The default is MSB priority (**LSB_FIRST** = 0).

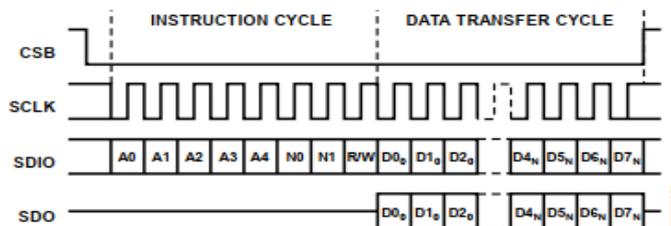
When **LSB_FIRST** = 0 (MSB priority), instruction and data bits must be written in MSB-to-LSB order. Multibyte data transfer in MSB priority format begins with an instruction containing the address of the most significant data byte register. Subsequent data bytes must be transferred in high-address-to-low-address order. In MSB mode, the serial port's internal address generator decrements by 1 for each data byte transferred during a multibyte communication cycle.

When **LSB_FIRST** = 1 (LSB priority), instruction and data bits must be written in LSB to MSB order. LSB priority begins with an instruction that includes the address of the least significant data byte register. Subsequent data bytes must be transmitted in low-address to high-address order. In LSB mode, the serial port's internal address generator increments by 1 for each data byte transmitted in a multi-byte communication cycle.

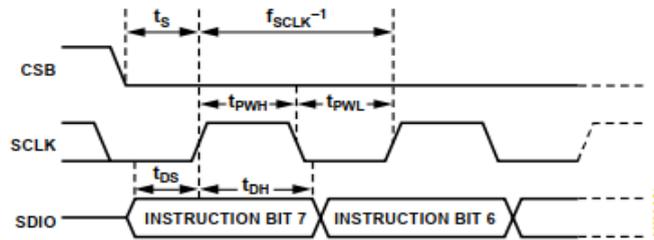
If MSB priority mode is enabled, the serial port controller's data address will decrement starting from the data address where 0x00 is written for multi-byte I/O operations. If LSB priority mode is enabled, the serial port controller's address will increment starting from the data address where 0x7F is written for multi-byte I/O operations.



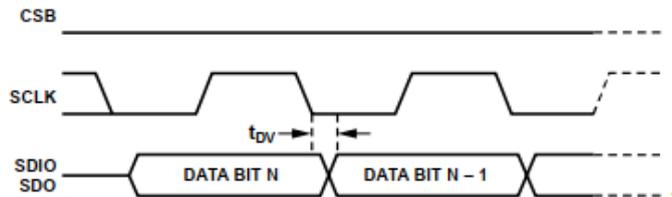
Serial register interface timing (MSB priority)



Serial register interface timing (LSB priority)



Serial register write operation timing diagram



Serial register read operation timing diagram

SPI Register Description

Register Name	Address	Bit	Bit Name	Description
SPI Control Register	0x00	7	SDIODIR	0 = SPI is a four-wire operating mode, SDIO is an input pin. 1 = SPI is a three-wire operating mode, SDIO is a bidirectional input/output pin.
		6	LSBFIRST	0 = LSBFIRST mode is off, SPI serial data format is MSB mode. 1 = LSBFIRST mode enabled, SPI serial data format is LSB mode.
		5	RESET	0 = Normal working mode 1 = Soft reset; restores all registers to their default state (except for register 0x00).
Data Control Register	0x02	7	DATA	0 = Sets the DAC input data to two's complement format. 1 = Sets the DAC input data to unsigned binary format.
		4	INVDCO	1 = DCO output inverted
Power-Down Control Register	0x03	7	PD_DCO	1 = DCO output power failure
		6	PD_INPT	1 = DCO Input power failure
		5	PD_AUX2	1 = AUX2 DAC power failure
		4	PD_AUX1	1 = AUX1 DAC power failure
		3	PD_BIAS	1 = Reference voltage bias power loss
		2	PD_CLK	1 = DAC clock input circuit power failure
		1	PD_DAC2	1 = DAC2 analog output power off
		0	PD_DAC1	1 = DAC1 analog output power off
Establish and Maintain Registers	0x04	7:4	SET[3:0]	Determine the creation time of the input data
		3:0	HLD[3:0]	Determine the retention time of the input data
Clock Adjustment Register	0x05	4:0	SAMP_DLY[4:0]	5-digit positioning for input data and sampling clock position
Seek Control Register	0x06	2	LVDS Low	One LVDS input is higher than the IEEE standard.
		1	LVDS High	One LVDS input is below the IEEE standard.
		0	SEEK	The margin of input data is determined by LVDS_SET and LVDS_HLD.

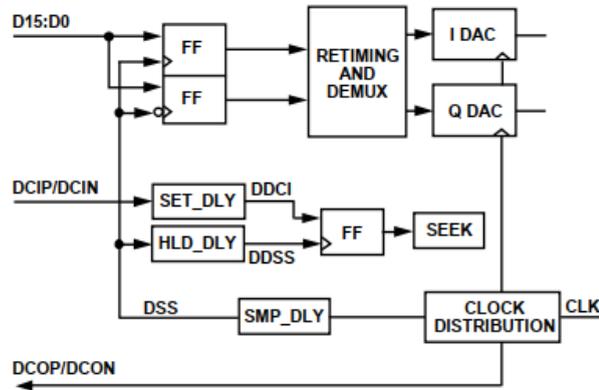
DAD9783 Dual-Channel, 16-Bit, 500 MSPS DAC with LVDS Interface

DAC Mode Control Register	0x0A	3:2	DAC1MODE[1:0]	00 = DAC1 is operating in normal mode.
				01 = DAC1 is operating in zero- return mode .
				10 = DAC1 is operating in zero-return mode.
				1 1 = DAC1 operates in mixer mode
	1:0	DAC2MODE[1:0]	00 = DAC2 is operating in normal mode.	
			01 = DAC2 is operating in zero- return mode .	
			10 = DAC2 is operating in zero-return mode.	
			1 1 = DAC1 operates in mixer mode	
DAC1 Gain Control Register	0x0B	7:0	DAC1FSC[9:0]	The full-scale output current adjustment word of DAC1, totaling 10 bits.
	0x0C	1:0	DAC1FSC[9:8]	0x03FF = Sets the maximum full-scale current to 31.66mA .
				0x0200 = Sets the full-amplitude current to the normal value of 20mA.
0x0000 = Sets the full-scale current to the minimum value of 8.66mA.				
Auxiliary DAC1 Control Register	0x0D	7 :0	AUXDAC1[9:0]	The output current adjustment word of auxiliary DAC1 is 10 bits.
	0x0E	1:0	AUXDAC1[9:8]	0x03FF = Sets the current output to 2mA
				0x0200 = Sets the current output to 1mA
				0x0000 = Sets the current output to 0mA
0x0E	7	AUX1PIN	1 = AUX1P output pin is active 0 = AUX1N output pin is active	
		6	AUX 1DIR	0 = AUX1DAC output is in current-pull mode.
				1 = AUX1DAC output is in current sinking mode
Bit control register	0x1A	7	BISTEN	
		6	BISTRD	
		5	BISTCLR	
BIST Results Register 1	0x1B	7:0	BISTRES1[15:0]	
	0x1C	7:0		
BIST Results Register 2	0x1 D	7:0	BISTRES1[15:0]	
	0x1 E	7:0		
Hardware Version	0x1F	7:4	VERSION[3:0]	
			DEVICE[3:0]	

Parallel Data Interface

The parallel data interface of the DAD9783 consists of 18 pairs of differential signal lines, including DCO, DCI, and 16 pairs of data lines D[15:0]. DCO is the clock signal provided by the DAD9783 to the digital signal processing unit, and the two DACs share one data input port. DCI provides timing information for the parallel input port data.

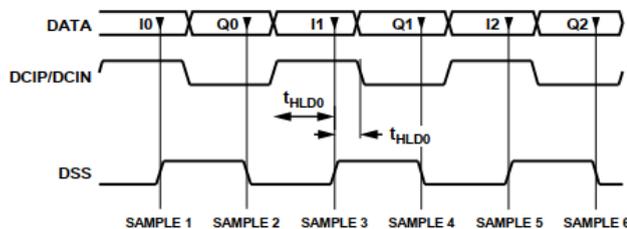
The diagram below shows the functional block diagram of the data interface. The internal clock distribution circuit receives the differential clock signal from the external input and generates the DSS signal. The DSS signal latches the LVDS input data into an internal register. The rising/ falling edges of the DSS signal can be adjusted using a point delay circuit to ensure correct sampling of the LVDS input signal.



Block diagram of digital data interface

Input Data Port Timing

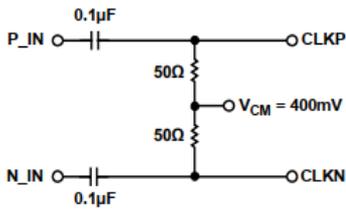
To ensure the DAC can correctly receive data input, a specific timing relationship must be maintained between the DAC's clock signal (CLKP/N), the DCO, and the input ports. The following diagram shows the interface timing sequence for the DAD9783.



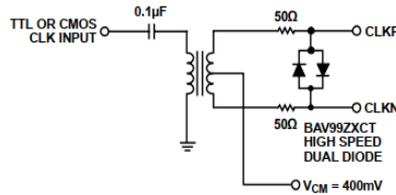
Block diagram of parallel interface clock

DAC Clock Input

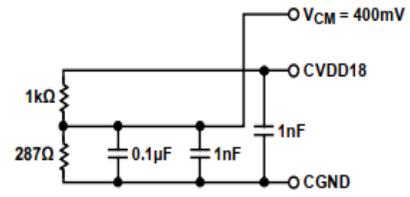
To achieve analog output performance, a low-jitter clock signal is required for the DAC. The common-mode voltage of the clock is 400mV. The figures below show typical clock drive circuits for LVDS, CMOS/TTL, and sinusoidal signals, respectively. Reference circuits for generating the clock common-mode voltage are also provided.



DAC CLK drive circuit



TTL/CMOS DAC CLK drive circuit



DAC CLK VCM GENERATOR circuit

Analog Interface

Full-scale current generation: The full-scale current of DAC1 and DAC2 is a function of the current flowing through pin FSADJ. During use, FSADJ needs to be connected to ground through a 10kΩ resistor. Meanwhile, REFIO needs to be connected to ground through a 0.1µF capacitor. The magnitude of the DAC output full-scale current can be adjusted using DAC1FSC[9:0] and DAC2FSC[9:0]. The following formula shows the relationship between the DAC full-scale output current and DACFSC:

$$IFS = (86.6 + (0.22 \times \text{DAC gain})) \times 1000/R$$

The DAC's transfer function: Each channel of the DAD9783 provides complementary differential currents IOUTP and IOUTN. When all input digital signals are 1, IOUTP outputs the maximum current (full-scale current), while IOUTN outputs zero current. IOUTP and IOUTN are functions of the input digital signals:

$$IOUTP = (\text{DAC DATA}/2^N) \times IFS$$

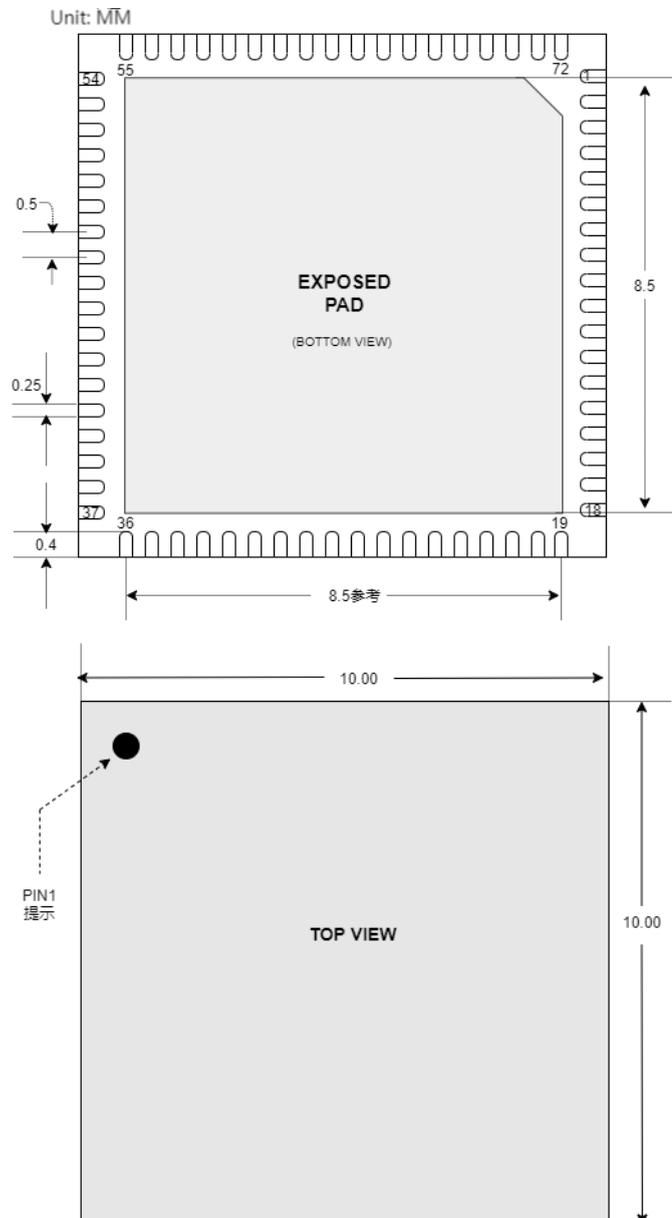
$$IOUTN = ((2^N - 1) - \text{DAC DATA})/2^N \times IFS$$

Wherein, DAC DATA is 0 to $2^N - 1$ (which is a base number). Thus, under the condition of load R, the values of VOUTP and VOUTN are IOUTP x R and IOUTN x R, respectively.

The output voltage is: $VOUT = (IOUTP - IOUTN) \times R$

Operating Modes Overview: The DAD9783 can operate in three modes: Normal Mode, Mixer Mode, and Zero-Return Mode.

Auxiliary DACs: The DAD9783 integrates four 10-bit low-speed DACs. Two are used internally to directly adjust the gain of the output signals of DAC1 and DAC2, while the other two output directly to an external chip for adjusting the DAC output bias. This provides flexible RF output port local oscillator leakage adjustment and image rejection adjustment functions for transmit systems that directly sample quadrature modulators.

Encapsulation Information


Note: If there are vias on the PCB under the device, they must be covered or filled with solder mask to avoid short circuits.

Device Ordering Information List

Product Model	Temperature Range	Packaging	Package	RoHS
DAD9783	-40 ° C to +85 ° C	72-QFN	168/tray	Y