1. Characteristic

- Low power consumption (under full operating conditions): 1.0W@1GSPS , 600mW@500MSPS
- ACLR for single-carrier WCDMA: 80dBc@80MHz intermediate frequency
- Adjustable analog output: 8.7mA-31.7mA (R_L = 25Ω-50Ω)
- Novel 2×, 4×, 8× interpolators/coarse-tuning, complex modulators can place the carrier anywhere within the DAC bandwidth
- The auxiliary DAC can control the external VGA and offset
- Multi-chip synchronous interface
- High-performance, low-noise phase-locked loop clock multiplier
- Digital inverse sinc filter
- Circuit interfaces: CMOS interface, SPI interface
- TQFP100 package

2. Applications

- Wireless infrastructure: W-CDMA, GSM, CDMA2000 TD-SCDMA, WiMax, LTE
- Digital high/low intermediate frequency synthesis
- Internal digital upconversion function
- Launch diversity
- Broadband communication: LMDS, MMDS, point-to-point communication

3. Overview

The DAD9779 is a dual-channel, 16-bit, high dynamic range digital-to-analog converter (DAC). This converter offers sampling rates up to 1 GSPS and can generate multi-carrier signals up to the Nyquist frequency. It features optimized for direct-conversion transmission applications, including digital real/complex modulation and gain and offset compensation. The DAC core output stage is optimized for seamless interface with mainstream analog quadrature modulators, such as Analog Devices' ADL537X FMOD series modulators. A three-wire interface allows for programming and readback of many internal parameters. The DAC core's full-scale output current is programmable from 10mA to 30mA. Manufactured using advanced 0.18μm CMOS technology, it operates from a 1.8V/3.3V supply with a total power consumption of 1.0W. It is packaged in a 100-pin T QFP100 package.

The DAD9779 can be functionally divided into a digital filter unit, a DAC core unit, a clock unit (including an internal phase-locked loop), auxiliary DACs, and a multi-chip synchronization unit. The digital section performs digital interpolation and digital-domain real-domain modulation and complex modulation on the input signal; the DAC core performs digital-to-analog conversion on the digital signal; SPI configures the entire chip; the clock unit provides a high-quality clock for the entire circuit; and four auxiliary DACs are used for channel amplification.

4. Device packaging information

Product Model	Packaging	Package size
DAD9779	TQFP100	14mm×14mm

5. Functional Block Diagram

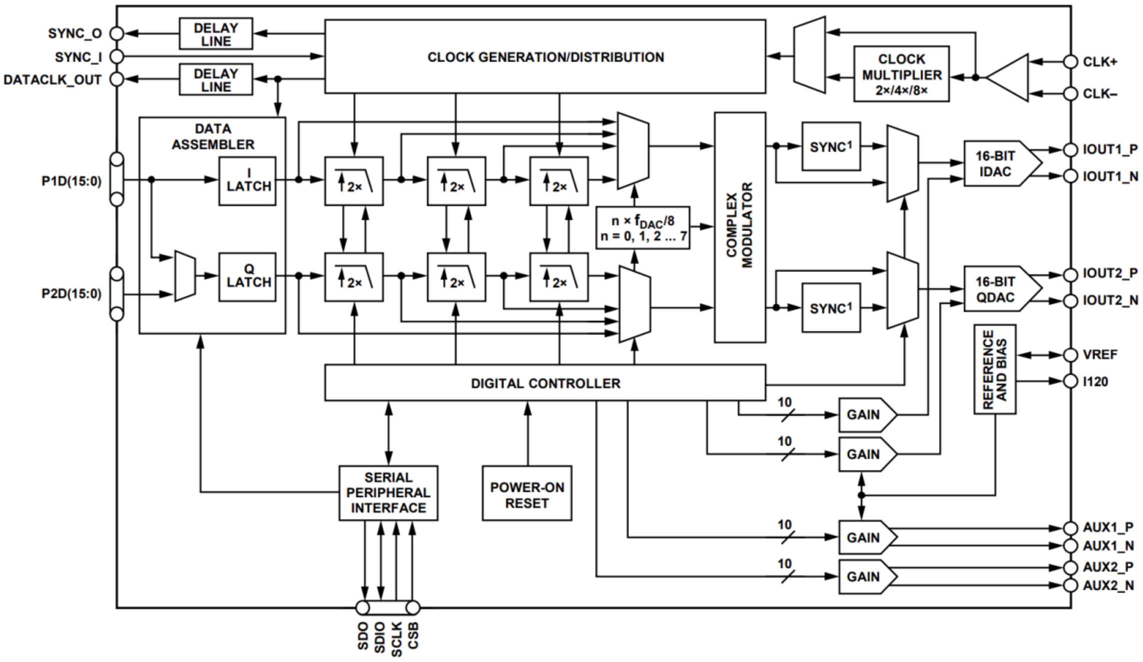


Figure 1. Functional Block Diagram

6. Pin Configuration and Functions

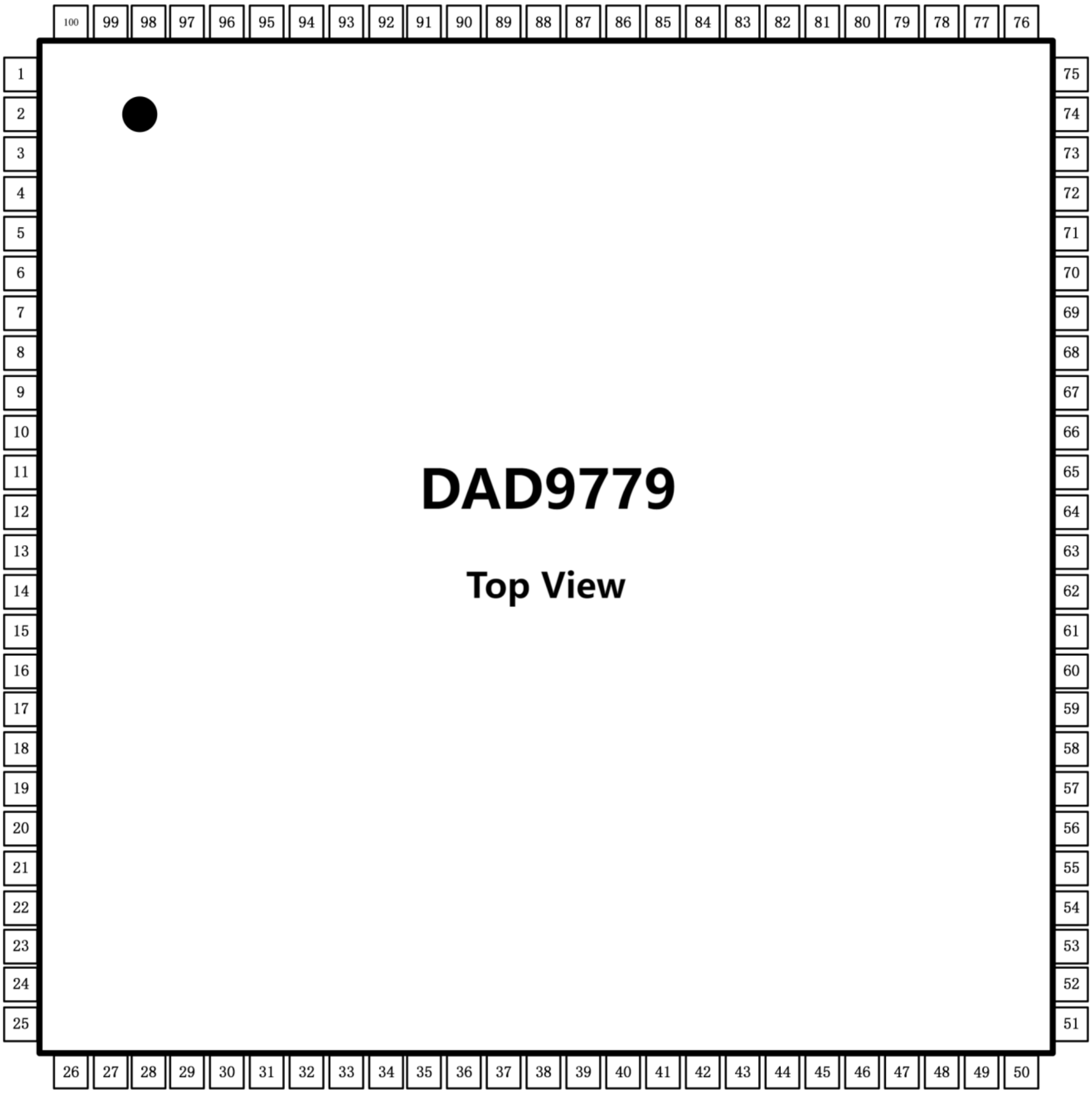


Figure 2. Pin configuration

Pin Description

PIN No.	Mnemonic	Function	PIN No.	Mnemonic	Function
1	V_{DDC}	1.8V clock power supply	51	P2B6	Port 2 data input bits 6
2	V_{DDC}	1.8V clock power supply	52	P2B5	Port 2 data input bit 5
3	GND_C	Clock common	53	V_{DDD}	1.8V digital power supply
4	GND_C	Clock common	54	GND_D	Digital common
5	CLK+	Differential clock input positive terminal	55	P2B4	Port 2 data input bit 4
6	CLK-	Differential clock input negative terminal	56	P2B3	Port 2 data input bit 3
7	GND_C	Clock common	57	P2B2	Port 2 data input bit 2
8	GND_C	Clock common	58	P2B1	Port 2 data input bit 1
9	V_{DDD}	1.8V digital power supply	59	P2B0	Port 2 data input bit 0
10	V_{DDD}	1.8V digital power supply	60	V_{DDD}	1.8V digital power supply
11	GND_C	Clock common	61	V_{DDIO}	3.3V digital power supply
12	GND_A	Analog common	62	SYNC_O-	LVDS Differential Synchronous Output Negative Terminal
13	SYNC_I+	LVDS Differential Synchronous Input Positive Terminal	63	SYNC_O+	LVDS Differential Synchronous Output Positive Terminal
14	SYNC_I-	LVDS Differential Synchronous Input Negative Terminal	64	GND_D	Digital common
15	GND_D	Digital common	65	PLL_LOCK	PLL Lock Indicator
16	V_{DDD}	1.8V digital power supply	66	SPI_SDO	Serial interface data output
17	P1B15	Port 1 data input bit 15	67	SPI_SDIO	Serial interface data input/output
18	P1B14	Port 1 data input bit 14	68	SPI_CLK	Serial interface clock
19	P1B13	Port 1 data input bit 13	69	SPI_CSB	Serial interface chip select signal
20	P1B12	Port 1 data input bit 12	70	RESET	Reset, active high
21	P1B11	Port 1 data input bit 11	71	IRQ	Interruption Request
22	GND_D	Digital common	72	GND_A	Analog common
23	V_{DDD}	1.8V digital power supply	73	IPTAT	Factory test pin
24	P1B10	Port 1 data input bit 10	74	VREFF	Reference voltage output
25	P1B9	Port 1 data input bit 9	75	I120	120μA reference current
26	P1B8	Port 1 data input bits 8	76	V_{DDA}	3.3V analog power supply
27	P1B7	Port 1 data input bit 7	77	GND_A	Analog common
28	P1B6	Port 1 data input bits 6	78	V_{DDA}	3.3V analog power supply
29	P1B5	Port 1 data input bit 5	79	GND_A	Analog common
30	P1B4	Port 1 data input bits 4	80	V_{DDA}	3.3V analog power supply
31	P1B3	Port 1 data input bit 3	81	GND_A	Analog common
32	GND_D	Digital common	82	GND_A	Analog common
33	V_{DDD}	1.8V digital power supply	83	I_{OUTA2}	Channel 2 Differential DAC Current Output Positive Terminal
34	P1B2	Port 1 data input bit 2	84	I_{OUTB2}	Channel 2 Differential DAC Current Output Negative Terminal
35	P1B1	Port 1 data input bit 1	85	GND_A	Analog common
36	P1B0	Port 1 data input bit 0	86	AUX2_P	Channel 2 Auxiliary DAC Current Output Positive Terminal
37	DATACLK	Data clock output	87	AUX2_N	Channel 2 Auxiliary DAC Current Output Negative Terminal
38	V_{DDIO}	3.3V digital power supply	88	GND_A	Analog common
39	TXENABLE	Enable occurs. In single-port mode, this pin is also used as an IQ select.	89	AUX1_N	Channel 1 Auxiliary DAC Current Output Negative Terminal
40	P2B15	Port 2 data input bit 15	90	AUX1_P	Channel 1 Auxiliary DAC Current Output Positive Terminal
41	P2B14	Port 2 data input bit 14	91	GND_A	Analog common
42	P2B13	Port 2 data input bit 13	92	I_{OUTB1}	Channel 1 Differential DAC Current Output Negative Terminal
43	V_{DDD}	1.8V digital power supply	93	I_{OUTA1}	Channel 1 Differential DAC Current Output Positive Terminal
44	GND_D	Digital common	94	GND_A	Analog common
45	P2B12	Port 2 data input bit 12	95	GND_A	Analog common
46	P2B11	Port 2 data input bit 11	96	V_{DDA}	3.3V analog power supply
47	P2B10	Port 2 data input bit 10	97	GND_A	Analog common
48	P2B9	Port 2 data input bit 9	98	V_{DDA}	3.3V analog power supply
49	P2B8	Port 2 data input bits 8	99	GND_A	Analog common
50	P2B7	Port 2 data input bit 7	100	V_{DDA}	3.3V analog power supply

8. Electrical characteristics

(Unless otherwise specified, V_{CC}=3.3V, V_{DD}=1.8V, GND_A = GND_D = 0V, -40℃≤TA≤85℃)

Parameter	Condition	Min	Typ	Max	Unit
Resolution			16		Bits
Logic input high level voltage	SCLK, CSB, SDI pins	2.0			V
Logic input low level voltage				0.8	V
Logic input high-level current	VIH = VCC, CSB pin			28	μA
	VIH=VCC, pinout			44	μA
	VIH=VCC, SCLK pin			300	nA
	VIH = VCC, SDI pin			300	nA
Logic input low-level current	VIL=GNDA, CSB pin	- 70			μA
	VIL=GNDA, pinout	- 300			nA
	VIL=GNDA, SCLK pin	- 300			nA
	VIL=GNDA, SDI pin	- 300			nA
Logic output high level voltage	IOUT = -0.5mA, SDO pin	1.8			V

9. Recommended working conditions

- Input data rate: ≤300MSPS
- Operating frequency: ≤1000MHz
- 3.3V Analog Supply Voltage: 3.1V~3.5V
- 3.3V Digital Supply Voltage: 3.1V~3.5V
- 1.8V Clock and Analog Supply Voltage: 1.7V~1.9V
- 1.8V Digital Supply Voltage: 1.7V~1.9V
- Operating ambient temperature: -55℃~125℃
- Operating temperature range (T_C): -40℃~85℃

10. Absolute maximum ratings

- 3.3V Analog Supply Voltage: -0.3V-3.6V
- 3.3V Digital Supply Voltage: -0.3V-3.6V
- 1.8V Clock Supply Voltage: -0.3V-1.98V
- 1.8V Digital Supply Voltage: -0.3V-1.98V
- Storage temperature: -65℃~150℃
- Junction temperature: 125℃
- Lead soldering temperature resistance: 300℃

11. Performance Indicators

Unless otherwise specified, V_{DDC} = V_{DD} = 1.8V, V_{DDIO} = V_{DDA}= 3.3V, GND_C = GND_D = GND_A = 0V.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resolution	RES			16		bit
Differential nonlinearity	E_{DL}		- 6	±2.5	+6	LSB
Integral nonlinearity	E_L		-12	±3.5	+12	LSB
Offset error	E_O		-1%	±0.005%	+1%	FSR
Gain error	E_G		-8%	±2%	+8%	FSR
Power consumption	P_W	2x mode, PLL off, f_{DAC} = 320MSPS, IF = 16MHz		550	650	mW
Operating frequency	f_{CLK}		1,000	1,000		MHz
Stray dynamic range	SFDR	f_{DATA} =100MSPS, f_{OUT} =20MHz	65	80		dBFS
Dual-tone intermodulation distortion	IMD	f_{DATA} =200MSPS, f_{OUT} =50MHz	65	81		dBFS
Functional testing		By modifying the SPI registers 0X0C[1:0] and 0X0B[7:0] respectively Configured to 1023 and 0, adjusting the full-scale output current of channel I.	When the configuration value is 1023, the full-scale output current of channel I should be between 30.5mA and 32.5mA; when the configuration value is 0, the full-scale output current of channel I should be between 7.5mA and 9.5mA.			
		By modifying the SPI registers 0X10[1:0] and 0X0F[7:0] respectively Configured to 1023 and 0, the full-scale output current of the Q channel is adjusted.	When the configuration value is 1023, the full-scale output current of the Q channel should be between 30.5mA and 32.5mA; when the configuration value is 0, the full-scale output current of the Q channel should be between 7.5mA and 9.5mA.			

12. Timing Diagram

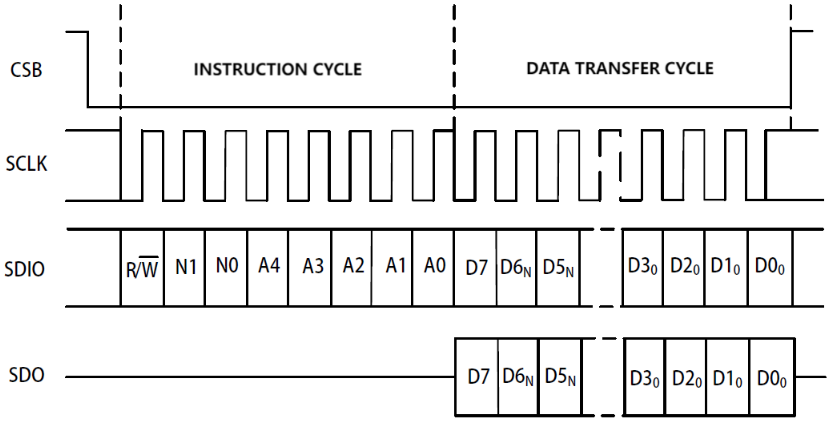


Figure 3. Serial register interface timing, MSB first

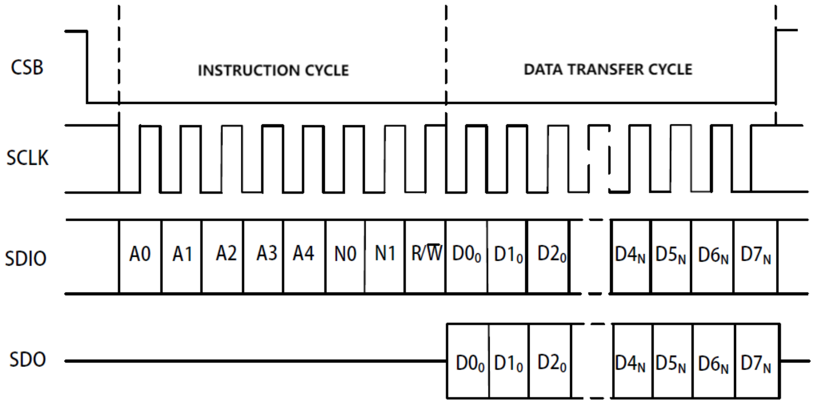


Figure 4. Serial register interface timing, LSB first

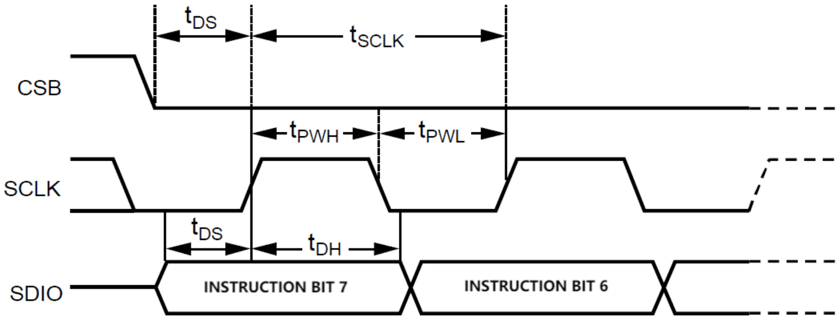


Figure 5. Timing diagram for SPI register write

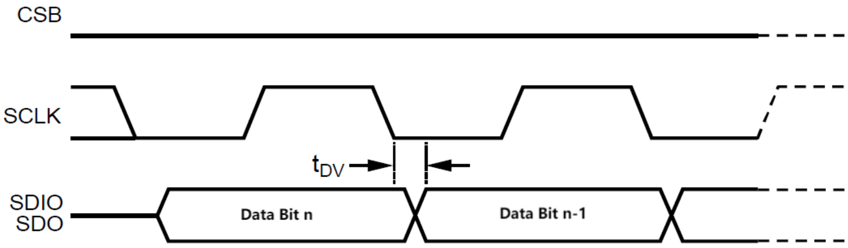


Figure 6. Timing diagram for SPI register read

13. Application Instructions

- **Three-wire interface**

The DAD9779 employs a three-wire interface, a flexible synchronous serial communication port that easily interfaces with various industry-standard microcontrollers and microprocessors. This port is compatible with most synchronous transmission formats, including Motorola SPI and Intel*SSR protocols. This interface allows read and write operations to access all registers used to configure the DAD9779. It supports single-byte and multi-byte transfers, as well as MSB-first and LSB-first transfer formats. Serial data input/output can be achieved via a single bidirectional pin (SDIO) or two unidirectional pins (SDIO/SDO). Serial port configuration is controlled by bits 7:6 of register 0x00. It is important to note that any changes made to the serial port configuration take effect immediately upon writing the last bit of this byte. Therefore, multi-byte transfers can be written to this register, and the configuration can be changed during a communication cycle. It is crucial to ensure that the new configuration is used for the remaining bytes of the current communication cycle. When changing the serial port configuration, it is recommended to use single-byte transfers to avoid unpredictable device behavior. As described in this section, all serial port data transfers written to or read from the device are synchronized with the SCLK pin. If synchronization is lost, the device has the capability to asynchronously terminate the I/O operation, placing the serial port controller in a known state to regain synchronization.

- **General operation of serial interface**

A communication cycle of the DAD9779 has two phases. Phase 1 is the instruction cycle, used to write an instruction byte to the DAD9779, corresponding to the first group of eight rising edges of SCLK. The instruction byte in Phase 1 defines whether the upcoming data transfer is a read or a write, and the register address corresponding to the first byte of data transfer. The first group of eight rising edges of SCLK in each communication cycle is typically used to write the instruction byte to the DAD9779. The logic level of the CSB pin goes high followed by low, resetting the timing of the three-wire interface port to the initial state of the instruction cycle. From this state, the subsequent eight rising edges of SCLK represent the instruction bit of the current I/O operation, regardless of the state of the internal registers or other signal levels input to the three-wire interface port. If the three-wire interface port is in an instruction cycle or a data transfer cycle at this time, no existing data will be written. The remaining SCLK edges are used for the second phase of the communication cycle. The second phase is the phase where data transfer actually occurs between the device and the system controller. Based on the information provided by the instruction byte, the second stage transfers one, two, three, or four data bytes. It is best to use a multi-byte transfer. Single-byte data transfers can be used to reduce CPU overhead when register access requires only one byte. The register is changed immediately after the last bit of each transferred byte is written.

- **Instruction byte**

The information contained in the instruction byte is shown in Table 1.

MSB LSB

17	16	15	14	13	12	11	10
R/W	N1	N0	A4	A3	A2	A1	A0

Table 1. Three-wire interface instruction bytes

Bit 7 (R / W) of the instruction byte determines whether a read or write operation occurs after the instruction byte write cycle. Logic 1 indicates a read operation, and logic 0 indicates a write operation. Bits 6 (N1) and 5 (NO) of the instruction byte determine the number of bytes to be transferred during the data transfer cycle. Table 2 lists the corresponding number of bytes to be transferred. Bits 4, 3, 2, 1, and 0 of the A4, A3, A2, A1, and A0 instruction bytes determine which register is accessed during the data transfer phase of the communication cycle. For multi-byte transfers, this address is the starting byte address. The remaining register addresses are generated by the device based on the LSB priority bit (bit 6 of register 0x00).

N1	N0	Description
0	0	Transmit one byte
0	1	Transmit two bytes
1	0	Transmit three bytes
1	1	Transmit four bytes

Table 2. Byte Transfer Count

- **Serial interface port pin function description**

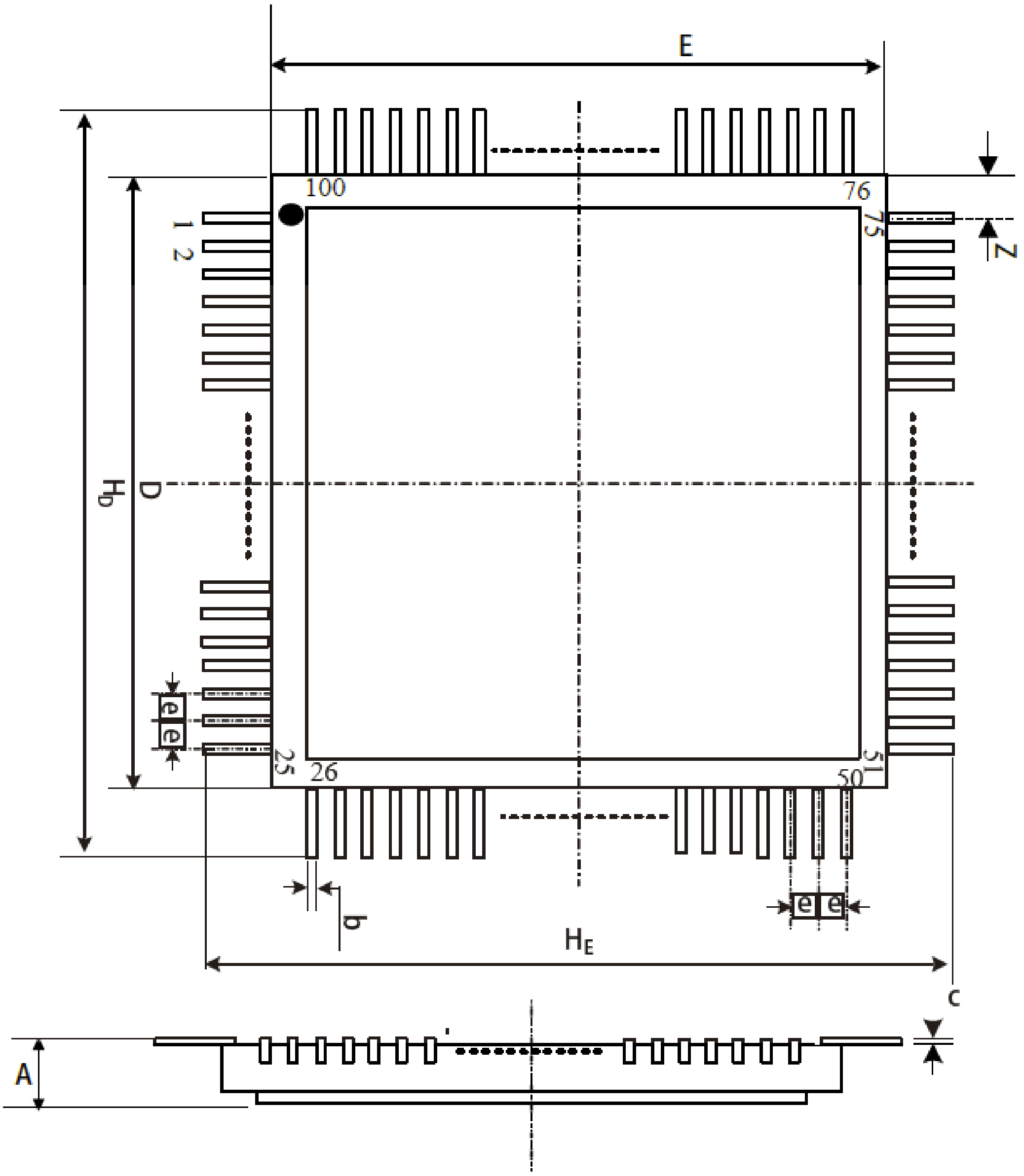
1. Serial Clock (SCLK) : The serial clock pin is used to synchronize data input/output devices and control the internal state machine. The maximum frequency of SCLK is 40 MHz. All data inputs are valid on the rising edge of SCLK. All data is output on the falling edge of SCLK.
2. Chip Select (CSB) : Active low input initiates and strobes one communication cycle. It allows multiple devices to be connected on the same serial communication line. When this input is high, the SDO and SDIO pins enter a high-impedance state. The chip select should remain low throughout the communication cycle.
3. Serial Data Input/Output (SDIO) : Data must be written to the device through this pin. However, this pin can also be used as a bidirectional data line. Bit 7 of register 0x00 controls the configuration of this pin. The default value is logic 0, which configures the SDIO pin as a unidirectional data line.
4. Serial Data Output (SDO) : If the protocol selects to use different communication lines to send and receive data, then the data is read from this pin. When the device is operating in a separate bidirectional I/O mode, this pin does not output data and is set to a high impedance state.
5. MSB/LSB Transmission: The serial port supports both MSB-first and LSB-first data formats. This function is controlled by the LSB/MSB-first register bit (bit 6 of register 0x00). The default is MSB-first format (LSB/MSB-first = 0). When MSB-first format is selected (LSB/MSB-first = 0), instruction and data bits must be written in order from MSB to LSB. Multibyte data transmission in MSB-first format begins with an instruction byte, which includes the register address of the most significant data byte. Subsequent data bytes should be transmitted in order from high address to low address. In MSB-first mode, the serial port's internal byte address generator decrements by 1 for each data byte transmitted in a multibyte communication cycle. When LSB/MSB-first = 1 (LSB-first), instruction and data bits must be written in order from LSB to MSB. Multibyte data transmission in LSB-first format begins with an instruction byte, which includes the register address of the least significant data byte, followed by multiple data bytes. In multi-byte communication cycles, the internal byte address generator of the serial port increments by 1 for each byte transmitted. If MSB priority format is enabled, for multi-byte I/O operations, the serial port controller data address will decrement starting from the data address written to 0x00. If LSB priority format is enabled, for multi-byte I/O operations, the serial port controller address will increment starting from the data address written to 0x1F.

14. Three - wire interface register mapping table

Register Name	Address		Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default value
	Hexadecimal	Decimal									
Communication	0x00	00	SDIO bidirectional	LSB/MSB priority	Software reset	Power-off mode	Automatic power-down enable		PLL locking refers to Show (read-only)		0x00
Digital control	0x01	01	Interpolation coefficients [1:0]		Filter modulation mode [3:0]				DATACLK Delay [4]	zero value Fill Enable	0x00
	0x02	02	Data format	single port	Real number mode	DATACLK Delayed enable	Inverse sinc enable	DATACLK Inverted	TxEnable Inverted	Q Priority	0x00
Synchronous control	0x03	03	DATACLK Delay mode	Reserve (set to 1)	DATACLK frequency division [1:0]		Data timing margin [3:0]				0x00
	0x04	04	DATACLK delay [3:0]				SYNC_O frequency division [2:0]			SYNC_O Delay [4]	0x00
	0x05	05	SYNC_O delay [3:0]				SYNC_I ratio [2:0]			SYNC_I Delay [4]	0x00
	0x06	06	SYNC_I delay [3:0]				SYNC_I Timing Margin [3:0]				0x00
	0x07	07	SYNC_I Enable	SYNC_O Enable	SYNC_O Trigger edge	Clock status [4:0]					0x00
PLL control	0x08	08	PLL band selection [5:0]						PLL VCO drive [1:0]		0xE7
	0x09	09	PLL Enable	PLL VCO division ratio [1:0]		PLL loop division ratio [1:0]		PLL bias [2:0]			0 x52
Other control	0x0A	10	VCO control voltage [2:0] (read-only)			PLL loop bandwidth [4:0]					0 x1F
IDAC control	0x0B	11	I DAC gain adjustment [7:0]								0 xF9
	0x0C	12	IDAC hibernation	IDAC power failure					IDAC Gain Adjustment [9:8]		0 x01
DAC1 Auxiliary Control	0x0D	13	Support DAC1 data [7:0]								0x00
	0x0E	14	Auxiliary DAC1 symbol	Auxiliary DAC1 current direction	Auxiliary DAC1 power off				Auxiliary DAC1 data [9:8		0x00
QDAC control	0x0F	15	Q DAC gain adjustment [7:0]								0 xF9
	0x10	16	Q DAC sleep	Q DAC Power outage					Q DAC Gain adjustment [9:8]		0 x01
Control Auxiliary DAC2	0x11	17	Support DAC2 data [7:0]								0x00
	0x12	18	Auxiliary DAC2 symbol	Auxiliary DAC2 Current Direction	Auxiliary DAC2 power off				Auxiliary DAC2 data [9:8		0x00
	0x13 ~ 0x18	19~24	Reserved								
Interruption	0 x19	25	Data timing error IRQ	Synchronization timing error IRQ		Data timing error types	Data timing error IRQ enable	Error IRQ Synchronization Timing Enable		Internal synchronization feedback	0x00
Version	0 x1F	31	Version [7:0]								0x07

15 . Package Dimensions and Structure

TQFP100 package



Unit: mm

Dimension symbol	Values			Dimension symbol	Values		
	Min	Typ	Max		Min	Typ	Max
A	2.15	2.65	2.75	b	0.15	0.2	0.25
D		14.6	14.78	e		0.5	
E		14.6	14.78	H_D	19.00		23.00
c	0.05	0.15	0.25	H_E	19.00		23.00
Z			1.62				

16. Package Information

Model	Temperature range	Packaging	Package
DAD9779	-40 ℃ ~85 ℃	TQFP100	90/tray