DAD9747 Dual-channel, 16bit, 250MSPS DAC with COMS Interface

Characteristics

- High dynamic range, dual DAC
- Low noise and intermodulation distortion
- Single-carrier W-CDMA ACLR = 80dBc (61.55MHz)
- The innovative switching output stage allows for output frequencies exceeding the Nyquist frequency
- Includes dual-port LVCMOS input or select interleaved access single-port operation
- The differential analog current output can be programmed from 8.6mA to 31.7mA
- The auxiliary 10-bit current DAC has current sinking/current sourcing capabilities and can be used in external zero-bias compensation circuits
- Built-in 1.2V precision reference voltage source
- Operating power supply: 1.8V ~ 3.3V
- Power consumption: 320mW
- Small size, lead-free, 72-pin QFN package

Applications

- Wireless infrastructure:
  WCDMA, CDMA2000, TD-SCDMA, WiMAX
- Broadband communication: LMDS/MMDS, point-to-point
- Instrumentation: Radio frequency (RF) signal generators, arbitrary waveform generators

Overview

The DAD9747 is a high dynamic range DAC, a dual-channel digital-to-analog converter with 16-bit resolution and a sampling rate up to 250 MSPS. It can output multi-carrier wideband signals within the Nyquist band. Internally, it is specifically designed for direct-conversion transmit applications, including gain and bias compensation. The output can be seamlessly connected to an analog quadrature modulator. A 4-wire SPI interface allows for DAC configuration, readout, and other operations. The DAC output current is configurable from 8.6mA to 31.7mA.

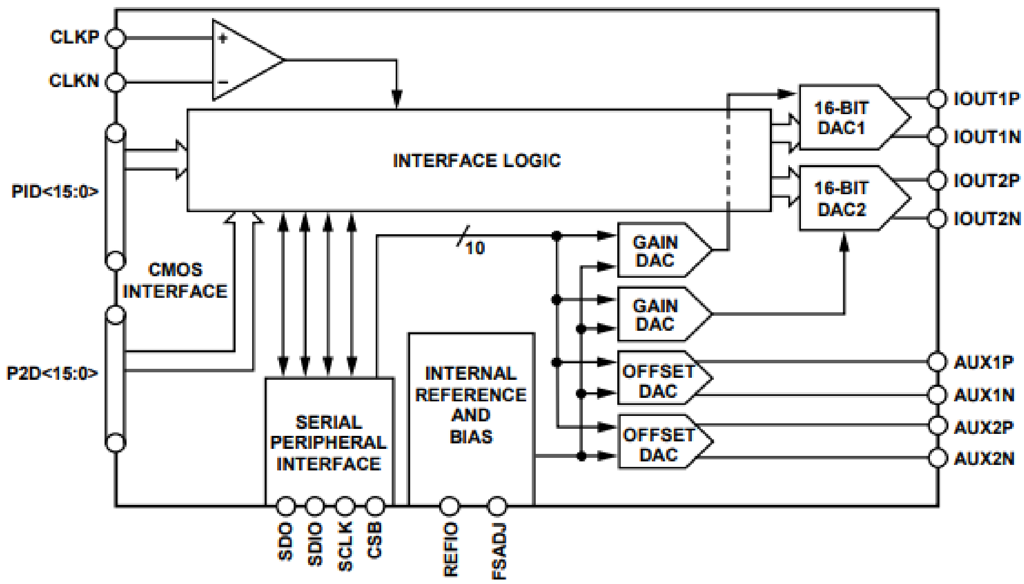
Product Features

1. Utilizing low noise and intermodulation distortion (IMD) characteristics enable high-quality synthesis of broadband signals.

2. Proprietary switch outputs enhance dynamic performance.

3. Programmable current output and dual auxiliary DACs provide both flexibility and enhanced system functionality.

Functional Block Diagram



DC Characteristics

Unless otherwise specified, T_{min} to T_{max}, AVDD33=3.3V, DVDD33=3.3V, AVDD18=1.8V, DVDD18=1.8V, Ioutfs =20mA, full power digital input, maximum sampling rate

Table 1.

Parameter	Min	Typ	Max	Unit
Resolution		16		Bits
Accuracy				
Differential nonlinearity (DNL)		±2		LSB
Integral nonlinearity (INL)		±4		LSB
Main DAC output				
Offset error		±0.001		% FSR
Offset error temperature coefficient		0.1		ppm/℃
Gain error		±2.0		% FSR
Gain error temperature coefficient		100		ppm/℃
Gain matching (DAC 1 - DAC 2)		±1.0		% FSR
Full-scale output current	8.6		31.7	mA
Constant current source output	-1.0		+1.0	V
voltage		10		MΩ
Output impedance				
Auxiliary DAC output				
Resolution		10		Bits
Full-scale output current	-2		+2	mA
Output compliance range (Sink)	0.8		1.6	V
Output compliance range (Source)	0		1.6	V
Output impedance		1		MΩ
Monotonicity	10			Bits
Reference input/output				
Output voltage		1.2		V
Output voltage temperature		10		ppm /℃
coefficient	1.15		1.3	V
External input voltage range		5		kΩ
Output or output impedance				
Power input voltage				
AVDD 33 , DVDD 33	3.13		3.47	V
CVDD 18 , DVDD 18	1.70		1.90	V
Digital power supply				
IAVDD33		56	60	mA
IDVDD 33		12	16	mA
ICVDD18		18	22	mA
IDVDD18		32	36	mA
Power consumption				
fDAC = 250 MSPS, fout = 20 MHz		310	355	mW
Disabling DAC output		125		mW
Power-off mode		3		mW
Operating temperature	-40		+85	℃

AC Characteristics

Unless otherwise specified, T_{min} to T_{max}, AVDD33=3.3V, DVDD33=3.3V, AVDD18=1.8V, DVDD18=1.8V, Ioutfs =20mA, full power digital input, fDAC = 250Msps

Table 2.

Parameter	Min	Typ	Max	Unit
Spurious-free dynamic range (SFDR)				
fDAC = 250 MSPS , fOUT = 20 MHz		83		dBC
fDAC = 250MSPS , fOUT = 70MHz		70.5		dBC
fDAC = 250MSPS , fOUT = 180MHz (Note 1)		66		dBC
Intermodulation distortion (IMD)				
fDAC = 250 MSPS , fOUT = 20 MHz		87		dBC
fDAC = 250MSPS , fOUT = 70MHz		81		dBC
fDAC = 250MSPS , fOUT = 180MHz (Note 1)		73		dBC
Crosstalk				
fDAC = 250MSPS , fOUT = 20MHz		80		dBC
fDAC = 250MSPS , fOUT = 70MHz		80		dBC
fDAC = 250MSPS , fOUT = 180MHz (Note 1)		80		dBC
Adjacent channel leakage ratio				
fDAC =245 .7 6MSPS , fOUT =15.36MHZ		82		dBC
fDAC =245.76MSPS , fOUT =61.44MHZ		80		dBC
fDAC =245.76MSPS , fOUT =184.32MHZ (Note 1)		74		dBC
Noise spectral density				
fDAC =245.76MSPS , fOUT =15.36MHZ		-164		dBC /HZ
fDAC =245.76MSPS , fOUT =61.44MHZ		-161		dBC /HZ
fDAC =245.76MSPS , fOUT =184.32MHZ (Note 1)		-159		dBC /HZ

Note 1: Operating in mixing mode

Digital and Clock Characteristics

Unless otherwise specified , T_{min} to T_{max} , AVDD33=3.3V, DVDD33=3.3V, AVDD18=1.8V, DVDD18=1.8V, Ioutfs =20mA, full power digital input, maximum sampling rate

Table 2.

Parameter	Min	Typ	Max	Unit
DAC Clock Inputs (CLKP, CLKN)				
Differential voltage	400	800	1600	mV
Single-ended peak-to-peak voltage			800	mV
Common mode voltage	300	400	500	mV
Input current			1	uA
Input frequency			250	MHZ
DAC Clock Output (DCO)				
Output high voltage	24			V
Output low voltage			0.4	V
Output current	2.0		10	mA
DAC clock to DCO delay (tDCO)		22	2.8	ns
Data Port Input				
Output high voltage	2.0			V
Output low voltage			0.8	V
Input current			1	uA
CSB to SCLK setup time (tDBS dual - port mode)	400			ps
CSB to SCLK hold time (tDBH dual- port mode)	1200			ps
DAC clock to analog output data delay			7	Cycles
Input for DAC clock hold time (tDBS single-mode port	400			ps
mode)	1200			ps
Input for DAC clock hold time (tDBH single-mode port			8	Cycles
mode)				
DAC clock to analog output data delay (single-port				
mode)				
Serial Port				
SCLK frequency (fSCLK)			40	MHZ
SCLK pulse width is high (tPWH)	10			ns
SCLK has a low pulse width (tPWL).	10			ns
CSB to SCLK time setting (tS)	1			ns
CSB to SCLK holding time (tH)	0			ns
SDIO to SCLK setting time (tDS)	1			ns
CSB to SCLK holding time (tDH)	0			ns
SCLK to SDIO /SDO data validity time (tDV)			1	ns
RESET pulse width is high.	10			ns
Wake-up time and output delay				
From the disabled DAC output		200		uS
Power off all equipment		1200		uS
DAC clock to analog output delay (dual-port mode)		7		Cycles
DAC clock to analog output delay (single-port mode)		8		Cycles

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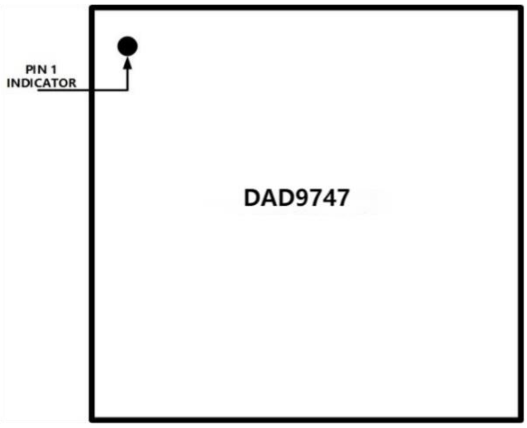
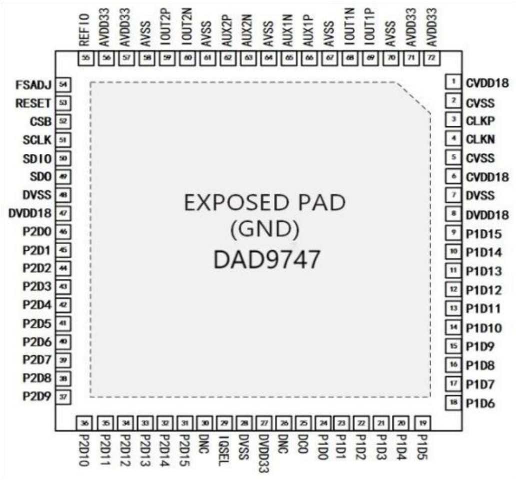
Pin Definitions and Function Descriptions





Pin No.	Symbol	Function Description
1, 6	CVDD18	Clock circuit 1.8V power supply
2, 5	CVSS	Clock circuit ground (0V)
3, 4	CLKP, CLKN	Differential clock input positive and negative terminals
7, 28, 48	DVSS	Digital ground (0V)
8, 47	DVDD18	Digital core voltage (1.8V)
9-24	P1D15-P100	Data port 1 input
26, 30	DNC	Suspended
25	DCO	Data clock output, which can be used as a data source clock.
27	DVDD33	Digital input/output power supply (3.3V)
29	IQSEL	I/Q frame signal in single-port mode
31-46	P2D15-P2D0	Digital Input Port 2
49	SDO	SPI data output signal
50	SDIO	SPI data input/output signals
51	SCLK	SPI clock input signal
52	CSB	SPI chip select signal, active low
53	RESET	Hardware reset, high-level reset
54	FSADJ	Full-scale current output adjustment requires a 10KΩ resistor.
55	REFIO	The reference voltage source outputs 1.2V, which is then connected to ground via a 0.1uF capacitor.
56, 57, 71, 72	ADVDD33	Analog power supply (3.3V)
58, 61, 64, 67, 70	AVSS	Analog ground (0V)
59, 60	IOUT2P, IOUT2N	DAC2 positive and negative current output
62, 63	AUX2P, AUX2N	Auxiliary DAC2 positive and negative current output
66, 65	AUX1P, AUX1N	Auxiliary DAC1 positive and negative current output
68, 69	IOUT1P, IOUT1N	DAC1 positive and negative current output
	EPAD	Exposed pads, soldered to the ground plane

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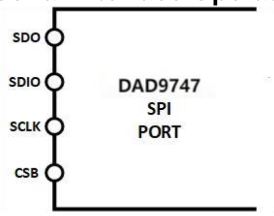
SPI Serial Interface Operation



The Serial Port (SPI) is a flexible synchronous serial communication port that can easily interface with a variety of industry-standard microcontrollers and microprocessors. Users can read and write to the DAD9747 via the SPI port and access all configuration registers. It supports both single-byte and multi-byte operations.

Data transmission, and high-order priority and low-order priority transmission modes. Serial data input and output can be implemented through a bidirectional SDIO pin or two unidirectional SDIO and SDO pins . The working mode of the serial port is controlled by register 0x00 bit [7] , and the configuration takes effect immediately after writing the last bit of the register.

The SPI communication cycle of the DAD9747 is divided into two phases. The first phase is the instruction cycle (writing the instruction byte to the device), which is synchronized with the first 8 rising edges of SCLK. The instruction byte provides the serial port controller with information about the data transmission cycle (and the second phase of the communication cycle), specifying whether the upcoming data transmission is a read or write operation, and the enable register for the first byte in the data transmission. The first 8 rising edges of SCLK in each communication cycle are used to write the instruction byte to the device.

When the CSB pin changes from logic high to logic low, the serial port timing is reset to the initial state of the instruction cycle. The first eight rising edges of SCLK from this state represent the instruction bit for the current I/O operation. The remaining SCLK bits are used for the second phase of the communication cycle. The second phase is where the actual data transmission occurs between the device and the system controller. One or more data bytes can be transmitted during the second phase of the communication cycle.

Data Format

The instruction bytes for the SPI port are shown in the table below:

MSB **LSB**

B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
R/W	N1	N0	A4	A3	A2	A1	A0

R/W : Bit 7 determines whether a read or write operation is performed after the instruction byte write cycle ends. 1 indicates a read operation, and 0 indicates a write operation.

Bits [6:5]: Bits 6 and 5 define the number of bytes transmitted. 00: Transmit one byte; 01: Transmit two bytes; 10: Transmit three bytes; 11: Transmit four bytes. Bits [4:0] of the A4 , A3 , A2 , A1 , and A0 instruction bytes determine the register address to be accessed during the data transmission phase of the communication cycle. For multi-byte transmissions, this address is the end address in MSB mode. In LSB mode , this address is the start byte address.

Serial Port (SPI) Pin Function Description

Serial clock (SCLK)

The serial clock pin is used to synchronize data input to and output to the device and to run the internal state machine. SCLK supports a frequency of 40MHz. All data input occurs on the rising edge of SCLK, and output occurs on the falling edge of SCLK.

Film Selection (CSB)

The chip select signal is active low and is used to initiate and signal a communication cycle. When the chip select is high, SDIO enters a high-impedance state. The chip select signal should remain low throughout the entire SPI communication process.

Serial Data Input/ Output (SDIO)

Both write and read operations to the device registers must be performed through this pin. It is a bidirectional data port, and data input is always completed through this pin. After power-on reset, this pin defaults to a bidirectional pin.

Serial Data Output (SDO)

device register data is the data output port. The enable of this pin is controlled by bit 7 of register 0x00. When this bit is set to '0' , SDO has no data output and is in a high-impedance state.

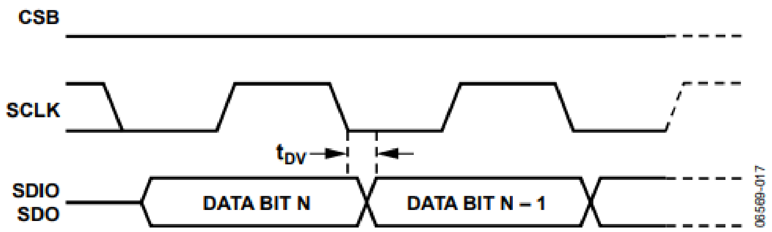


Figure 25. Timing Diagram for SPI Register Read

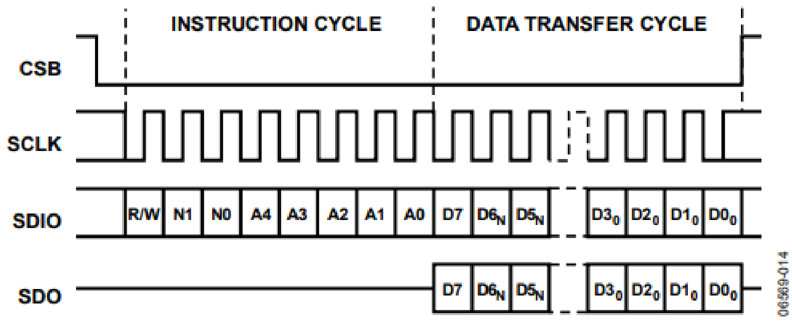


Figure 22. Serial Register Interface Timing—MSB First

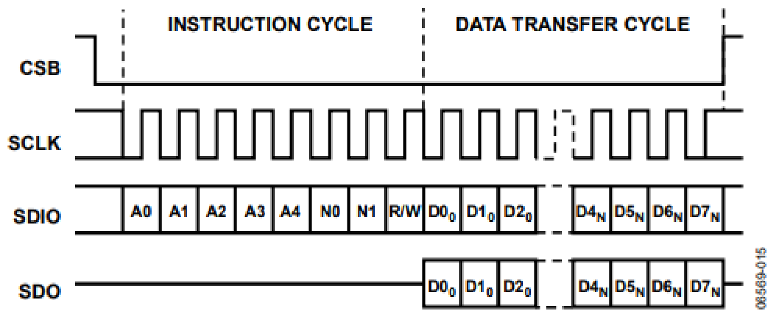


Figure 23. Serial Register Interface Timing—LSB First

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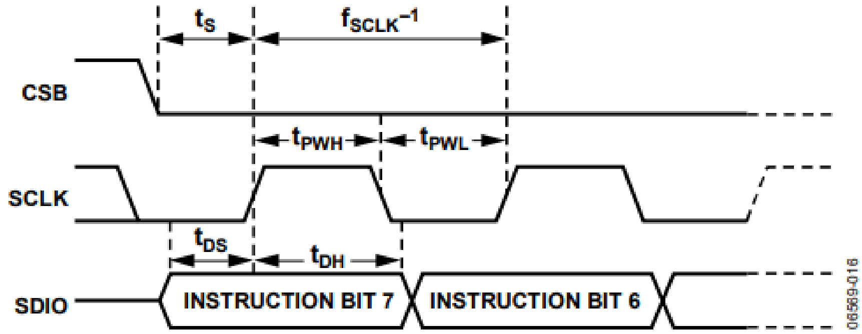

Figure 24. Timing Diagram for SPI Register Write

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SPI Register Description

Register name	Address	Bit	Name	Description
SPI Control Register	0x00	7	SDIODIR	0 = SPI is a four-wire operating mode, SDIO is an input pin.
				1 = SPI is a three-wire operating mode, SDIO is a bidirectional input/output pin.
		6	LSBFIRST	0 = LSBFIRST mode is off, SPI serial data format is MSB mode.
				0 = LSBFIRST mode enabled, SPI serial data format is LSB mode.
		5	SWRESET	0 = Normal working mode
				1 = Soft reset; restores all registers to their default state (except for register 0x00).
Data Control Register	0x02	7	DATATYPE	0 = Sets the DAC input data to two's complement format
				1 = Sets the DAC input data to unsigned binary format
		6	ONEPORT	0 = Standard dual-port input mode
				1 = Set the DAC input data to unsigned binary format
		4	INVDCO	1 = DCO output inverted
Power-Down Control Register	0x03	7	PD_DCO	1 = DCO output power failure
		5	PD_AUX2	1 = AUX2 DAC power failure
		4	PD_AUX1	1 = AUX 1 DAC power off
		3	PD_BIAS	1 = Reference voltage bias power off
		2	PD_CLK	1 = DAC clock input circuit power off
		1	PD_DAC2	1 = DAC 2 Analog output power failure
		0	PD_DAC1	1 = DAC 1 analog output power off
DAC Mode Control Register	0x0A	3 : 2	DAC1MODE[1 : 0]	00 = D AC1 operates in normal mode
				01 = DAC1 is operating in mixer mode
				10 = DAC1 is operating in zero-return mode
		1:0	ONEPORT	00 = D AC 2 is working in normal mode
				01 = DAC 2 operates in mixer mode
				10 = D AC 2 is operating in zero-return mode
DAC1 Gain Control Register	0x0B	7 : 0	DAC1FSC[7 : 0]	Scale output current adjustment word of DAC1 has 10 digits
	0X0C	1 : 0	DAC1FSC[9 : 8]	0x03FF = Sets the maximum full-scale current to 31.7mA
				0x0200 = Sets the full-amplitude current to the normal value of 20mA.
				0x0000 = Sets the full-amplitude current to the minimum value of 8.7mA.
Auxiliary DAC1 Control Register	0x0D	7 : 0	AUXDAC1[7 : 0]	The auxiliary DAC1 output current adjustment word has 10 bits. 0x03FF = Set the current output to 2mA 0x0200 = Sets the current output to 1mA 0x0000 = Sets the circuit output to 0mA
	0x0E	1 : 0	AUXDAC1[9 : 8]	
		7	AUX1PIN	1 = AUX1P output pin is active 0 = AUX1N output pin is valid
		6	AUX1DIR	0 = AUX1DAC output is in current sourcing mode
				1 = AUX1DAC output is in current sinking mode

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	0x0F	7 : 0	DA C2FSC[7 : 0]	Scale output current adjustment word of DAC1 has 10 digits
	0X10	1 : 0	D AC2FSC[9 : 8]	0x03FF = Sets the maximum full-amplitude current to 31.7mA.
				0x0200 = Sets the full-amplitude current to the normal value of 20mA.
				0x0000 = Sets the full-scale current to the minimum value of 8.7mA.
Auxiliary DAC2 Control Register	0x11	7 : 0	A UX D AC2[7 : 0]	The output current adjustment word of auxiliary DAC 2 has 10 bits. 0x03FF = Set the current output to 2mA. 0x0200 = Sets the current output to 1mA 0x0000 = Sets the circuit output to 0mA
	0x12	1 : 0	A UX D AC2[9 : 8]	
		7	AUX 2 PIN	1 = AUX2P output pin is active 0 = AUX2N output pin is active
		6	AUX 2 DIR	0 = AUX2DAC output is in current-pull mode
				1 = AUX2DAC output in current sinking mode

Digital Inputs and Outputs

The DAD9747 operates in two data input modes: dual-port and single-port. Upon power-on reset, it defaults to dual-port mode, where each DAC receives data from a fixed data input port. In single-port mode, both DACs receive data from data input port 1. In this mode, the data inputs of DAC 1 and DAC 2 are interleaved, and the IQSEL signal is used to indicate which DAC to interleave the data to. When IQSEL is high, data from port 1 is sent to DAC 1; when IQSEL is low, data from port 1 is sent to DAC 2. Due to the maximum data input port speed limit (250Msps), the DAC clock rate should not exceed 125MHz in single-port mode.

Data Input Timing

To ensure the DAC can correctly receive data input, a specific timing relationship must be met between the DAC 's clock signal (CLKP/N), the DCO, and the input ports. Below are the timing diagrams for the DAD9747 operating in two data modes.

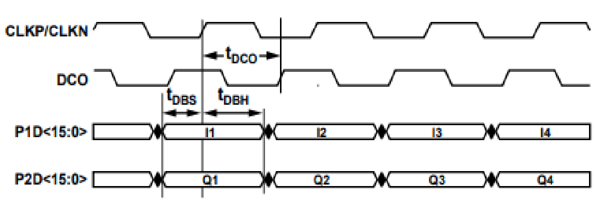

Figure 26. Data Interface Timing, Dual-Port Mode

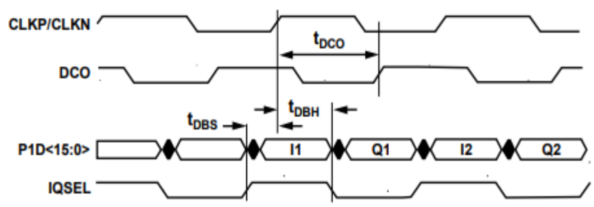

Figure 27. Data Interface Timing, Single-Port Mode

DAC Clock Input

To achieve analog output performance, a low-jitter clock signal is required for the DAC. The common-mode voltage of the clock is 400mV. The figures below show typical clock drive circuits for LVDS, CMOS /TTL, and positive/negative signals, respectively. A reference circuit for generating the clock common-mode voltage is also provided.

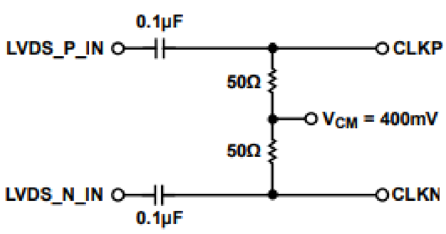

Figure 28. LVDS DAC Clock Drive Circuit

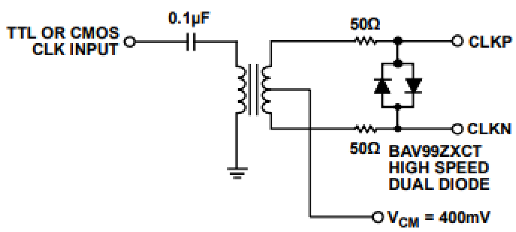

Figure 29. TTL or CMOS DAC Clock Drive Circuit

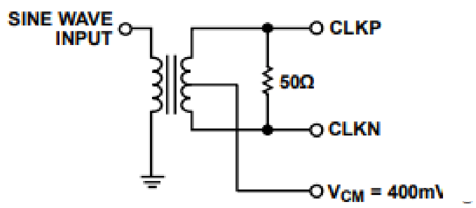

Figure 30. Sine Wave DAC Clock Drive Circuit

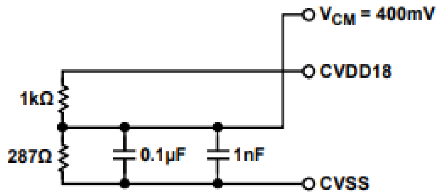

Figure 31. DAC Clock VCM Circuit

Analog Interface

Full-Amplitude Current Generation

The full-scale currents of DAC1 and DAC2 are functions of the current flowing through the pin FSADJ. During use, FSADJ needs to be connected to ground through a 10KΩ resistor. At the same time, REF IO needs to be connected to ground through a 0.1uF capacitor. The magnitude of the full-scale current of the DAC output can be adjusted by DAC1FSC [9 : 0] and DAC2FSC [9 : 0] .

The following formula shows the relationship between the DAC full-scale output current and the DACFSC.

IFS =1.2V/10000* (72+ (3 /16*DACnFSC))

DAC Transfer Function

Each channel of the DAD9747 provides complementary differential currents IOUTP and IOUTN . When all input digital signals are 1, IOUTP outputs the maximum current (full-scale current), while IOUTN outputs zero current. IOUTP and IOUTN are functions of the input digital signals.

IOUTP = (DAC DATA / 2^N) * IFS , IOUTN = ((2^N - 1) - DAC DATA) / 2^N * IFS, where DAC DATA is 0 to 2^N – 1 (a number in base). Thus, under load R, the values of VOUTP and VOUTN are IOUTP x * R and IOUTN * R, respectively. The output voltage is: VOUT = (IOUTP – IOUTN) * R

Work Mode Overview

It operates in three modes: normal mode, mixing mode, and zero-scale mode.

Auxiliary DAC

The DAD9747 integrates four 10-bit low-speed DACs. Two are used for internal direct gain adjustment of the output signals of DAC 1 and DAC 2 , while the other two output directly to an external chip, which can be used for output biasing of frame-skipping DACs. This provides flexible RF output port local oscillator leakage adjustment and image rejection adjustment functions for transmit systems using direct sampling quadrature modulators.

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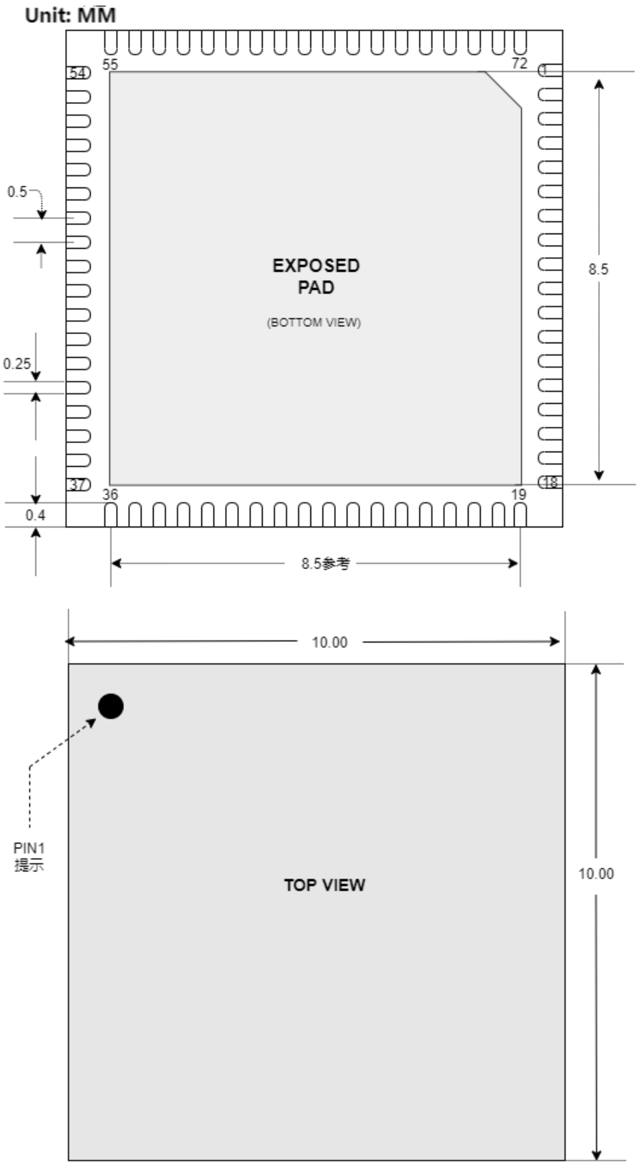
Encapsulation Information



Note: If there are vias on the PCB under the device, they must be covered or filled with solder mask to avoid short circuits.

Device Ordering Information List

Product Model	Temperature Range	Packaging	Package	RoHS
DAD9747	-40 ° C to +85 ° C	72-QFN	168/tray	Y

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