1. Characteristics

Resolution: 14-bit

- Sampling rate: 2.5 GSPS
- SFDR ≥ 55dBc @ fout = 950MHz
- Internal 1.2V reference voltage source
- Input data interface: LVDS

2. Application

- Broadband communication system
- Automatic testing instruments
- Base stations, handheld devices
- Radar, avionics equipment

3. Overview

The DAD9739 is a semiconductor integrated circuit manufactured using CMOS technology. This product features a segmented current-controlled structure, internally including an LVDS receiver, timing synchronization circuitry, bandgap reference source, SPI interface circuitry, clock receiving circuitry, and a 14-bit DAC core. This high-performance, high-frequency digital-to-analog converter can provide sampling rates up to 2500MHz and support multi-carrier signal generation within the Nyquist frequency range. It has an SPI interface, allowing for programming of numerous internal parameters and readback of the status register; it utilizes an LVDS interface to achieve a high sampling rate; and the output current is programmable from 8.66mA to 31.66mA. The product is packaged in a BGA160 plastic package and is functionally compatible with Analog Devices' AD9739A .

4. Device packaging information

Product Model	Packaging	Package Size
DAD9739	BGA160	12mm × 12mm

5. Functional Block Diagram

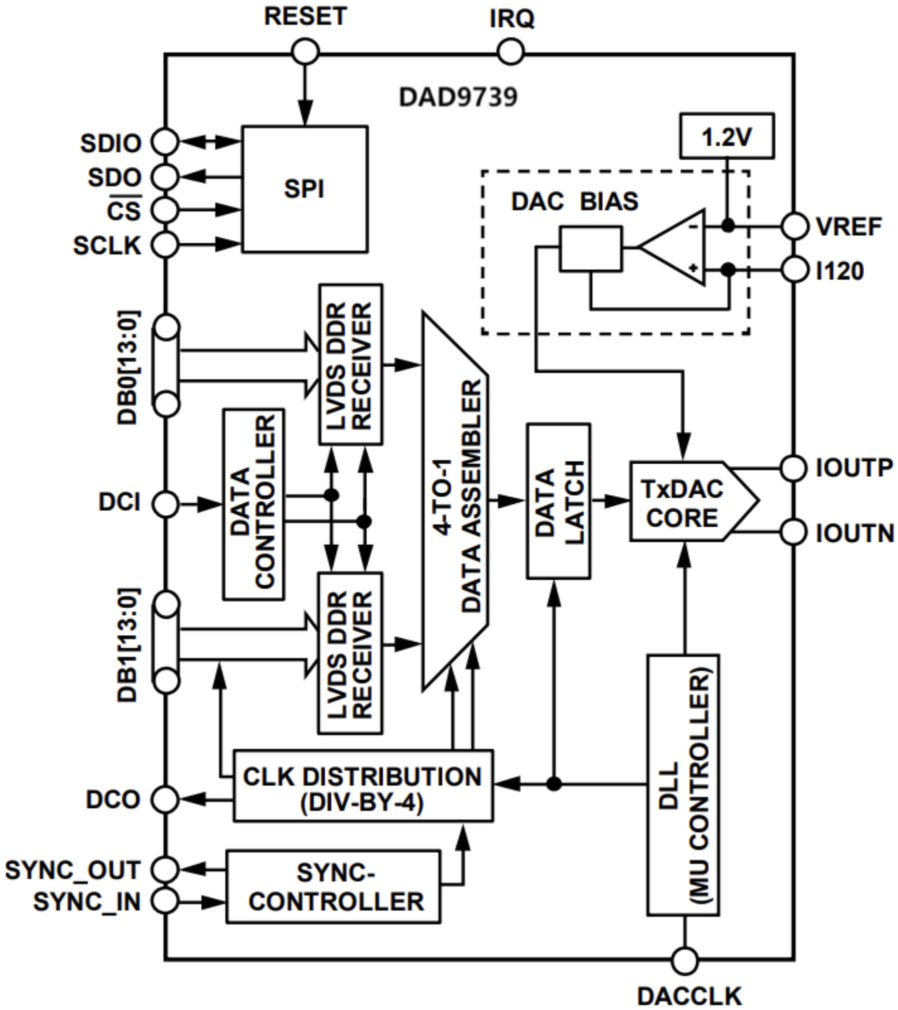

Figure 1

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6. Pin Configuration and Functions

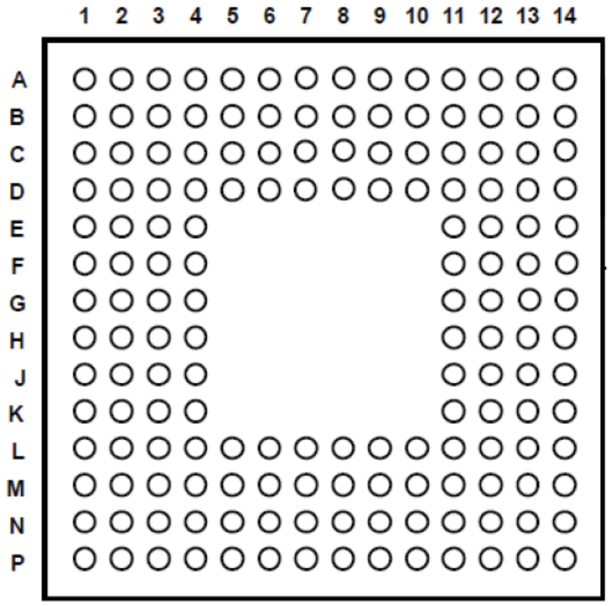

Figure 2. Pin configuration (top view)

Pin Functions

Pin No.	Symbol	Name	Pin No.	Symbol	Name
A1	GND_C	Clock power ground	H1	GND_D	Digital
A2	GND_C	Clock power ground	H2	GND_D	Digital
A3	GND_C	Clock power ground	H3	GND_D	Digital
A4	GND_C	Clock power ground	H4	GND_D	Digital
A5	GND_C	Clock power ground	H11	GND_D	Digital
A6	GND_{AS}	Analog ground shielding	H12	GND_D	Digital
A7	I_{OUTN}	Negative output terminal	H13	SCLK	Serial clock terminal
A8	I_{OUTP}	Positive output terminal	H14	SDO	Serial port data output
A9	GND_{AS}	Analog ground shielding	J1	SYNC_OUT_P	Multi-chip synchronous positive output
A10	V_{DDA}	Analog power supply	J2	SYNC_OUT_N	Multi-chip synchronous negative output
A11	V_{DDA}	Analog power supply	J3	V_{DD33}	3.3V digital power supply
A12	GNDA	Analog	J4	V_{DD33}	3.3V digital power supply
A13	GNDA	Analog	J11	V_{DD33}	3.3V digital power supply
A14	NC	Suspended	J12	V_{DD33}	3.3V digital power supply
B1	GND_C	Clock power ground	J13	DCO_P	Data clock output positive terminal
B2	GND_C	Clock power ground	J14	DCO_N	Data clock output negative terminal
B3	GND_C	Clock power ground	K1	SYNC_IN_P	Multi-chip synchronous positive input
B4	GND_C	Clock power ground	K2	SYNC_IN_N	Multi-chip synchronous negative input
B5	GND_C	Clock power ground	K3	GND_D	Digital
B6	GND_{AS}	Analog ground shielding	K4	GND_D	Digital
B7	I_{OUTN}	negative output terminal	K11	GND_D	Digital
B8	I_{OUTP}	Positive output terminal	K12	GND_D	Digital
B9	GND_{AS}	Analog ground shielding	K13	DCI_P	Data clock input positive terminal
B10	VDD_A	Analog power supply	K14	DCI_N	Data clock input negative terminal
B11	VDD_A	Analog power supply	L1	DB1[0]P	Port 1 Positive data input bit 0
B12	GND_A	Analog	L2	DB1[1]P	Port 1 Positive data input bit 1
B13	GND_A	Analog	L3	DB1[2]P	Port 1 Positive Data Input Bit 2
B14	I_{120}	Reference current	L4	DB1[3]P	Port 1 Positive Data Input Bit 3
C1	VDD_C	Clock power supply	L5	DB1[4]P	Port 1 Positive Data Input Bit 4
C2	VDD_C	Clock power supply	L6	DB1[5]P	Port 1 Positive Data Input Bit 5

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Pin No.	Symbol	Name	Pin No.	Symbol	Name
C3	CLK_N	Clock negative input	L7	DB1[6]P	Port 1 Positive Data Input Bit 6
C4	GND_C	Clock power ground	L8	DB1[7]P	Port 1 Positive Data Input Bit 7
C5	GND_C	Clock power ground	L9	DB1[8]P	Port 1 Positive Data Input Bit 8
C6	GND_{AS}	Analog ground shielding	L10	DB1[9]P	Port 1 Positive Data Input Bit 9
C7	I_{OUTN}	negative output terminal	L11	DB1[10]P	Port 1 Positive Data Input Bit 10
C8	I_{OUTP}	Positive output terminal	L12	DB1[11]P	Port 1 Positive Data Input Bit 11
C9	GND_{AS}	Analog ground shielding	L13	DB1[12]P	Port 1 Positive Data Input Bit 12
C10	VDD_A	Analog power supply	L14	DB1[13]P	Port 1 Positive Data Input Bit 13
C11	VDD_A	Analog power supply	M1	DB1[0]N	Port 1 Negative Data Input Bit 0
C12	GND_A	Analog	M2	DB1[1]N	Port 1 Negative Data Input Bit 1
C13	GND_A	Analog	M3	DB1[2]N	Port 1 Negative Data Input Bit 2
C14	V_{REF}	Reference voltage	M4	DB1[3]N	Port 1 Negative Data Input Bit 3
D1	VDD_C	Clock power supply	M5	DB1[4]N	Port 1 Negative Data Input Bit 4
D2	VDD_C	Clock power supply	M6	DB1[5]N	Port 1 Negative Data Input Bit 5
D3	CLK_P	Clock positive input	M7	DB1[6]N	Port 1 Negative Data Input Bit 6
D4	GND_C	Clock power ground	M8	DB1[7]N	Port 1 Negative Data Input Bit 7
D5	GND_C	Clock power ground	M9	DB1[8]N	Port 1 Negative Data Input Bit 8
D6	GND_{AS}	Analog ground shielding	M10	DB1[9]N	Port 1 Negative Data Input Bit 9
D7	I_{OUTN}	Negative output terminal	M11	DB1[10]N	Port 1 Negative Data Input Bit 10
D8	I_{OUTP}	Positive output terminal	M12	DB1[11]N	Port 1 Negative Data Input Bit 11
D9	GND_{AS}	Analog ground shielding	M13	DB1[12]N	Port 1 Negative Data Input Bit 12
D10	VDD_A	Analog power supply	M14	DB1[13]N	Port 1 Negative Data Input Bit 13
D11	VDD_A	Analog power supply	N1	DB0[0]P	Port 0 Positive Data Input Bit 0
D12	VDD_A	Analog	N2	DB0[1]P	Port 0 Positive Data Input Bit 1
D13	VDD_A	Analog	N3	DB0[2]P	Port 0 Positive Data Input Bit 2
D14	I_{PTAT}	Test pin	N4	DB0[3]P	Port 0 Positive Data Input Bit 3
E1	VDD_C	Clock power supply	N5	DB0[4]P	Port 0 positive Data Input Bit 4
E2	VDD_C	Clock power supply	N6	DB0[5]P	Port 0 Positive Data Input Bit 5
E3	VDD_C	Clock power supply	N7	DB0[6]P	Port 0 Positive Data Input Bit 6
E4	VDD_C	Clock power supply	N8	DB0[7]P	Port 0 Positive Data Input Bit 7
E11	GND_{AS}	Analog ground shielding	N9	DB0[8]P	Port 0 Positive Data Input Bit 8
E12	GND_{AS}	Analog ground shielding	N10	DB0[9]P	Port 0 Positive Data Input Bit 9
E13	GND_{AS}	Analog ground shielding	N11	DB0[10]P	Port 0 Positive Data Input Bit 10
E14	GND_{AS}	Analog ground shielding	N12	DB0[11]P	Port 0 Positive Data Input Bit 11
F1	GND_{AS}	Analog ground shielding	N13	DB0[12]P	Port 1 Positive Data Input Bit 12
F2	GND_{AS}	Analog ground shielding	N14	DB0[13]P	Port 0 Positive Data Input Bit 13
F3	GND_{AS}	Analog ground shielding	P1	DB0[0]N	Port 0 Negative Data Input Bit 0
F4	GND_{AS}	Analog ground shielding	P2	DB0[1]N	Port 0 Negative Data Input Bit 1
F11	GND_{AS}	Analog ground shielding	P3	DB0[2]N	Port 0 Negative Data Input Bit 2
F12	GND_{AS}	Analog ground shielding	P4	DB0[3]N	Port 0 Negative Data Input Bit 3
F13	IRQ	Interruption Request	P5	DB0[4]N	Port 0 Negative Data Input Bit 4
F14	RESET	Reset	P6	DB0[5]N	Port 0 Negative Data Input Bit 5
G1	V_{DD}	1.8V digital power supply	P7	DB0[6]N	Port 0 Negative Data Input Bit 6
G2	V_{DD}	1.8V digital power supply	P8	DB0[7]N	Port 0 Negative Data Input Bit 7
G3	V_{DD}	1.8V digital power supply	P9	DB0[8]N	Port 0 Negative Data Input Bit 8
G4	V_{DD}	1.8V digital power supply	P10	DB0[9]N	Port 0 Negative Data Input Bit 9
G11	V_{DD}	1.8V digital power supply	P11	DB0[10]N	Port 0 Negative Data Input Bit 10
G12	V_{DD}	1.8V digital power supply	P12	DB0[11]N	Port 0 Negative Data Input Bit 11
G13	CS	Serial port enable pin	P13	DB0[12]N	Port 0 Negative Data Input Bit 12
G14	SDIO	Serial port data input / output	P14	DB0[13]N	Port 0 Negative Data Input Bit 13

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7. Performance Index

Unless otherwise specified, V_{DDA} = 3.3V, V_{DD33} = 3.3V, V_{DDC} = 1.8V, V_{DD} = 1.8V, f_{CLK} = 2.5GHz, -40℃≤T_A≤85 ℃ .

Name	Symbol	Condition	Limit value		Unit
			Min	Max	
Reference voltage	V_{REF}		1.15	1.25	V
Linear error	E_L		-3	3	LSB
Differential linearity error	E_{DL}		-3	3	LSB
Power consumption	P_W	f_o = 100MHz	—	1.25	W
Stray dynamic range	SFDR	f_o = 100MHz, normal mode	62	—	dBc
		f_o = 950MHz, normal mode	46	—	dBc
Functional testing		mudelay timing control function	powering on the configuration circuit and enabling the multi-delay timing control function, read back bit <0> of register 0x2A. If it is 1, it indicates that the function is normal.		
		LVDS interface timing control function	powering on the circuit and enabling the LVDS interface timing control function, read back bit<0> of register 0x21. If it is 1, it means the function is normal.		

8. Absolute Maximum Ratings

Name	Parameter
Analog power supply voltage (V_{DDA})	3.6V
1.8V digital power supply voltage (V_{DD})	1.98V
3.3V digital power supply voltage (V_{DD33})	3.63V
Clock power supply voltage (V_{DDC})	1.98V
Junction temperature (T_J)	150℃
Storage temperature (T_{stg})	-55℃~125℃

9. Recommended Operational Conditions

Name	Parameter
Analog power supply voltage (V_{DDA})	3.135V~3.465V
1.8V digital power supply voltage (V_{DD})	1.71V~1.89V
3.3V digital power supply voltage (V_{DD33})	3.135V~3.465V
Clock power supply voltage (V_{DDC})	1.71V~1.89V
Operating temperature (T_A)	-40℃~85℃

10. Serial Port Interface Register

- **SPI interface**

The DAD9739 uses an SPI interface, allowing easy connection to many industry-standard microcontrollers and microprocessors. This serial I/O port is compatible with most synchronous transmission formats, including Motorola SPI and Inter SSR protocols. This interface allows read/write access to all registers that configure the DAD9739. It supports single-byte or multi-byte transmissions, and MSB-first or LSB-first transmission formats. The DAD9739 serial interface port can be configured with one bidirectional pin I/O (SDIO) or two unidirectional input/output pins (SDIO/SDO).

1) Serial interface typical operating conditions

The DAD9739 has two phases. Phase 1 is the instruction cycle, used to write an instruction byte to the DAD9739, corresponding to the first group of eight rising edges of SCLK, as shown in Table 1. The instruction byte in Phase 1 defines whether the upcoming data transfer is a read or a write, and the register address corresponding to the data transfer of the first byte. The first group of eight rising edges of SCLK in each communication cycle is typically used to write the instruction byte to the DAD9739.

Table 1. Description of Instruction Bytes

MSB							LSB
17	16	15	14	13	12	11	10
Reading/Writing	A6	A5	A4	A3	A2	A1	A0

The remaining SCLK edge is used for phase 2 of the communication cycle. Phase 2 is the actual data transmission between the DAD9739 and the system controller. The CSB (chip select) signal can rise every 8 bits to stop the transmission path. When the CSB goes low, the transmission of unfinished data continues. If it does not stop at a byte boundary, the SPI is reset. The SPI read/write operation timing is shown in Figure 3. For both read and write operations, the instruction cycle is triggered by the rising edge of the clock to write information. During a write operation, the communication cycle writes input data on the rising edge of the clock, and during a read operation, the communication cycle updates output data on the falling edge of the clock.

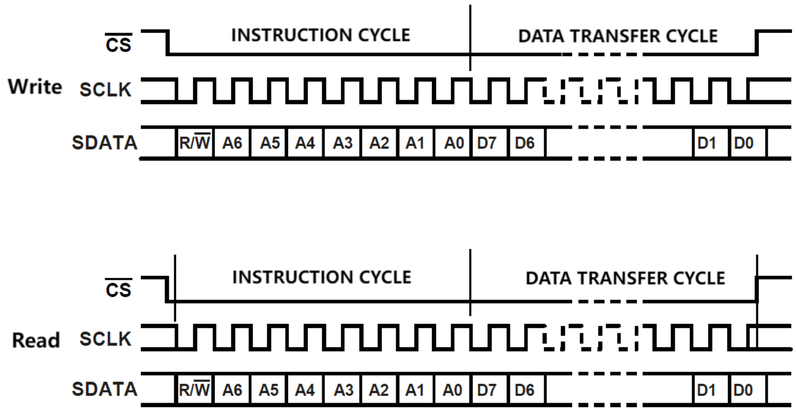

Figure 3. SPI read / write operation timing diagram

2) SPI port description

SCLK - Serial Clock: The maximum operating frequency of SCLK is 20MHz.

CSB - Chip Select: Active low to start the communication cycle and defines one communication cycle. Allows multiple devices to use the same serial channel. When this port input is high, ports SDO and SDIO become high impedance. The chip select signal should remain low throughout the communication cycle.

SDIO - Serial Data I/O Port: Data is always written to the DAD9739 from this port. Additionally, this port can also be used as a bidirectional data line. This port is configured by SDIO_DIR (Reg.0, Bit7). The default value is 0, which configures SDIO as a unidirectional port.

SDO - Serial Data Output: Data is read from this port. When the DAD9739 is operating in bidirectional I/O mode, this port cannot output data and is set to a high-impedance state.

MSB/LSB Transmission: The DAD9739 supports both MSB-first and LSB-first data formats. This function is controlled by LSBFIRST (Reg.0, Bit6). The default is MSB first (LSBFIRST=0).

When LSBFIRST = 0 (MSB first), instruction and data bytes must be written in order from the most significant bit to the least significant bit.

When LSBFIRST = 1 (LSB first), instruction and data bytes must be written in order from least significant bit to most significant bit.

3) Precautions for SPI operation

The DAD9739 serial port configuration is controlled by Reg.0, Bit4, Bit5, Bit6, and Bit7. Note that the configuration changes immediately after the last bit is written to the register. When the last bit of the instruction is written to the SDIO port, the path rotation drive signal must be set to a high-impedance state in a timely manner. The DAD9739 's serial output signal is enabled by the falling edge of SCLK. This results in the first output data bit being shorter than the other data bits.

4) SPI Register Table

Name	Hexa-decimal	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
Mode	00	SDIO_DIR	LSB/MSB	Reset	N/A	N/A	N/A	N/A	N/A	0x00
Power-Down	01	N/A	N/A	LVDS_DRVR_PD	LVDS_RCVR_PD	N/A	N/A	CLK_RCVR_PD	DAC_BIAS_PD	0x00
CNT_CLK_DIS	02	N/A	N/A	N/A	N/A	CLKGEN_PD	N/A	REC_CNT_CLK	MU_CNT_CLK	0x03
IRQ_EN	03	N/A	N/A	SYNC_LST_EN	SYNC_LCK_EN	MU_LST_EN	MU_LCK_EN	RCV_LST_EN	RCV_LCK_EN	0x00
IRQ_REQ	04	N/A	N/A	SYNC_LST_IQR	SYNC_LCK_IQR	MU_LST_IQR	MU_LCK_IQR	RCVLST_IRQ	RCVLCK_IRQ	0x00

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RSVD	05	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
FSC_1	06	FSC[7]	FSC[6]	FSC[5]	FSC[4]	FSC[3]	FSC[2]	FSC[1]	FSC[0]	0x00
FSC_2	07	Sleep	N/A	N/A	N/A	N/A	N/A	FSC[9]	FSC[8]	0x02
DEC_CNT	08	N/A	N/A	N/A	N/A	N/A	N/A	DAC_DEC[1]	DAC_DEC[0]	0x00
RSVD	09	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
L VDS_CNT	0A	N/A	N/A	N/A	N/A	HNDOFF_CHK_RST	N/A	LVDS_Bias[1]	LVDS_Bias[0]	0x00
DIG_STAT	0B	HNDOFF_Fall[3]	HNDOFF_Fall[2]	HNDOFF_Fall[1]	HNDOFF_Fall[0]	HNDOFF_Rise[3]	HNDOFF_Rise[2]	HNDOFF_Rise[1]	HNDOFF_Rise[0]	RNDM
LVDS_STAT1	0C	SUP/HLD_Edge1	N/A	DCI_PHS3	DCI_PHS1	DCI_PRE_PH2	DCI_PRE_PH0	DCI_PST_PH2	DCI_PST_PH0	RNDM
LVDS_STAT2	0D	SUP/HLD_SYNC	SUP/HLD_Edge0	SYNC_SAMP1	SYNC_SAMP0	LVDS1_HI	LVDS1_LO	LVDS0_HI	LVDS0_LO	RNDM/0
RSVD	0E	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
RSVD	0F	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LVDS_REC_CNT1	10	SYNC_FLG_RST	SYNC_LOOP_ON	SYNC_MST/SLV	SYNC_CNT_ENA	N/A	RCVR_FLG_RST	RCVR_LOOP_ON	RCVR_CNT_ENA	0x42
LVDS_REC_CNT2	11	SMP_DEL[1]	SMP_DEL[0]	FINE_DEL_MID[3]	FINE_DEL_MID[2]	FINE_DEL_MID[1]	FINE_DEL_MID[0]	RCVR_GAIN[1]	RCVR_GAIN[0]	0xDD
LVDS_REC_CNT3	12	SMP_DEL[9]	SMP_DEL[8]	SMP_DEL[7]	SMP_DEL[6]	SMP_DEL[5]	SMP_DEL[4]	SMP_DEL[3]	SMP_DEL[2]	0x29
LVDS_REC_CNT4	13	DCI_DEL[3]	DCI_DEL[2]	DCI_DEL[1]	DCI_DEL[0]	FINE_DEL_SKW[3]	FINE_DEL_SKW[2]	FINE_DEL_SKW[1]	FINE_DEL_SKW[0]	0x71
LVDS_REC_CNT5	14	CLKDIVPH[1]	CLKDIVPH[0]	DCI_DEL[9]	DCI_DEL[8]	DCI_DEL[7]	DCI_DEL[6]	DCI_DEL[5]	DCI_DEL[4]	0x0A
LVDS_REC_CNT6	15	SYNC_GAIN[1]	SYNC_GAIN[0]	SYNCOUT_PH[1]	SYNCOUT_PH[0]	LCKTHR[3]	LCKTHR[1]	LCKTHR[2]	LCKTHR[0]	0x42
LVDS_REC_CNT7	16	N/A	SYNCO_DEL[6]	SYNCO_DEL[6]	SYNCO_DEL[6]	SYNCO_DEL[6]	SYNCO_DEL[6]	SYNC_DEL[6]	SYNCO_DEL[6]	0x00
LVDS_REC_CNT8	17	SYNCSH_DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_REC_CNT9	18	SYNCSH_DEL[8]	SYNCSH_DEL[7]	SYNCSH_DEL[6]	SYNCSH_DEL[5]	SYNCSH_DEL[4]	SYNCSH_DEL[3]	SYNCSH_DEL[2]	SYNCSH_DEL[1]	0x00
LVDS_REC_STAT1	19	SMP_DEL[1]	SMP_DEL[0]	N/A	N/A	SMP_FINE_DEL[3]	SMP_FINE_DEL[2]	SMP_FINE_DEL[1]	SMP_FINE_DEL[0]	0xC7
LVDS_REC_STAT2	1A	SMP_DEL[9]	SMP_DEL [8]	SMP_DEL[7]	SMP_DEL[6]	SMP_DEL[5	SMP_DEL[4	SMP_DEL[3]	SMP_DEL[2]	0x29
LVDS_REC_STAT3	1B	DCI_DEL[1]	DCI_DEL[0]	N/A	N/A	SYNCOUT PH[1]	SYNCOUT PH[0]	CLKDIV PH[1]	CLKDIV PH[0]	0xC0
LVDS_REC_STAT4	1C	DCI_DEL[9]	DCI_DEL[8]	DCI_DEL[7]	DCI_DEL[6]	DCI_DEL[5]	DCI_DEL[4]	DCI_DEL[3]	DCI_DEL[2]	0x29
LVDS_REC_STAT5	1D	FINE_DEL_PST[3]	FINE_DL_PST[2]	FINE_DEL_PST[1]	FINE_DEL_PST[0]	FINE_DEL_PRE[3]	FINE_DEL_PRE[2]	FINE_DEL_PRE[1]	FINE_DEL_PRE[0]	0x86
LVDS_REC_STAT6	1E	N/A	SYNCO_DEL[6]	SYNCO_DEL[5]	SYNCO_DEL[4]	SYNCO_DEL[3]	SYNCO_DEL[2]	SYNC_DEL[1]	SYNCO_DEL[0]	0x00
LVDS_REC_STAT7	1F	SYNCSH _DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_REC_STAT8	20	SYNCSH_DEL[8]	SYNCSH_DEL[7]	SYNCSH_DEL[6]	SYNCSH_DEL[5]	SYNCSH_DEL[4]	SYNCSH_DEL[3]	SYNCH_DEL[2]	SYNCSH_DEL[1]	0x00
LVDS_REC_STAT9	21	SYNC_TRK_ON	SYNC_INIT_ON	SYNC_LST_LCK	SYNC_LCK	RCVR_TRK_ON	RCVR_FE_ON	RCVR_LST	RCVR_LCK	0x00

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CROSS_CNT1	22	N/A	N/A	N/A	DIR_P	CLKP_OFFSET[3]	CLKP_OFFSET[2]	CLKP_OFFSET[1]	CLKP_OFFSET[0]	0x00
CROSS_CNT2	23	N/A	N/A	N/A	DIR_N	CLKN_OFFSET[3]	CLKN_OFFSET[2]	CLKN_OFFSET[1]	CLKN_OFFSET[0]	0x00
PHS_ DET	24	N/A	N/A	CMP_BST	PHS_DET AUTO_EN	Bias[3]	Bias[2]	Bias[1]	Bias[0]	0x00
MU_ DUTY	25	MU_DUTYAUTO_EN	POS/NEG	ADJ[5]	ADJ[4]	ADJ[3]	ADJ[2]	ADJ[1]	ADJ[0]	0x00
MU_CNT1	26	N/A	Slope	Mode[1]	Mode[0]	Read	Gain[1]	Gain[0]	Enable	0x42
MU_CNT2	27	MUDEL[0]	SRCH_MODE[1]	SRCH_MODE[0]	SET_PHS[4]	SET_PHS[3]	SET_PHS[2]	SET_PHS[1]	SET_PHS[0]	0x40
MU_CNT3	28	MUDEL[8]	MUDEL[7]	MUDEL[6]	MUDEL[5]	MUDEL[4]	MUDEL[3]	MUDEL[2]	MUDEL[1]	0x00
MU_CNT4	29	SEARCH_TOL	Retry	CONTRST	Guard[4]	Guard[3]	Guard[2]	Guard[1]	Guard[0]	0x0B
MU_STAT1	2A	N/A	N/A	N/A	N/A	N/A	N/A	MU_LOST	MU_LKD	0x00
RSVD	2B	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
RSVD	2C	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
ANA_CNT1	32	HDRM[7]	HDRM[6]	HDRM[5]	HDRM[4]	HDRM[3]	HDRM[2]	HDRM[1]	HDRM[0]	0xCA
ANA_CNT2	33	N/A	N/A	N/A	N/A	N/A	N/A	MSEL[1]	MSEL[0]	0x03
RSVD	34	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
PART ID	35	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0x20

11. Working Principle

- **Work mode**

The DAD9739 can operate in three modes: Normal mode, Return-to-Zero mode, and Mixer mode. Normal mode is best suited for operation in the first Nyquist region, maximizing signal power; Return-to-Zero mode is best suited for operation in the second Nyquist region, minimizing roll-off; and Mixer mode is best suited for operation in the second/third Nyquist region, maximizing signal power. Different operating modes can be achieved by modifying bits <1:0> of 0x08 via SPI. The corresponding relationships are shown in Table 2.

Table 2. Operating Modes of DAD9739

0x08: Bit<1:0>	Function
0 0	Normal mode
0 1	Zeroing mode
1 0	Mixing mode

- **Drive DACCLK input**

The common-mode clock input of the DAD9739 is generated internally by the circuit and is CLKVDD/2 (0.9V). Therefore, AC coupling is required to provide the clock to the DAD9739. To optimize the clock duty cycle, the DAD9739 adds a clock common-mode point adjustment circuit, which sets DIR_P, DIR_N, CLKP_OFFSET, and CLKN_OFFSET via SPI. DIR_P and DIR_N represent the direction of change of the common-mode point at the P and N terminals of CLK; a low level indicates a decrease in the clock common-mode point, and a high level indicates an increase. CLKP_OFFSET and CLKN_OFFSET represent the magnitude of the change in the common-mode point at the P and N terminals, with a maximum value of 15. Since the DAD9739 uses a pseudo-differential input structure, the common-mode points of the P and N terminals of CLK can be set independently. When the common-mode points of the P and N terminals change in the same direction, the duty cycle of the differential clock is adjusted. When the common-mode points of the P and N terminals change in opposite directions, the crossover point of the P and N terminals is adjusted.

- **Micro-delay timing adjustment settings**

The DAD9739 uses a delay-locked loop (PLL) to optimize timing between its internal digital and analog domains, ensuring correct data reception even at high speeds of 2.5 GSPS. The DAC clock is split into an analog path and a digital path. The analog path clock is directly input to the DAC core (to reduce jitter), while the digital path clock is input to a programmable delay line. The delay line's output clock serves as the entire internal digital master clock, supplying all other internal and external digital clocks. The mu delay controller manages the total delay of the digital path, optimizing timing between the two clock domains while continuously tracking any changes (in track mode) to ensure correct data reception. The mu delay controller adjusts the timing between the digital and analog domains via a tapped digital delay line with a total delay of 864 ps. Digitizing the delay value into a 9-bit precision binary number (decimal from 0 to 432) using the MUDEL register results in a 2 ps LSB. Because a phase shift corresponds to a delay at a fixed clock frequency, the control loop essentially compares the phase relationship between two clock domains and adjusts the phase of the digital domain clock (via tapped delay lines) to equal the set phase shift

(SET_PHS). After the mu delay controller completes the search and locks onto the target mu phase value, it maintains a fixed timing relationship between the two clock domains within the specified temperature and power supply range. If the mu delay setting required by the mu delay controller exceeds the range of the tapped delay lines (less than 0 or greater than 432), it may lose lock, leading to a system interrupt (in which case an IRQ can be generated or the search can be restarted). To avoid this hypothetical situation, it is recommended to use symmetrical guard bands at both ends of the mu delay value range. The recommended guard band setting is 11 (Register 0x29 = 0xCB), corresponding to 88 LSBs of the MUDEL.

1) mu delay controller working status

The mu delay controller is enabled via register 0x26 Bit0. Before enabling, the phase comparator (Regiser0x24 Bits[5:4]) and the mu delay controller duty cycle adjustment circuit (Regiser0x25 Bit7) should be enabled. The mu delay controller has three operating modes, determined by Mode[1:0] and Regiser0x26 Bits[5:4] as follows:

- Search and Tracking (0x0) (Optimal Settings)
- Track only (0x1)
- Search only (0x2)

1. Search mode

The search algorithm begins with an initial value, which can be set via MUDEL[8:0] (MUDEL[0], Bit7 of Register 0x27 and Bits[7:0] of Register 0x28). Although the delay line has 9 bits of precision, the maximum mu delay value is 432 (decimal). The optimal point to start the search is the middle of the delay line, i.e., 216. The initial search algorithm scans different mu delay values until it finds the set phase value, which is set by Bits[4:0] of SetPhs Register 0x27, with a maximum value of 16. When the set phase value is found, the phase slope is calculated and compared with the set slope, set via the Slope bit of Register 0x26. A positive slope indicates that the phase value increases as the mu delay increases, and a negative slope indicates that the phase value decreases as the mu delay increases. If both the phase value and the slope match, the search algorithm ends. The Search_Tol bit (Register 0x29, Bit7) is used to specify the search precision:

- Inaccurate (0x0) — Can find phase values within two values of the specified phase value
- Precise (0x1) — Finds the specified phase value (optimal setting)

The search direction can be specified using SrchMode[1:0] and Bits[6:5] of Register 0x27. There are three options:

- Downwards only (0x0)
- Only upwards (0x1)
- Alternate up and down (0x2) (Optimal setting)

If the mode is alternating up and down, the search proceeds in both directions until one side reaches the guard band. The search then continues, but only in the opposite direction. If the set phase value is not found before reaching the guard band in this direction, the search reverts to the alternating up and down mode and continues within the guard band. The search fails if the mu delay controller reaches the endpoint. If the controller does not find the set phase value in the previously described search, Bit 5 of ContRst , Register 0x29, determines the corrective action:

- Continue (0x0) — Continue searching (best settings)
- Reset (0x1)

2. Tracking mode

In tracking mode, a control loop increments, decrements, or leaves the mu delay value unchanged based on the measured phase value. The controller determines whether to increment or decrement the mu delay value based on the set slope. The user can identify the control loop's operating state using two status bits: MU_LKD (Regiser 0x2A, Bit0) and MU_LOST (Register 0x2A, Bit1). MU_LKD is cleared if the current phase is more than 5 steps away from the set phase; MU_LOST is set to 1 if a lock was previously acquired. Furthermore, if a lock is lost, the controller can choose to continue tracking or restart the search. By setting the read bit high (Register 0x26, Bit3), the user can read back the mu delay and phase values when the controller was locked (via MUDEL[8:0] and SetPhs[4:0]). The mu delay and phase values set at the start of the search cannot be read back at this time. The typical lock time of the mu delay controller is approximately 180K DAC cycles (approximately 90μs at 2GSPS).

- **LVDS Interface Timing Settings**

The DAD9739 employs a dual-channel 14-bit LVDS data interface. Due to data skew and jitter, to ensure reliable data transmission, it's crucial to minimize skew and jitter on the FPGA and PCB, and to ensure the clock sampling time is centered within the data frame. To optimize data reception timing, a dedicated accompanying clock (DCI) is provided. This DCI uses the same generation method as the data, but consists of a set of "010101..." data. The changing edge of the DCI represents the data edge. By comparing the phase of the DCI and the sampling clock, the optimal sampling time—that is, the sampling time being in the middle of the stable and valid data period—is found. Specifically, the DAD9739 uses the interface structure shown in Figure 4. This structure adjusts the DCI delay line to align the 0° four-way clock with the DCI edge, and assigns this DCI delay setting value to the SMP delay line. Since this delay line is a 90° four-way clock, the clock sampling edge is precisely in the middle of the stable and valid data period.

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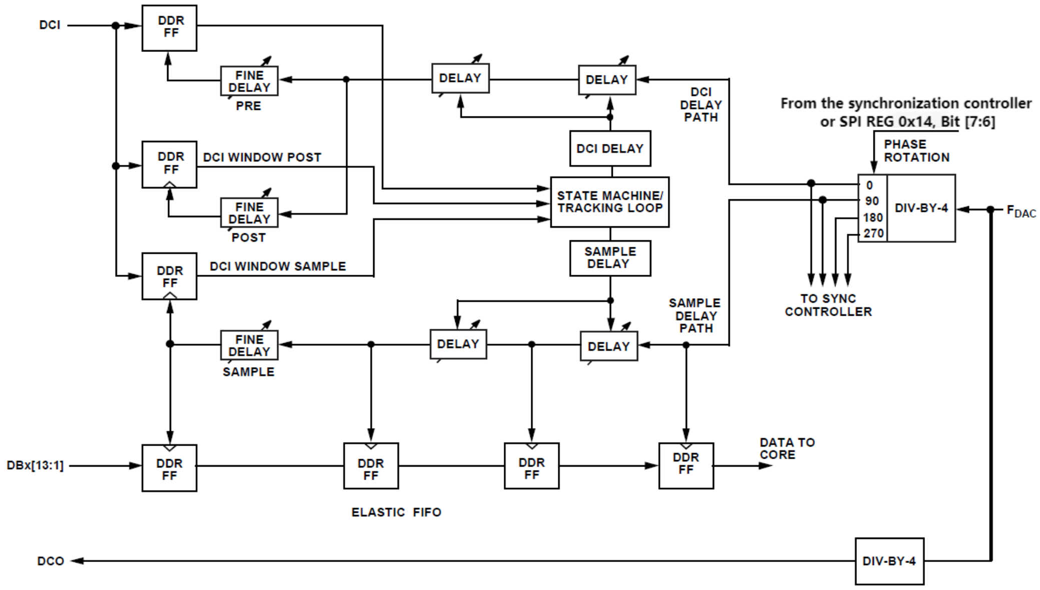

Figure 4. Schematic diagram of LVDS receiver circuit

When in use, there are automatic mode (controller enabled) and manual mode (controller disabled) to choose from. The window width can be set from 1 to 7 (default is 2) and the delay line can be set from 0 to 334 (default is 167) through the SPI control register. Automatic mode takes 135k DAC clock cycles by default.

Recommended operating steps are as follows:

1) Set the window width to 2, which is 0x13=72. At this time, DCI_DEL and SMP_DEL are 167, which are the default optimal values.
2) The controller is disabled, i.e., 0x10 = 0x00.
3) The controller is enabled by two operations: 0x10 = 0x02 and 0x10 = 0x13.
4) Waiting for 135k DAC clock cycles.
5) Read back and confirm the value in register 0x21. If it is 0x09, the search is successful and the tracing mode has been entered.
6) If the input data rate is less than 1.6 GSPS, read back the DCI_DEL value to confirm whether it is within the range set by the user. If not, flip CLKDIVPH (i.e., 0x14 , Bit[7:6]) and return to step 2.

- **Power-on sequence**

The 1.8V power supply must be active before the 3.3V power supply. When the 1.8V power supply fails, the 3.3V power supply cannot be applied.

- **Recommended configuration process**

Table 3. Recommended target Mu phase settings and clock rates

Clock rate (GSPS)	Slope	Mu Phase
0.8	-	6
0.9	-	4
1.0	+	5
1.1	+	8
1.2	+	1 2
1.3	-	1 2
1.4	-	1 0
1.5	-	8
1.6 to 2.5	-	6

Table 4. SPI configuration process when multi-chip synchronization is disabled

Step	Address	Written value	Description
1	0x00	0x00	Configure four-wire SPI mode. Bits [7:5] must be mirrored to bits [2:0] because the MSB/LSB format is unknown at power-up.
2	0x00	0x20	The software resets the SPI value to the default value.
3	0x00	0x00	Remove the reset bit.
4	0x22	0x0F	Set the common-mode voltages of the input differential clocks DACCLK_P and DACCLK_N.
5	0x23	0x0F	

6	0x24	0x30	When configuring the micro-delay unit controller, the target slope and target phase values of the micro-delay unit should be set according to Table 3 at different master clock frequencies.
7	0x25	0x80	
8	0x27	0x4C	
9	0x28	0x6C	
1 0	0x29	0xCB	
1 1	0x26	0x02	
1 2	0x26	0x03	Enables the search and track mode of the microdelay unit controller.
1 3	N/A	N/A	Waiting for 160k master clock cycles.
1 4	0x2A		Read back register 0x2A and confirm its value is 0x01 to ensure the DLL loop is locked. If it is not locked, return to step 10 and repeat the operation. After three attempts without locking, break the loop and report a microdelay unit failure.
1 5	N/A	N/A	Ensure that the data input of the DAD9739 is fed by the DCI clock.
1 6	0x13	0x72	Set the window width to 2.
1 7	0x10	0x00	Before enabling the data receiving controller, disable the data receiving controller.
1 8	0x10	0x02	Enable the data receive controller to establish a loop and respond to interrupts.
1 9	0x10	0x03	Enable the data receiving controller to enter search and track mode.
20	N/A	N/A	Waiting for 135k master clock cycles.
twenty one	0x21		Read back register 0x21 to ensure it equals 0x09 to confirm the DLL loop is locked and in a traced state. If not, toggle bits [7:6] of register 0x14 and return to step 17, repeating the operation. After three attempts without locking, disconnect the loop and report a data receive lock failure.
twenty two	0x06, 0x07	0x00, 0x02	Optional: Modify the DAC's full-amplitude output current (default is 20mA).
twenty three	0x08	0x00	Optional: Modify the DAC's operating mode (default is normal mode).

Table 5. SPI configuration process when multi-chip synchronization is enabled

Step	Address	Written value	Description
1	0x00	0x00	Configure four-wire SPI mode. Bits [7:5] must be mirrored to bits [2:0] because the MSB/LSB format is unknown at power-up.
2	0x00	0x20	The software resets the SPI value to the default value.
3	0x00	0x00	Remove the reset bit.
4	0x22	0x0F	Set the common-mode voltages of the input differential clocks DACCLK_P and DACCLK_N.
5	0x23	0x0F	
6	0x24	0x30	When configuring the micro-delay unit controller, the target slope and target phase values of the micro-delay unit should be set according to Table 3 at different master clock frequencies.
7	0x25	0x80	
8	0x27	0x4C	
9	0x28	0x6C	
1 0	0x29	0xCB	
1 1	0x26	0x02	
1 2	0x26	0x03	Enables the search and track mode of the microdelay unit controller.
1 3	N/A	N/A	Waiting for 160k master clock cycles.
1 4	0x2A		Read back register 0x2A and confirm its value is 0x01 to ensure the DLL loop is locked. If it is not locked, return to step 10 and repeat the operation. After three attempts without locking, break the loop and report a microdelay unit failure.
1 5	0x15	0x42	Configure multi-chip synchronization
1 6	0x10	0x00	Before enabling the multi-chip synchronous controller, first disable the multi-chip controller.
1 7	0x10	0x60 or 0x40	Enable multi-chip controllers to establish loops and interrupt responses 0x60 = Main chip mode 0x40 = From chip mode
1 8	0x10	0x70 or 0x50	Enable multi-chip controller 0x70 = Main chip mode

			0x50 = From chip mode
1 9	N/A	N/A	Locking the DLL requires waiting for 160k master clock cycles.
20	0x21		Read back register 0x21 to confirm appropriate operation 0x90 = Main chip mode 0x00 = From chip mode If not, return to step 15 and repeat the operation. If this is still incorrect after 3 attempts, disconnect the loop and report a multi-chip synchronization lock failure.
twenty one	0x0D		Read back the 0x0D register and confirm that [5:4}=10. If not, return to step 2 and repeat the operation. If this is still incorrect after 3 attempts, break the loop and report a multi-chip synchronization lock failure.
twenty two	N/A	N/A	Ensure that the data input of the DAD9739 is fed by the DCI clock.
twenty three	0x13	0x72	Set the window width to 2.
twenty four	0x10	0x00	Before enabling the data receiving controller, disable the data receiving controller.
2 5	0x10	0x02	Enable the data receive controller to establish a loop and respond to interrupts.
2 6	0x10	0x03	Enable the data receiving controller to enter search and track mode.
2 7			Waiting for 135k master clock cycles.
2 8	0x21		Read back register 0x21 to ensure it equals 0x09 to confirm the DLL loop is locked and in a traced state. If not, toggle bits [7:6] of register 0x14 and return to step 17, repeating the operation. After three attempts without locking, disconnect the loop and report a data receive lock failure.
2 9	N/A	N/A	Read back the DCI_DEL values in registers 0x1B and 0x1C of the master and slave chips. If the difference between the read back values of the master and slave chips exceeds 40 code values, the target value of DCI_DEL needs to be re-specified as the average of the master chip and the read back DCI_DEL values.
3 0	0x06, 0x07	0x00,0x02	Optional: Modify the DAC's full-amplitude output current (default is 20mA).
3 1	0x08	0x00	Optional: Modify the DAC's operating mode (default is normal mode).

12 . Precautions

- **Product installation precautions:**

1) Please pay attention to the orientation of the components when soldering to avoid soldering them incorrectly.
2) All instruments and meters used for circuit debugging must have a good, unified ground. The PCB design must ensure proper grounding and power decoupling.
3) Care should be taken not to reverse the power supply or short-circuit the input/output terminals with the power supply, as this can easily damage the circuit.

- **Product usage precautions:**

1) Use 0.1μF/10μF capacitors as close as possible to the power supply for power decoupling.
2) To ensure device performance, do not exceed the device's maximum operating frequency during use.
3) Analog ground and digital ground should be kept isolated to prevent digital signals from flowing through analog ground and causing analog noise. Internally, analog ground and digital ground are not connected; they must be connected externally for the device to function. This connection point is a single point and should be as close to the device as possible.
4) It is recommended to reset the circuit after powering on before using it.

- **Product protection precautions:**

1) Provided that direct exposure to rain and snow is avoided, product packaging can be transported using safe means of transport. However, it must not be stored together with acidic, alkaline, or other corrosive substances. The packaging should be secure and existing means of transport should be used.
2) The storage environment for packaged products should meet the requirements of Class I warehouse conditions specified in Q/W657A Section 8.1 (temperature: 15℃~25℃, humidity: 25%~65%), with no acid, alkali or other corrosive gases in the vicinity, good ventilation, and appropriate anti-static measures.
3) It is recommended to use within 4 hours after opening. If exposed to air for more than 4 hours, it is recommended to bake at 125℃ for 8 hours, then vacuum pack and place in a desiccant cabinet.

13. Electrical Installation Requirements

1) This product has a moisture sensitivity rating of MSL3. The permissible time for the product to be exposed to the external environment after being removed from the moisture-proof bag, stored in a dry place or dried, and before reflow soldering is : ≤30℃/60RH% , 168h.
2) If the storage conditions of the components cannot be controlled or traced, please strictly follow the baking process of 125℃ for 8 hours before electrical assembly;
3) If the ambient temperature and humidity of the electrical installation environment cannot be guaranteed to be ≤30℃/60RH%, please complete the soldering within 12 hours after baking.
4) After the product is baked, it is very easy to generate static electricity, and ESD protection should be taken into account in all operations.
5) When using leaded reflow soldering (Sn63Pb37) for board-level assembly, the recommended peak temperature range is 210℃~220℃, the maximum peak temperature is not recommended to exceed 235℃, the dwell time within ±5℃ of the peak temperature is ≤20s, the dwell time above the liquidus line is 60~90s, the heating rate is 2~4℃/s, and the cooling rate is 2~6℃/s.
6) When using lead-free reflow soldering (SAC305) for board-level assembly, the recommended peak temperature range is 230℃~245℃, and the maximum peak temperature is not recommended to exceed 260℃. The dwell time within ±5℃ of the peak temperature is ≤20s, the dwell time above the liquidus line is 60~90s, the heating rate is 2~4℃/s, and the cooling rate is ≤2℃~6℃.
7) If the hybrid assembly process requires increased temperature, the device body temperature should be ensured not to exceed 260°C. (The device body temperature measurement point is located on the upper surface of the device during reflow soldering).
8) This product uses lead-free/lead solder balls made of SAC305.

14. Common Faults and Troubleshooting

1) No signal output: Check if the voltage at I_{120} terminal is normal to ensure the reference is working properly; check if the OUT DATACLK terminal is normal to ensure the clock can be received correctly.
2) Device malfunction: Identify the device's operating mode. It is recommended to reset the circuit after power-on to allow the internal registers to enter their default state.
3) Device malfunction: Check the power supply and ensure the power supply voltage is stable.

15. Packaging and Ordering Information

External dimensions

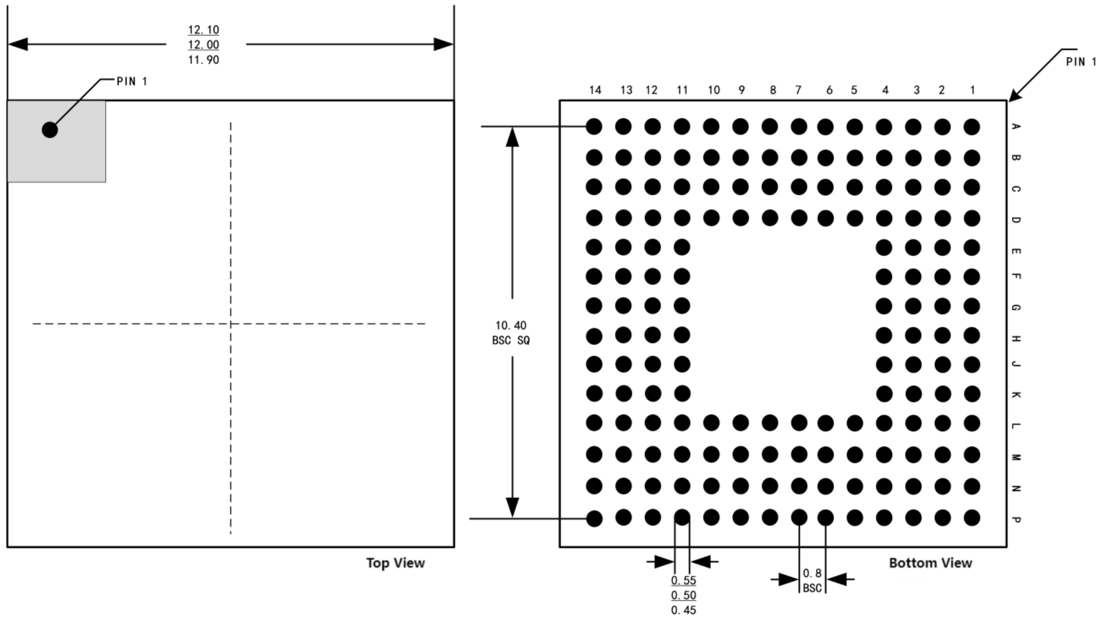

Figure 5. 160 -pin BGA package

The unit of measurement for the dimensions shown in the diagram is mm.

14. Ordering Guide

Model	Temperature range	Package Description	Package
DAD9739	-40 °C to +85°C	160BGA	184/TRAY

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