DAD9361/63/64-C RF Agile Transceiver

1. Features

- RF with integrated 12-bit DAC and ADC 2×2 transceiver frequency band: 70 MHz to 6.0 GHz
- Supports TDD and FDD
- Tunable channel bandwidth: <200 kHz to 56 MHz
- Dual-channel receiver: 6 differential or 12 single-ended inputs
- Excellent receiver sensitivity with a noise figure of 2. dB(800 MHz, Local Oscillator (LO)
- RX gain control
- Real-time monitoring and control signals are used for manual gain-independent automatic gain control.
- Dual transmitters: 4-channel differential output high linearity broadband transmitter
- TX EVM: ≤ − 40 dB
- TX noise: ≤ −157 dBm/Hz background noise
- TX monitor: Dynamic range ≥ 66 dB, precision = 1 dB
- The integrated fractional-N frequency synthesizer has a maximum LO step size of 2.4. Hz
- Multi-device synchronization
- CMOS/LVDS digital interface

2. Applications

- Point-to-point communication system
- Femtocell / Picocell / Base station
- General Radio System

3. Overview

The DAD9361/63/64-C is a high-performance, highly integrated radio frequency (RF) agile transceiver for 3G and 4G base station applications. Its programmability and broadband capabilities make it ideal for a variety of transceiver applications. The device integrates the RF front-end with a flexible mixed-signal baseband section, incorporating a frequency synthesizer and providing a configurable digital interface to the processor, simplifying design implementation. The DAD9361/63/64-C operates from 70 MHz to 6.0 GHz, covering most licensed and unlicensed bands, and supports channel bandwidths from less than 200 kHz to 56 MHz. Two independent direct-conversion receivers offer unparalleled noise figure and linearity. Each receiver (RX) subsystem features independent automatic gain control (AGC), DC offset correction, quadrature correction, and digital filtering, eliminating the need to provide these functions in the digital baseband. The DAD9361/63/64-C also features a flexible manual gain mode and supports external control. Each channel features two high dynamic range ADCs that digitize the received I and Q signals before passing them through a configurable decimation filter and a 128-tap finite impulse response (FIR) filter, generating a 12-bit output signal at the corresponding sampling rate. The transmitter employs a direct conversion architecture, achieving high modulation accuracy and ultra-low noise. This transmitter design delivers a TX EVM of less than -40 dB, providing considerable system margin for the selection of external power amplifiers. An onboard transmit (TX) power monitor can be used as a power detector, enabling highly accurate TX power measurement. A fully integrated phase-locked loop (PLL) provides low-power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation required for frequency division duplex (FDD) systems is integrated into the design. All VCO and loop filter devices are also integrated. The DAD9361/63/64-C core can be directly powered by a 1.3 V regulator. The IC is controlled via a standard four-wire serial port and four real-time I/O control pins. Comprehensive power-saving modes minimize power consumption during normal use. The DAD9361/63/64-C is packaged in a 10 mm × 10 mm, 144-pin BGA package.

4. Device packaging information

Product Model	Package Type	Package size
DAD9361/63/64-C	BGA144	10mm × 10mm

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5. Functional Block Diagram

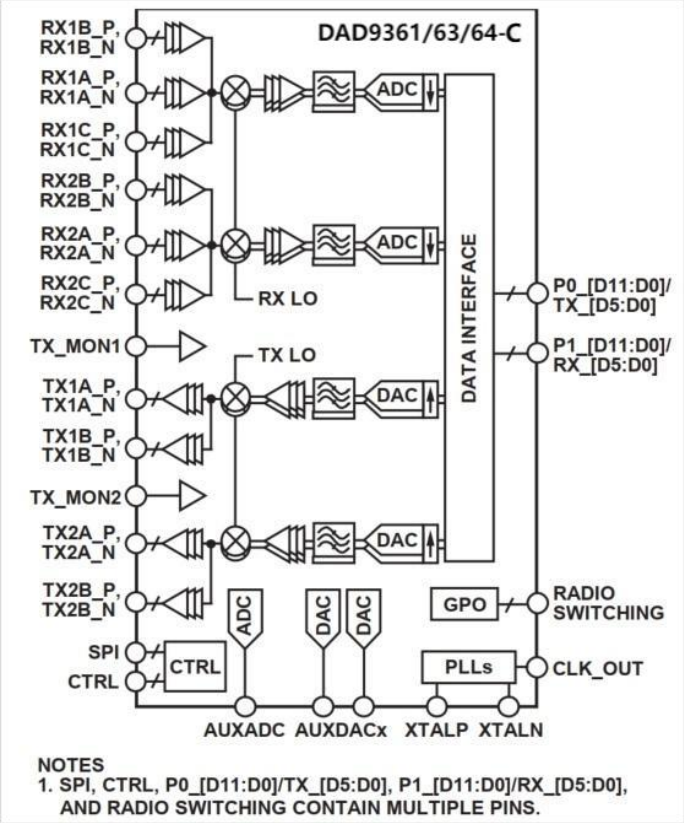

Figure 1. Functional Block Diagram

6. Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9	10	11	12
A	RX2A_N	RX2A_P	NC	VSSA	TX_MON2	VSSA	TX2A_N	TX2A_P	TX2B_N	TX2B_P	VDDA1P1_ TX_VCO	TX_EXT_ LO_IN
B	VSSA	VSSA	AUXDAC1	GPO_3	GPO_2	GPO_1	GPO_0	VDD_GPO	VDDA1P3_ TX_LO	VDDA1P3_ TX_VCO_ LDO	TX_VCO_ LDO_OUT	VSSA
C	RX2C_P	VSSA	AUXDAC2	TEST/ ENABLE	CTRL_IN0	CTRL_IN1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
D	RX2C_N	VDDA1P3_ RX_RF	VDDA1P3_ RX_TX	CTRL_OUT0	CTRL_IN3	CTRL_IN2	P0_D9/ TX_D4_P	P0_D7/ TX_D3_P	P0_D5/ TX_D2_P	P0_D3/ TX_D1_P	P0_D1/ TX_D0_P	VSSD
E	RX2B_P	VDDA1P3_ RX_LO	VDDA1P3_ TX_LO_ BUFFER	CTRL_OUT1	CTRL_OUT2	CTRL_OUT3	P0_D11/ TX_D5_P	P0_D8/ TX_D4_N	P0_D6/ TX_D3_N	P0_D4/ TX_D2_N	P0_D2/ TX_D1_N	P0_D0/ TX_D0_N
F	RX2B_N	VDDA1P3_ RX_VCO_ LDO	VSSA	CTRL_OUT6	CTRL_OUT5	CTRL_OUT4	VSSD	P0_D10/ TX_D5_N	VSSD	FB_CLK_P	VSSD	VDDD1P3_ DIG
G	RX_EXT_ LO_IN	RX_VCO_ LDO_OUT	VDDA1P1_ RX_VCO	CTRL_OUT7	EN_AGC	ENABLE	RX_ FRAME_N	RX_ FRAME_P	TX_ FRAME_P	FB_CLK_N	DATA_ CLK_P	VSSD
H	RX1B_P	VSSA	VSSA	TXNRX	SYNC_IN	VSSA	VSSD	P1_D11/ RX_D5_P	TX_ FRAME_N	VSSD	DATA_ CLK_N	VDD_ INTERFACE
J	RX1B_N	VSSA	VDDA1P3_ RX_SYNTH	SPI_DI	SPI_CLK	CLK_OUT	P1_D10/ RX_D5_N	P1_D9/ RX_D4_P	P1_D7/ RX_D3_P	P1_D5/ RX_D2_P	P1_D3/ RX_D1_P	P1_D1/ RX_D0_P
K	RX1C_P	VSSA	VDDA1P3_ TX_SYNTH	VDDA1P3_ BB	RESETB	SPI_ENB	P1_D8/ RX_D4_N	P1_D6/ RX_D3_N	P1_D4/ RX_D2_N	P1_D2/ RX_D1_N	P1_D0/ RX_D0_N	VSSD
L	RX1C_N	VSSA	VSSA	RBIAS	AUXADC	SPI_DO	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
M	RX1A_P	RX1A_N	NC	VSSA	TX_MON1	VSSA	TX1A_P	TX1A_N	TX1B_P	TX1B_N	XTALP	XTALN

☐ ANALOG I/O ☐ DC POWER
☐ DIGITAL I/O ☐ GROUND
☐ NO CONNECT

Figure 2. Pin configuration (top view)

Pin Functions

Pin No.	Type	Pin Name	Description
A1, A2	I	RX2A_N, RX2A_P	Receive channel 2 differential input A. Alternatively, each pin can be used as a single-ended input or a combination input.
			Form differential pairs. Ground any unused pins.
A3, M3	NC	NC	Do not connect. Do not connect to these pins.
A4, A6, B1, B2,	I	VSSA	Analog ground. Connect these pins directly to the VSSD digital ground (a ground plane) on the printed circuit board.
B12, C2, C7 to			
C12, F3, H2,			
H3, H6, J2, K2,			
L2, L3, L7 to			
L12, M4, M6			
A5	I	TX_MON2	Transmit Channel 2 power monitoring input. If this pin is not used, ground it.
A7, A8	O	TX2A_N, TX2A_P	Transmit channel 2 differential output A. Connect any unused pins to 1.3. V.
A9, A10	O	TX2B_N, TX2B_P	Transmit channel 2 differential output B. Connect any unused pins to 1.3. V.
A11	I	VDDA1P1_TX_VCO	Transmit VCO power input. Connect to B11 .
A12	I	TX_EXT_LO_IN	External emitter (LO) input. If this pin is not used, ground it.
B3	O	AUXDAC1	Auxiliary DAC 1. Output.
B4 to B7	O	GPO_3 to GPO_0	Supports version 3.3 The general output of V.
B8	I	VDD_GPO	2.5 V to 3.3 The VDD_GPO power supply supports AUXDAC and general-purpose output pins. When the VDD_GPO power supply is not used,
			The power supply must be set to 1.3. V.
B9	I	VDDA1P3_TX_LO	Launch LO 1.3 V power input.
B10	I	VDDA1P3_TX_VCO_LDO	Launch VCO LDO 1.3 V power input. Connect to B9.
B11	O	TX_VCO_LDO_OUT	Launch VCO LDO output. Connect to A11 to output a 1 µF bypass capacitor and a 1 The Ω resistor is connected in series and grounded.
C1, D1	I	RX2C_P, RX2C_N	Receive channel 2 differential input C. Each pin can be used as a single-ended input or combined to form a differential pair.
			These inputs are in 3 Performance will degrade above GHz . Ground unused pins.

Pin No.	Type	Pin Name	Description
C3	O	AUXDAC2	Auxiliary DAC 2. Output.
C4	I	Test/ Enable	Test input. This pin is grounded during normal operation.
C5, C6, D5, D6	I	CTRL_IN0 to CTRL_IN3	Control input. Used for manual RX gain and TX attenuation control.
D2	I	VDDA1P3_RX_RF	Receiver 1.3 V power input. Connect to D3 .
D3	I	VDDA1P3_RX_TX	1.3 V power input.
D4, E4 to E6	O	CTRL_OUT0, CTRL_OUT1 to	Control outputs. These pins are multi-function outputs with programmable capabilities.
F4 to F6, G4		CTRL_OUT3, CTRL_OUT6 to	
		CTRL_OUT4, CTRL_OUT7	
D7	I/O	P0_D9/TX_D4_P	Digital data port P0/ differential output transmission bus. This is a dual-function pin. For P0_D9, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D4_P) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
D8	I/O	P0_D7/TX_D3_P	Digital data port P0/ Differential output transmission bus. This is a dual-function pin. For P0_D7, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D3_P) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
D9	I/O	P0_D5/TX_D2_P	Digital data port P0/ Differential output transmission bus. This is a dual-function pin. For P0_D5, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D2_P) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
D10	I/O	P0_D3/TX_D1_P	Digital data port P0/ Differential output transmission bus. This is a dual-function pin. For P0_D3, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D1_P) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
D11	I/O	P0_D1/TX_D0_P	Digital data port P0/ differential output transmission bus. This is a dual-function pin. For P0_D1, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D0_P) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
D12, F7, F9,	I	VSSD	Digital ground. Connect these pins directly to the VSSA analog ground (a ground plane) on the printed circuit board.
F11, G12, H7,			
H10, K12			
E1, F1	I	RX2B_P, RX2B_N	Receiver channel 2 differential input B. Each pin can be used as a single-ended input or combined to form a differential pair. The performance of these inputs will deteriorate above 3 GHz. The unused pins should be grounded.
E2	I	VDDA1P3_RX_LO	Receive LO 1.3 V power input.
E3	I	VDDA1P3_TX_LO_BUFFER	1.3 V power input.
E7	I/O	P0_D11/TX_D5_P	Digital data port P0/ Differential output transmission bus. This is a dual-function pin. For P0_D11, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D5_P) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
E8	I/O	P0_D8/TX_D4_N	Digital data port P0/ Differential output transmission bus. This is a dual-function pin. For P0_D8, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D4_N) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
E9	I/O	P0_D6/TX_D3_N	Digital data port P0/ Differential output transmission bus. This is a dual-function pin. For P0_D6, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D3_N) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
E10	I/O	P0_D4/TX_D2_N	Digital data port P0/ differential output transmission bus. This is a dual-function pin. For P0_D4, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D2_N) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
E11	I/O	P0_D2/TX_D1_N	Digital data port P0/ Differential output transmission bus. This is a dual-function pin. For P0_D2, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D1_N) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
E12	I/O	P0_D0/TX_D0_N	Digital data port P0/ Differential output transmission bus. This is a dual-function pin. For P0_D0, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D0_N) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).

Pin No.	Type	Pin Name	Description
F2	I	VDDA1P3_RX_VCO_LDO	Receive VCO LDO 1.3 V power input. Connect to E2 .
F8	I/O	P0_D10/TX_D5_N	Digital data port P0/ differential output transmission bus. This is a dual-function pin. For P0_D10, it serves as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D5_N) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS terminals).
F10, G10	I	FB_CLK_P, FB_CLK_N	Feedback clock. These pins receive the FB_CLK signal which serves as the TX data clock. In CMOS mode, use FB_CLK_P as the input and ground FB_CLK_N.
F12	I	VDDD1P3_DIG	1.3 V digital power input.
G1	I	RX_EXT_LO_IN	External receive (LO) input. If this pin is not used, ground it.
G2	O	RX_VCO_LDO_OUT	Receive the output of the VCO LDO. Connect this pin directly to G3, and connect a 1 µF bypass capacitor in series with a 1 Ω resistor to ground.
G3	I	VDDA1P1_RX_VCO	Receives VCO power input. Connect this pin directly to G2 .
G5	I	EN_AGC	Manual control input for automatic gain control (AGC) .
G6	I	Enable	Control input. This pin allows the device to switch between various operating states.
G7, G8	O	RX_FRAME_N, RX_FRAME_P	Receive digital data frame output signal. These pins emit the RX_FRAME signal to indicate whether the RX output data is valid. In CMOS mode, the RX_FRAME_P is used as the output, while keeping RX_FRAME_N in an open state.
G9, H9	I	TX_FRAME_P, TX_FRAME_N	Transmit digital data frame input signal. These pins receive the TX_FRAME signal which indicates when the TX data is valid. In CMOS mode, use TX_FRAME_P as the input and ground TX_FRAME_N.
G11, H11	O	DATA_CLK_P, DATA_CLK_N	Receive data clock output. These pins emit the DATA_CLK signal, which is used by the BBP to provide the clock for the RX data. In CMOS mode, the DATA_CLK_P is used as the output, while keeping DATA_CLK_N in an open state.
H1, J1	I	RX1B_P, RX1B_N	The differential input B of the receiving channel 1 is connected. Additionally, each pin can also be used as a single-ended input. The performance of these inputs will deteriorate above 3 GHz. The unused pins should be grounded.
H4	I	TXNRX	Enables the state machine control signal. This pin controls the direction of the data port bus. A logic low level selects the RX direction, and a logic high level selects the TX direction.
H5	I	SYNC_IN	The input for synchronizing the digital clocks between multiple TRX9361 devices. If this pin is not used, it should be grounded.
H8	I/O	P1_D11/RX_D5_P	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D11, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D5_P) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
H12	I	VDD_INTERFACE	Digital I/O pins, 1.2 V to 2.5 V power supply (1.8V in LVDS mode) V to 2.5 V) .
J3	I	VDDA1P3_RX_SYNTH	1.3 V power input.
J4	I	SPI_DI	SPI serial data input.
J5	I	SPI_CLK	SPI clock input.
J6	O	CLK_OUT	Output clock. This pin can be configured as an output buffer for the external input clock DCXO, or as an output divider for the internal ADC_CLK.
J7	I/O	P1_D10/RX_D5_N	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D10, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D5_N) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
J8	I/O	P1_D9/RX_D4_P	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D9, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D4_P) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
J9	I/O	P1_D7/RX_D3_P	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D7, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D3_P) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
J10	I/O	P1_D5/RX_D2_P	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D5, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D2_P) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).

Pin No.	Type [1]	Pin Name	Description
J11	I/O	P1_D3/RX_D1_P	Digital data port P1/Receiving differential output bus. This is a dual-function pin. For P1_D3, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D1_P) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
J12	I/O	P1_D1/RX_D0_P	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D1, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D0_P) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
K1, L1	I	RX1C_P, RX1C_N	The differential input C of the receiving channel 1 is provided. Additionally, each pin can also be used as a single-ended input. The performance of these inputs will deteriorate above 3 GHz. The unused pins should be grounded.
K3	I	VDDA1P3_TX_SYNTH	1.3 V power input.
K4	I	VDDA1P3_BB	1.3 V power input.
K5	I	RESETB	Asynchronous reset. Logic low-level reset device.
K6	I	SPI_ENB	SPI enable input. Set this pin to logic low to enable the SPI bus.
K7	I/O	P1_D8/RX_D4_N	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D8, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D4_N) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
K8	I/O	P1_D6/RX_D3_N	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D6, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D3_N) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
K9	I/O	P1_D4/RX_D2_N	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D4, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D2_N) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
K10	I/O	P1_D2/RX_D1_N	Digital data port P1/ receives differential output bus. This is a dual-function pin. For P1_D2, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D1_N) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
K11	I/O	P1_D0/RX_D0_N	Digital data port P1/Receiving differential output bus. This is a dual-function pin. For P1_D0, it serves as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D0_N) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
L4	I	RBIAS	Bias input reference. Through a 14.3 kΩ A (1% tolerance) resistor grounds this pin.
L5	I	AUXADC	Auxiliary ADC input. If this pin is not used, ground it.
L6	O	SPI_DO	SPI serial data output in 4-wire mode, or high Z in 3-wire mode .
M1, M2	I	RX1A_P, RX1A_N	Receive channel 1 differential input A. Additionally, each pin can be used as a single-ended input. Ground the unused pins.
M5	I	TX_MON1	Transmit Channel 1 power monitoring input. Ground this pin when not in use.
M7, M8	O	TX1A_P, TX1A_N	Transmit channel 1 differential output A. Connect any unused pins to 1.3. V.
M9, M10	O	TX1B_P, TX1B_N	Transmit channel 1 differential output B. Connect any unused pins to 1.3. V.
M11, M12	I	XTALP, XTALN	Reference frequency crystal oscillator connection. When using the crystal oscillator, connect it between these two pins. When using an external clock source, connect it to XTALN and keep XTALP disconnected.

7. Specifications

Unless otherwise specified, electrical characteristics are defined at VDD_GPO = 3.3. V, VDD_INTERFACE = 1.8 V, all other VDDx pins = 1.3 V, T_A = Measured at 25°C .

Parameter [1]	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
Receiver , General						
Center frequency		70		6000	MHz	
Gain						
Minimum value			0		dB	
Maximum value			74.5		dB	800 MHz
			73.0		dB	2300 MHz (RX1A, RX2A)
			72.0		dB	2300 MHz (RX1B, RX1C, RX2B, RX2C
			65.5		dB	5500 MHz (RX1A, RX2A)
Gain Step			1		dB	
Received signal strength indicator	RSSI					
Gear			100		dB	
Accuracy			±2		dB	
Receiver, 800 MHz						
Noise figure	NF		2		dB	Maximum RX gain
Third-order input intermodulation	IIP3		-18		dBm	Maximum RX gain
Load point						
Second-order input	IIP2		40		dBm	Maximum RX gain
Interchange Load Point						
Local oscillator (LO) leakage			-122		dBm	RX front-end input
orthogonal						
Gain error			0.2		%	
Phase error			0.2		Spend	
Modulation precision (EVM)			-42		dB	19.2 MHz reference clock
Enter S_{11}			-10		dB	
RX1 to RX2 isolation						
RX1A to RX2A, RX1C to RX2C, RX1B to			70		dB	
RX2B			55		dB	
RX2 to RX1 isolation						
RX2A to RX1A, RX2C to RX1C, RX2B			70		dB	
to RX1B			55		dB	
Receiver, 2.4 GHz						
Noise figure	NF		3		dB	Maximum RX gain
Third-order input	IIP3		-14		dBm	Maximum RX gain
Intermodulation						
Load point	IIP2		45		dBm	Maximum RX gain
Second-order input						
Interchange Load Point			-110		dBm	Receiver front-end input
Local oscillator (LO) Leakage						
Orthogonal			0.2		%	
Gain error			0.2		Spend	
Phase error			-42		dB	40 MHz reference clock
Modulation precision			-10		dB	
(EVM)						

Enter S_{11}						
RX1 to RX2 isolation			65		dB	
RX1A to RX2A, RX1C to RX2C, RX1B to RX2B			50		dB	
RX2 to RX1 isolation			65		dB	
RX2A to RX1A, RX2C to RX1C, RX2B to RX1B			50		dB	
Logical output						
Output voltage						
High				1,375	mV	
Low		1025			mV	
Output differential voltage		150			mV	It can be programmed in 75 mV steps
Output offset voltage			1200		mV	
General output						
Output voltage						
High		VDD_GPO × 0.8			V	
Low				VDD_GPO × 0.2	V	
Output current			10		mA	
SPI Timing						VDD_INTERFACE=1.8V
SPI_CLK						
Cycle	t_{CP}	20			ns	
Pulse width	t_{MP}	9			ns	
SPI_ENB is set until the last falling edge of SPI_CLK after the first rising edge of SPI_CLK, and then remains in the set state until the next rising edge of SPI_CLK	t_{SC}	1			ns	
	t_{HC}	0			ns	
SPI_DI						
Digital input established to SPI_CLK	t_S	2			ns	
Data input is held until SPI_CLK	t_H	1			ns	
SPI_CLK rising edge to output						
Data delay						
4-line mode	t_{CO}	3		8	ns	
3-line mode	t_{CO}	3		8	ns	
Bus turnaround time, read	t_{HZM}	t_H		$tCO_{(max)}$	ns	After the last address bit of the BBP driver
Bus turnaround time, read	t_{HZS}	0		$tCO_{(max)}$	ns	DAD9361/63/64-C driver last data bits

8. Power Consumption — VDD_INTERFACE

Table 2 , VDD_INTERFACE = 1.2 V

Parameter	Min	Typ	Max	Unit	Test conditions / comments
Hibernation mode		45		µA	Power on, device disabled
1RX, 1TX, DDR					
LTE10					
Single port		2.9		mA	30.72 MHz data clock, CMOS
Dual-port		2.7		mA	15.36 MHz data clock, CMOS
LTE20					
Dual-port		5.2		mA	30.72 MHz data clock, CMOS
2RX, 2TX, DDR					
LTE3					
Dual-port		1.3		mA	7.68 MHz data clock, CMOS
LTE10					
Single port		4.6		mA	61.44 MHz data clock, CMOS
Dual-port		5.0		mA	30.72 MHz data clock, CMOS
LTE20					
Dual-port		8.2		mA	61.44 MHz data clock, CMOS
GSM					
Dual-port		0.2		mA	1.08 MHz data clock, CMOS
WiMAX 8.75					
Dual-port		3.3		mA	20 MHz data clock, CMOS
WiMAX 10					
Single port					
TDD RX		0.5		mA	22.4 MHz data clock, CMOS
TDD TX		3.6		mA	22.4 MHz data clock, CMOS
FDD		3.8		mA	44.8 MHz data clock, CMOS
WiMAX 20					
Dual-port					
FDD		6.7		mA	44.8 MHz data clock, CMOS

Table 3 , VDD_INTERFACE = 1.8 V

Parameter	Min	Typ	Max	Unit	Test conditions / comments
Hibernation mode		84		µA	Power on, device disabled
1RX, 1TX, DDR					
LTE10					
Single port		4.5		mA	30.72 MHz data clock, CMOS
Dual-port		4.1		mA	15.36 MHz data clock, CMOS
LTE20					
Dual-port		8.0		mA	15.36 MHz data clock, CMOS
2RX, 2TX, DDR					
LTE3					
Dual-port		2.0		mA	7.68 MHz data clock, CMOS
LTE10					
Single port		8.0		mA	61.44 MHz data clock, CMOS
Dual-port		7.5		mA	30.72 MHz data clock, CMOS
LTE20					
Dual-port		14.0		mA	61.44 MHz data clock, CMOS
GSM					
Dual-port		0.3		mA	1.08 MHz data clock, CMOS
WiMAX 8.75					
Dual-port		5.0		mA	20 MHz data clock, CMOS
WiMAX 10					
Single port					
TDD RX		0.7		mA	22.4 MHz data clock, CMOS
TDD TX		5.6		mA	22.4 MHz data clock, CMOS
FDD		6.0		mA	44.8 MHz data clock, CMOS
WiMAX 20					
Dual-port					
FDD		10.7		mA	44.8 MHz data clock, CMOS
P- P56					
75 mV differential output		14.0		mA	240 MHz data clock, LVDS
300 mV differential output		35.0		mA	240 MHz data clock, LVDS
450 mV differential output		47.0		mA	240 MHz data clock, LVDS

Table 4 , VDD_INTERFACE = 2.5 V

Parameter	Min	Typ	Max	Unit	Test conditions / comments
Gibernation mode		150		µA	Power on, device disabled
1RX, 1TX, DDR					
LTE10					
Single port		6.5		mA	30.72 MHz data clock, CMOS
Dual-port		6.0		mA	15.36 MHz data clock, CMOS
LTE20					
Dual-port		11.5		mA	30.72 MHz data clock, CMOS
2RX, 2TX, DDR					
LTE3					
Dual-port		3.0		mA	7.68 MHz data clock, CMOS
LTE10					
Single port		11.5		mA	61.44 MHz data clock, CMOS
Dual-port		10.0		mA	30.72 MHz data clock, CMOS
LTE20					
Dual-port		20.0		mA	61.44 MHz data clock, CMOS
GSM					
Dual-port		0.5		mA	1.08 MHz data clock, CMOS
WiMAX 8.75					
Dual-port		7.3		mA	20 MHz data clock, CMOS
WiMAX 10					
Single port					
TDD RX		1.3		mA	22.4 MHz data clock, CMOS
TDD TX		8.0		mA	22.4 MHz data clock, CMOS
FDD		8.7		mA	44.8 MHz data clock, CMOS
WiMAX 20					
Dual-port					
FDD		15.3		mA	44.8 MHz data clock, CMOS
P- P56					
75 mV differential output		26.0		mA	240 MHz data clock, LVDS
300 mV differential output		45.0		mA	240 MHz data clock, LVDS
450 mV differential output		58.0		mA	240 MHz data clock, LVDS

9. Power Consumption – VDDD1P3_DIG and VDDAx (all 1.3V power supply combinations)

Table 5. 800 MHz, TDD mode

Parameter	Min	Typ	Max	Unit	Test conditions / comments
1RX					
5 MHz bandwidth		180		mA	Continuous TX
10 MHz bandwidth		210		mA	Continuous TX
20 MHz bandwidth		260		mA	Continuous TX
2RX					
5 MHz bandwidth		265		mA	Continuous TX
10 MHz bandwidth		315		mA	Continuous TX
20 MHz bandwidth		405		mA	Continuous TX
1TX					
5 MHz bandwidth					
7 dBm		340		mA	Continuous TX
-27 dBm		190		mA	Continuous TX
10 MHz bandwidth					
7 dBm		360		mA	Continuous TX
-27 dBm		220		mA	Continuous TX
20 MHz bandwidth					
7 dBm		400		mA	Continuous TX
-27 dBm		250		mA	Continuous TX
2TX					
5 MHz bandwidth					
7 dBm		550		mA	Continuous TX
-27 dBm		260		mA	Continuous TX
10 MHz bandwidth					
7 dBm		600		mA	Continuous TX
-27 dBm		310		mA	Continuous TX
20 MHz bandwidth					
7 dBm		660		mA	Continuous TX
-27 dBm		370		mA	Continuous TX

Table 6. TDD mode, 2.4 GHz

Parameter	Min	Typ	Max	Unit	Test conditions / comments
1RX					
5 MHz bandwidth		175		mA	Continuous RX
10 MHz bandwidth		200		mA	Continuous RX
20 MHz bandwidth		240		mA	Continuous RX
2RX					
5 MHz bandwidth		260		mA	Continuous RX
10 MHz bandwidth		305		mA	Continuous RX
20 MHz bandwidth		390		mA	Continuous RX
1TX					
5 MHz bandwidth					
7 dBm		350		mA	Continuous TX
-27 dBm		160		mA	Continuous TX
10 MHz bandwidth					
7 dBm		380		mA	Continuous TX
-27 dBm		220		mA	Continuous TX
20 MHz bandwidth					
7 dBm		410		mA	Continuous TX
-27 dBm		260		mA	Continuous TX
2TX					
5 MHz bandwidth					
7 dBm		580		mA	Continuous TX
-27 dBm		280		mA	Continuous TX
10 MHz bandwidth					
7 dBm		635		mA	Continuous TX
-27 dBm		330		mA	Continuous TX
20 MHz bandwidth					
7 dBm		690		mA	Continuous TX
-27 dBm		390		mA	Continuous TX

Table 7. TDD mode, 5.5 GHz

Parameter	Min	Typ	Max	Unit	Test conditions / comments
1RX					
5 MHz bandwidth		175		mA	Continuous RX
40 MHz bandwidth		275		mA	Continuous RX
2RX					
5 MHz bandwidth		270		mA	Continuous RX
40 MHz bandwidth		445		mA	Continuous RX
1TX					
5 MHz bandwidth					
7 dBm		400		mA	Continuous TX
-27 dBm		240		mA	Continuous TX
40 MHz bandwidth					
7 dBm		490		mA	Continuous TX
-27 dBm		385		mA	Continuous TX
2TX					
5 MHz bandwidth					
7 dBm		650		mA	Continuous TX
-27 dBm		335		mA	Continuous TX
40 MHz bandwidth					
7 dBm		820		mA	Continuous TX
-27 dBm		500		mA	Continuous TX

Table 8. FDD mode, 800 MHz

Parameter	Min	Typ	Max	Unit	Test conditions / comments
1RX, 1TX					
5 MHz bandwidth					
7 dBm		490		mA	
-27 dBm		345		mA	
10 MHz bandwidth					
7 dBm		540		mA	
-27 dBm		395		mA	
20 MHz bandwidth					
7 dBm		615		mA	
-27 dBm		470		mA	
2RX, 1TX					
5 MHz bandwidth					
7 dBm		555		mA	
-27 dBm		410		mA	
10 MHz bandwidth					
7 dBm		625		mA	
-27 dBm		480		mA	
20 MHz bandwidth					
7 dBm		740		mA	
-27 dBm		600		mA	
1RX, 2TX					
5 MHz bandwidth					
7 dBm		685		mA	
-27 dBm		395		mA	
10 MHz bandwidth					
7 dBm		755		mA	
-27 dBm		465		mA	
20 MHz bandwidth					
7 dBm		850		mA	
-27 dBm		570		mA	
2RX, 2TX					
5 MHz bandwidth					
7 dBm		790		mA	
-27 dBm		495		mA	
10 MHz bandwidth					
7 dBm		885		mA	
-27 dBm		590		mA	
20 MHz bandwidth					
7 dBm		1020		mA	
-27 dBm		730		mA	

Table 9. FDD mode, 2.4 GHz

Parameter	Min	Typ	Max	Unit	Test conditions / comments
1RX, 1TX					
5 MHz bandwidth					
7 dBm		500		mA	
-27 dBm		350		mA	
10 MHz bandwidth					
7 dBm		540		mA	
-27 dBm		390		mA	
20 MHz bandwidth					
7 dBm		620		mA	
-27 dBm		475		mA	
2RX, 1TX					
5 MHz bandwidth					
7 dBm		590		mA	
-27 dBm		435		mA	
10 MHz bandwidth					
7 dBm		660			
-27 dBm		510		mA	
20 MHz bandwidth					
7 dBm		770		mA	
-27 dBm		620		mA	
1RX, 2TX				mA	
5 MHz bandwidth					
7 dBm		730		mA	
-27 dBm		425		mA	
10 MHz bandwidth					
7 dBm		800		mA	
-27dBm		500		mA	
20 MHz bandwidth					
7 dBm		900		mA	
-27 dBm		600		mA	
2RX, 2TX				mA	
5 MHz bandwidth					
7 dBm		820			
-27 dBm		515		mA	
10 MHz bandwidth					
7 dBm		900		mA	
-27 dBm		595		mA	
20 MHz bandwidth					
7 dBm		1050		mA	
-27 dBm		740		mA	

Table 10. FDD mode, 5.5 GHz

Parameter	Min	Typ	Max	Unit	Test conditions / comments
1RX, 1TX, 5 MHz bandwidth					
7 dBm		550		mA	
-27 dBm		385		mA	
2RX, 1TX, 5 MHz bandwidth					
7 dBm		645		mA	
-27 dBm		480		mA	
1RX, 2TX, 5 MHz bandwidth					
7 dBm		805		mA	
-27 dBm		480		mA	
2RX, 2TX, 5 MHz bandwidth					
7 dBm		895		mA	
-27 dBm		575		mA	

10. Absolute Maximum Ratings

Table 1.1

Parameter	Range
VDDx to VSSx	-0.3 V to +1.4 V
VDD_INTERFACE to VSSx	-0.3 V to +3.0 V
VDD_GPO to VSSx	-0.3 V to +3.9 V
Logic inputs and outputs to VSSx	-0.3 V to VDD_INTERFACE + 0.3 V
Input current to any pin other than the power supply pin	±10 mA
RF input (peak power)	2.5 dBm
TX monitor input power (Peak power)	9 dBm
Package power consumption	$(T_{JMAX} - T_A)/\theta_{JA}$
Maximum junction temperature (T_{JMAX})	110°C
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

11. Working Principle

- **General characteristics**

The DAD9361/63/64-C is a highly integrated radio frequency (RF) transceiver configurable for a wide range of applications, integrating all the necessary RF , mixed-signal, and digital modules that provide all transceiver functionality into a single device. Its programmability allows this wideband transceiver to be compatible with various communication standards, including Frequency Division Duplex (FDD) and Time Division Duplex (TDD) systems. Furthermore, this programmability allows for connection to various baseband processors (BBPs) via a single-channel 12-bit parallel data port, a dual-channel 12-bit parallel data port, or a 12-bit Low Voltage Differential Signaling (LVDS) interface. The DAD9361/63/64-C also features a self-calibration and automatic gain control (AGC) system to maintain high performance under various temperature and input signal conditions. Additionally, the device includes several test modes, allowing system designers to insert test tones and create internal loopback modes for debugging designs during prototyping and optimizing radio configurations for specific applications.

- **Receiver**

The receiver section contains all the necessary modules for receiving RF signals and converting them into digital data usable by the BBP . It has two independently controlled channels that can receive signals from different sources, enabling the device to be used in multiple-input multiple-output (MIMO) systems while also sharing a common frequency synthesizer. Each channel has three inputs that can be multiplexed to the signal chain, allowing the DAD9361/63/64-C to be used in diversity systems with multiple antenna inputs. The receiver is a direct-conversion system containing a low-noise amplifier (LNA), followed by matched in-phase (I) and quadrature (Q) amplifiers, a mixer, and a band-shaping filter that down-converts the received signal to baseband for digitization. An external LNA can also be connected to the device, providing designers with significant flexibility to customize the receiver front-end for specific applications. Gain control is achieved based on a pre-programmed gain index mapping, which distributes gain among the modules for performance optimization at various levels. This can be achieved by enabling the internal AGC in fast or slow modes, or by manual gain control, allowing the BBP to adjust the gain as needed. In addition, each channel has independent RSSI measurement capabilities, DC offset tracking, and all necessary circuitry for self-calibration. The receiver includes a 12-bit, Σ-Δ ADC with an adjustable sampling rate, capable of generating a data stream from the received signal. The digitized signal can be further conditioned through a series of decimation filters and a fully programmable 128-tap FIR filter (with additional decimation settings). The sampling rate of each digital filter module can be adjusted by changing the decimation coefficients to produce the desired output data rate.

- **Transmitter**

The transmitter section contains two identical, independently controlled channels, providing all the necessary digital processing, mixing, and RF modules to implement a direct conversion system while sharing a common general-purpose frequency synthesizer. Digital data received from the BBP passes through a fully programmable 128-tap FIR filter without interpolation options. The FIR output is sent to a series of interpolation filters, providing additional filtering and data rate interpolation processing before the output reaches the DAC. Each 12-bit DAC has an adjustable sampling rate. Both I and Q channels are fed into the RF module for up-conversion. When converted to baseband analog signals, the I and Q signals are filtered to remove sampling artifacts before being fed into the up-conversion mixer. Here, the I and Q signals are recombined and modulated at the carrier frequency for transmission to the output stage. The combined signal also passes through analog filters, which provide additional band-shaping processing before the signal is transmitted to the output amplifier. Each transmit channel offers a wide range of fine-grained attenuation adjustment to help designers optimize the signal-to-noise ratio (SNR). Each transmit channel incorporates self-calibration circuitry to support automatic real-time adjustment. The transmitter module also provides a TX monitor module for each channel. This module monitors the transmitter output and sends it back to the BBP via an unused receiver channel for signal monitoring. The TX monitor module is only available in TDD mode when the receiver is idle.

- **Clock input option**

The reference clock used by the DAD9361/63/64-C during operation can be provided by two different clock sources. The first option is to use a dedicated crystal oscillator with a frequency between 19MHz and 50MHz , connected between the XTALP and XTALN pins. The second option is to connect an external oscillator or clock distribution device (such as the AD9548) to the XTALN pin (with the XTALP pin remaining off) . If an external oscillator is used, the frequency can vary between 10MHz and 80MHz. This reference clock is used to power the frequency synthesizer modules, which generate all data clocks, sampling clocks, and local oscillator signals internally.

By using the digitally programmable, digitally controlled crystal oscillator (DCXO) function to adjust the on-chip variable capacitor, crystal frequency errors can be eliminated. This capacitor can tune the crystal frequency variation in the system, resulting in a more accurate reference clock from which all other frequencies are generated. This function can also be used in conjunction with on-chip temperature sensing to provide oscillator frequency temperature compensation during normal operation.

- **Frequency synthesizer**

The RF PLL – DAD9361/63/64-C contains two identical frequency synthesizers for generating the necessary LO signals for the RF signal path : one for the receiver and one for the transmitter. The phase-locked loop (PLL) frequency synthesizer employs a fractional -N design, incorporating a fully integrated voltage-controlled oscillator (VCO) and loop filter. In TDD operation mode, the frequency synthesizer turns on and off as needed for RX and TX frames. In FDD mode, the TX PLL and RX PLL can be active simultaneously. These PLLs require no external components.

The BB PLL – DAD9361/63/64-C also includes a baseband PLL frequency synthesizer for generating all baseband-related clock signals. These include the ADC and DAC sampling clocks, the DATA_CLK signal (see the "Digital Data Interface" section), and all data frame signals. The PLL's programming frequency range is 700MHz to 1400MHz, depending on the system's data rate and sampling rate requirements.

- **Digital Data Interface**

The DAD9361/63/64-C data interface uses parallel data ports (P0 and P1) to transfer data between the device and the BBP . The data ports can be configured in single-ended CMOS or differential LVDS format. Both formats can be configured in various ways to meet system requirements for data sequencing and data port connectivity. Specifically, this includes single-port data bus, dual-port data bus, single data rate, dual data rate, and various data sequencing combinations to transmit data from different channels across the bus at the appropriate time. Bus transmission is controlled via a simple hardware handshake signaling. Both ports can operate in bidirectional (TDD) mode or full-duplex (FDD) mode, in which half the bits are used for transmitting data and half for receiving data. The interface can also be configured to use only one data port for applications that do not require high data rates and prefer to use fewer interface pins.

- **DATA_CLK signal**

RX data provides the DATA_CLK signal, which the BBP can use when receiving data. DATA_CLK can be set to provide single data rate (SDR) timing (where data is sampled on each rising clock edge) or dual data rate (DDR) timing (where data is captured on both rising and falling edges) . This timing is suitable for single-port or two-port operating modes.

- **FB_CLK signal**

For transmit data, the interface uses the FB_CLK signal as a timing reference. For burst control signals, FB_CLK allows the source to be synchronized with rising edge capture timing, while for transmit signal bursts, it allows synchronization with rising edge (SDR mode) or dual-edge capture (DDR mode) timing. The FB_CLK signal must have the same frequency and duty cycle as DATA_CLK.

- **RX_FRAME signal**

Whenever the receiver outputs valid data, the device generates an RX_FRAME output signal. This signal has two modes: level mode (RX_FRAME remains high during valid data transmission) and pulse mode (RX_FRAME pulses with a 50% duty cycle). Similarly, the BBP must provide a TX_FRAME signal, with a rising edge indicating the start of valid data transmission. Similar to RX_FRAME, the TX_FRAME signal may remain high throughout the burst, or it may pulse with a 50% duty cycle.

- **Enable state machine**

DAD9361/63/64-C transceiver includes an Enable State Machine (ENSM) that allows for real-time control of the device's current state. During normal operation, the device can be placed in several different states, including

- Standby—Power saving, frequency synthesizer is disabled.
- Hibernation/Standby mode—all clocks/BB PLLs are disabled.
- TX—TX signal chain is enabled
- RX—RX signal chain is enabled
- FDD—TX and RX signal chains are enabled
- Alarm—Frequency synthesizer is enabled

ENSM has two possible control methods: SPI control and pin control.

- **SPI control mode**

In SPI control mode, asynchronous control of the ENSM is achieved by writing to the SPI register to transition from the current state to the next. SPI control is considered asynchronous with DATA_CLK because SPI_CLK may be derived from a different reference clock and still function correctly. SPI control of the ENSM is recommended when real-time control of the frequency synthesizer is not required. SPI control can be used for real-time control as long as the BBIC can accurately execute SPI write operations.

- **Pin control mode**

In pin control mode, enabling the ENABLE and TXNRX pins allows for real-time control of the current state. The ENSM supports TDD or FDD operating modes, depending on the configuration of the corresponding SPI registers. If the BBIC has additional control outputs that can be controlled in real-time, allowing for device state control via a simple two-wire interface, the ENABLE and TXNRX pin control method is recommended. To transition the ENSM from its current state to the next state, the ENABLE pin can be enabled with a pulse (edge detected internally) or a level. When using a pulse, the minimum pulse width must be one FB_CLK cycle. In level mode, the ENABLE and TXNRX pins are also edge-detected by the DAD9361/63/64-C and must meet the same minimum pulse width requirement of one FB_CLK cycle. In FDD mode, the ENABLE and TXNRX pins must be remapped as real-time RX and TX data transmission control signals. In this mode, the ENABLE pin enables or disables the receive signal path, and the TXNRX pin enables or disables the transmit signal path. In this mode, the ENSM is removed from the system so that all data flow is controlled by these pins.

- **SPI interface**

The DAD9361/63/64-C communicates with the BBP via a Serial Peripheral Interface (SPI). This interface can be configured as a 4-wire interface with dedicated receive and transmit ports, or as a 3-wire interface with a bidirectional data communication port. This bus allows the BBP to set all device control parameters via a simple address-data serial bus protocol. Write commands follow a 24-bit format. The first 6 bits are used to set the bus direction and the number of bytes to be transferred. The next 10 bits are the write address. The last 8 bits are the data to be transferred to the specified register address (MSB to LSB). The DAD9361/63/64-C also supports an LSB-first format, allowing commands to be written in LSB to MSB format. In this mode, for multi-byte write commands, the register address will increment. Read commands follow a similar format, except that the first 16 bits are transmitted on the SPI_DI pin, and the last 8 bits are read from the DAD9361/63/64-C . In 4-wire mode, this is done on the SPI_DO pin, and in 3-wire mode, it is done on the SPI_DI pin.

- **Control pin**

Control Outputs (CTRL_OUT[7:0]) - The DAD9361/63/64-C provides eight synchronous real-time output signals for use as interrupts for the BBP. These outputs can be configured to output internal settings and measurements that the BBP can use to monitor the transceiver's performance under different conditions. The control output pointer register selects which information is output to these pins, while the control output enable register determines which signals the BBP will activate for monitoring. Signals for manual gain mode, calibration flags, state machine status, and ADC outputs are some of the outputs that can be monitored on these pins.

Control Inputs (CTRL_IN[3:0]) - The DAD9361/63/64-C provides four edge-detected control input pins. In manual gain mode, the BBP can use these pins to change the gain table index in real time. In transmit mode, the BBP can use two of these pins to change the transmit gain in real time.

GPO Pins (GPO_3 to GPO_0) - The DAD9361/63/64-C provides four general-purpose logic output pins supporting 3.3V: GPO_3, GPO_2, GPO_1, and GPO_0. These pins can be used to control other peripheral devices, such as voltage regulators and switches, via the DAD9361/63/64-C SPI bus, or they can act as slave devices to the internal DAD9361/63/64-C state machine.

- **Auxiliary converter**

AUXADC – DAD9361/63/64-C includes an auxiliary ADC for monitoring system functions such as temperature and power output. The converter is 12-bit wide with an input range of 0V to 1.25V. When enabled, the ADC is in free-running mode. An SPI read operation provides the last value latched at the ADC output. A multiplexer preceding the ADC allows the user to select between the AUXADC input pins and the built-in temperature sensor.

AUXDAC1 and AUXDAC2 – The DAD9361/63/64-C contains two identical auxiliary DACs that can provide power amplifier (PA) bias or other system functions. The auxiliary DACs are 10-bit wide, with an output voltage range of 0.5V to VDD_GPO − 0.3V, a current drive of 10mA, and can be directly controlled via an internal enable state machine.

Power Supply for DAD9361/63/64-C – DAD9361/63/64-C must be powered by the following three power supplies: analog power (VDDD1P3_DIG/VDDAx=1.3V), interface power (VDD_INTERFACE=1.8V), and GPO power (VDD_GPO=3.3V).

12. Precautions

- **Product Installation Precautions**

1) Please pay attention to the orientation of the components when soldering to avoid soldering them incorrectly.
2) All instruments and meters used for circuit debugging must have a good, unified ground. The PCB design must ensure proper grounding and power decoupling.
3) Care should be taken not to reverse the power supply or short-circuit the input/output terminals with the power supply, as this can easily damage the circuit.
4) Denso specifications :

   This product has a moisture sensitivity rating of MSL3. The permissible time for the product to be exposed to the external environment from the time it is removed from the moisture-proof bag and after drying or baking until reflow soldering is: ≤30℃/60RH%, 168h. If the storage conditions of the device cannot be controlled or traced, please strictly implement baking at 125℃ for 8h before electrical assembly. If the temperature and humidity of the electrical assembly environment cannot be guaranteed to be ≤30℃/60RH%, please complete the soldering within 12h after baking . After baking, the product is highly susceptible to static electricity, and ESD protection should be taken into account during all operations. When using leaded reflow soldering (Sn63Pb37) for board-level assembly, the recommended peak temperature range is 210℃~235℃, and the maximum peak temperature is not recommended to exceed 235℃. The dwell time within ±5℃ of the peak temperature should be ≤20s , the dwell time above the liquidus line should be 60~90s, the heating rate is 2~4℃/s, and the cooling rate is 2~6℃/s . When using lead-free reflow soldering (SAC305) for board-level assembly , the recommended peak temperature range is 230℃~245℃, and the maximum peak temperature should not exceed 260℃. The dwell time within ±5℃ of the peak temperature should be ≤20s, and the dwell time above the liquidus line should be 60~90s. The heating rate is 2~4℃/s, and the cooling rate is 2~6℃. If the hybrid assembly process requires a higher temperature, the device body temperature should be ensured not to exceed 260℃ (the device body temperature measurement point is located on the upper surface of the device during reflow soldering).

- **Product usage precautions**

1) Power-on requirements: It is recommended to power on both analog and digital power supplies simultaneously, or power on the analog power supply first.
2) The decoupling capacitor at the LDO output should be a capacitor with a low ESR.
3) In applications, it is recommended to ground the PCB over a large area. This can eliminate potential differences that may exist due to different grounding points, and also reduce the impact of capacitance generated by the PCB on the circuit.
4) Each power supply pin needs to be connected to a 1μF or 0.1μF capacitor nearby.
5) In the analog input section, if differential input is used, the traces in the differential input section must be of equal length.
6) Digital power supplies and analog power supplies need to be separated.

- **Product protection precautions:**

All leads of this circuit are designed with electrostatic discharge (ESD) protection. However, high-energy electrical pulses may still damage the circuit. Therefore, ESD protection should be taken into account during testing, handling, and storage.

Note: For more detailed information, please contact the chip designer for technical support.

13. Packaging and Ordering Information

External dimensions

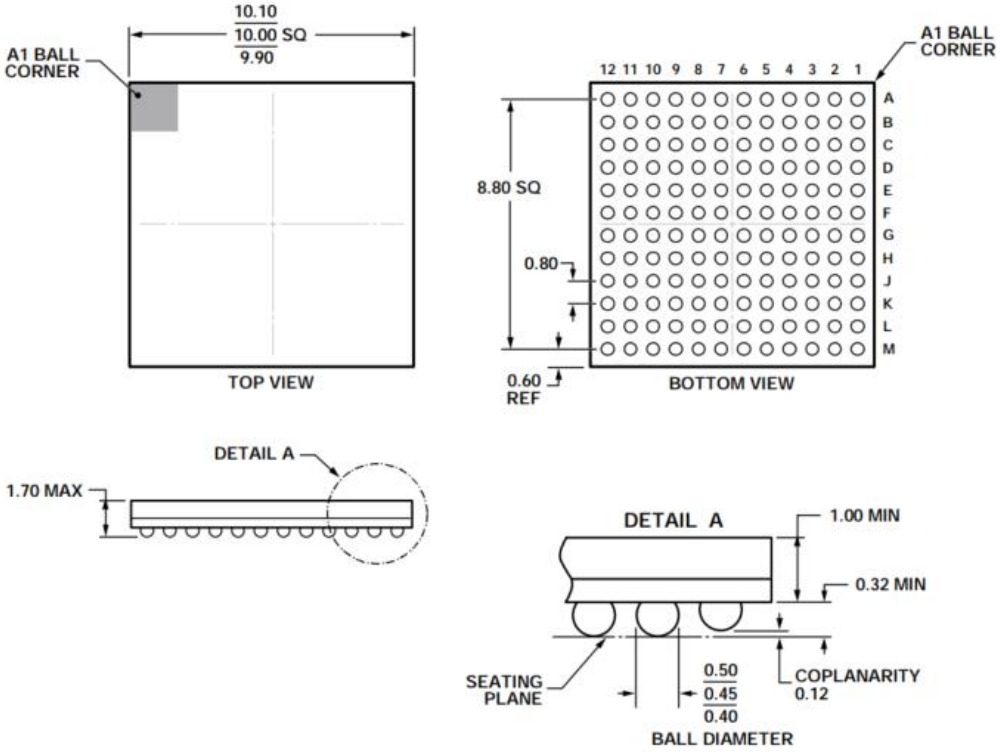

Figure 3 , 144-pin BGA package
The unit of measurement for the dimensions shown in the diagram is mm.

14. Ordering Guide

Model	Temperature range	Package Description	Package
DAD9361/63/64-C	-40 ℃ to + 85 ℃	144BGA	184/TRAY