DAD9122 Dual-Channel, 16-Bit, 1.2 GSPS DAC

Characteristics

- Flexible LVDS interface
- Single-carrier W-CDMA ACLR = 82 dBc (122.88 MHz intermediate frequency)
- Adjustable analog output: 8.7mA to 31.7mA, RL = 25 Ω to 50 Ω
- The integrated 2×/4×/8× interpolator/complex modulator enables the carrier to be placed at any position within the DAC bandwidth
- Gain, DC offset and phase adjustment support sideband suppression
- Multi-chip synchronous interface
- High-performance, low-noise phase-locked loop (PLL) clock multiplier
- Low power consumption: 1.5 W (1.2 GSPS), 800 mW (at 500 MSPS), under all operating conditions
- 72-pin, QFN package

Applications

- Wireless infrastructure: WCDMA, CDMA2000, TD-SCDMA, WiMAX
- Broadband communication: LMDS/MMDS, point-to-point
- Instrumentation: Radio frequency (RF) signal generators, arbitrary waveform generators

Overview

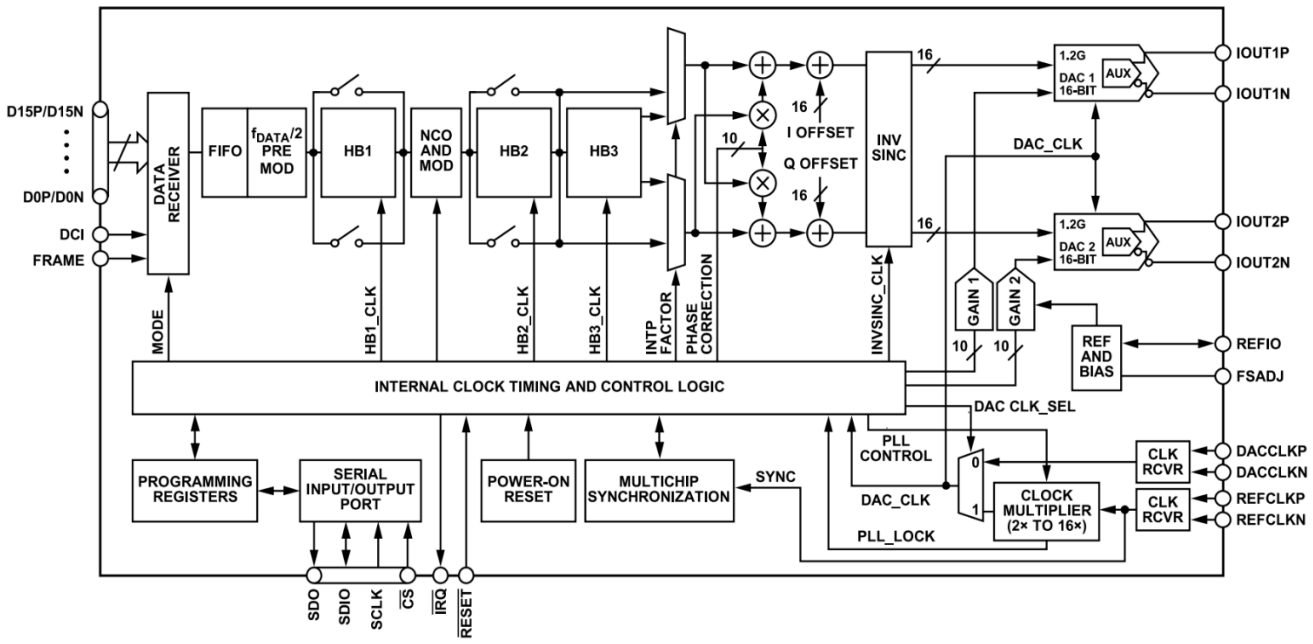
The DAD9122 is a dual-channel, 16-bit, high dynamic range digital-to-analog converter (DAC) offering a 1200 MSPS sampling rate and capable of generating multi-carrier signals up to the Nyquist frequency. It features characteristics optimized for direct conversion transmission applications, including complex digital modulation and gain and offset compensation. The DAC output is optimized for seamless interface with analog quadrature modulators. A four-wire serial port allows for programming and readback of many internal parameters. The full-scale output current is programmable from 8.7 mA to 31.7 mA. The device is packaged in a 72-pin LFCSP.

Product Features

1. Utilizing low noise and intermodulation distortion (IMD) characteristics enable high-quality synthesis of broadband signals.

2. Proprietary switch outputs can enhance dynamic performance.

3. Programmable current output and dual auxiliary DACs provide both flexibility and enhanced system functionality.



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DC Characteristics

Unless otherwise specified, Tmin to Tmax, AVDD33 = 3.3 V, CVDD18 = 1.8 V, DVDD18 = 1.8 V, IOVDD = 1.8 V, Ioutfs = 20mA, full power digital input, f_{DAC} = 1200Msps.

Table 1.

Parameter	Min	Typ	Max	Unit
Resolution		16		Bits
Accuracy				
Differential nonlinearity (DNL)		±2.1		LSB
Integral nonlinearity (INL)		±3.6		LSB
Main DAC output				
Offset error		±0.001		% FSR
Offset error temperature coefficient		±2.0		ppm/℃
Gain error		100		% FSR
Gain error temperature coefficient		±1.0		ppm/℃
Gain matching (DAC 1-ADC2)				% FSR
Full-scale output current	8.6		31.7	mA
Constant current source output voltage	-1.0		+1.0	V
Output impedance		10		MΩ
Reference output				
Output voltage		1.2		V
Output voltage temperature coefficient		10	1.3	ppm /℃
Power input voltage				
AVDD 33	3.13		3.47	V
CVDD 18 , DVDD 18	1.70		1.90	V
IOVDD	1.71	1.8	3.47	V
Digital power supply				
AVDD33		56	60	mA
CVDD18		12	16	mA
DVDD18		18	22	mA
IOVDD		32	36	mA
Power consumption				
2x Mode, f_{DAC} =491.22 MSPS, IF=10 MHz, PLL Off		850		mW
2x Mode, f_{DAC} =491.22 MSPS, IF=10 MHz, PLL On		920		mW
8x Mode,f_{DAC} =800 MSPS,IF=10 MHz,PLL Off	1125		1250	mW
AVDD33	55		59	mA
CVDD18	85		90	mA
DVDD18	440		500	mA
Power-down mode (Register 0x01=0xF0)			20	mA
Operating temperature	- 40		+85	℃

AC Specifications

Unless otherwise specified, Tmin to Tmax, AVDD33 = 3.3 V, CVDD18 = 1.8 V, DVDD18 = 1.8 V, IOVDD = 1.8 V, Ioutfs = 20mA, full power digital input, f_{DAC} = 1200Msps.

Table 2.

Parameter	Min	Typ	Max	Unit
Spurious-free dynamic range (SFDR)				
f_{DAC} = 100 MSPS, fout = 20 MHz		78		dBC
f_{DAC} = 200 MSPS, fout = 50 MHz		80		dBC
f_{DAC} = 400 MSPS, fout = 70 MHz		69		dBC
f_{DAC} = 800 MSPS, fout = 70 MHz		72		dBC
Intermodulation distortion (IMD)				
f_{DAC} = 200 MSPS, fout = 50 MHz		84		dBC
f_{DAC} = 400 MSPS, fout = 60 MHz		86		dBC
f_{DAC} = 400 MSPS, fout = 80 MHz		84		dBC
f_{DAC} = 800 MSPS, fout = 100 MHz		81		dBC
Adjacent channel leakage ratio				
f_{DAC} = 491.52 MSPS, fout =10 MHz		84		dBC
f_{DAC} = 491.52 MSPS, fout = 122.88 MHz		82		dBC
f_{DAC} = 983.04 MSPS, fout = 122.88 MHz		83		dBC
Noise spectral density				
f_{DAC} = 200 MSPS, fout = 80 MHz		-162		dBm /HZ
f_{DAC} = 400 MSPS, fout = 80 MHz		-163		dBm /HZ
f_{DAC} = 800 MSPS, fout = 80 MHz		-164		dBm /HZ

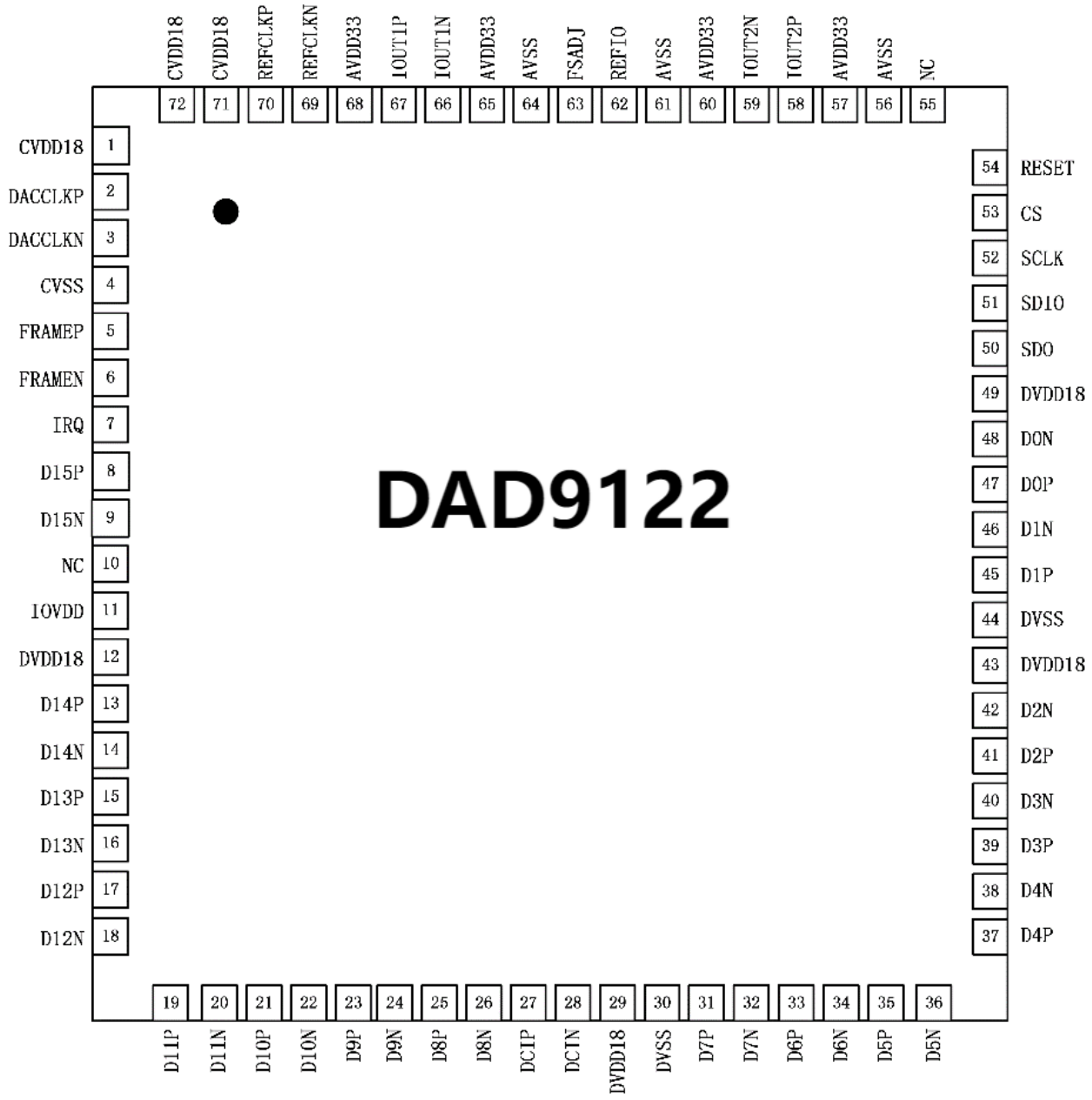
Digital and Clock Characteristics

Unless otherwise specified, Tmin to Tmax, AVDD33 = 3.3 V, CVDD18 = 1.8 V, DVDD18 = 1.8 V, IOVDD = 1.8 V, Ioutfs = 20mA , full power digital input, f_{DAC} = 1200Msps.

Table 3.

Parameter	Min	Typ	Max	Unit
CMOS input logic levels				
Input logic high level				
IOVDD=1.8V	1.2			V
IOVDD=2.5V	1.6			V
IOVDD=3.3V	2.0			V
Input logic low level				
IOVDD=1.8V			0.6	V
IOVDD = 2.5V, 3.3V			0.8	V
CMOS output logic level				
Output logic high level				
IOVDD=1.8V	1.4			V
IOVDD=2.5V	1.8			V
IOVDD=3.3V	2.4			V
Output logic low level				
IOVDD = 1.8V, 2.5V, 3.3V			0.4	V
LVDS receiver input				
Input voltage range, V_{IA} or V_{IB}	825		1675	mV
Input differential threshold, V_{IDTH}	-100		+100	mV
Input differential hysteresis, V_{IDTHH} to V_{IDTHL}		20		mV
Receiver differential input impedance, R_{IN}	80		120	Ω
DAC clock inputs (CLKP, CLKN)				
Differential voltage	100	500	2000	mV
Common mode voltage		1.25		V
Input frequency			1230	MHZ
Reference clock inputs (REFCLKP, REFCLKN)				
Differential voltage	100	500	2000	mV
Common mode voltage		1.25		V
Reference clock frequency (PLL mode)	15.625		600	MHz
Reference clock frequency (SYNC mode)	0		600	MHz
Data port input				
Output high voltage	2.0			V
Output low voltage			0.8	V
Input current			1	uA
CSB to SCLK setup time (tDBS dual - port mode)	400			ps
CSB to SCLK hold time (tDBH dual- port mode)	1200			ps
DAC clock to analog output data delay			7	Cycles
input for DAC clock hold time (tDBS single-mode port mode)	400			ps
input for DAC clock hold time (tDB H single-mode port mode)	1200			ps
DAC clock to analog output data delay (single-port mode)			8	Cycles
Serial port				
SCLK frequency (fSCLK)			40	MHZ
SCLK pulse width is high (tPWH)	12.5			ns
SCLK has a low pulse width (tPWL)	12.5			ns
SDIO to SCLK setting time (tDS)	1.9			ns
CSB to SCLK holding time (tDH)	0.2			ns
SCLK to SDIO /SDO data validity time (tDV)	2.3			ns
CSB to SCLK time setting (tDCSB)		1.4		ns

Pin Definitions and Function Descriptions



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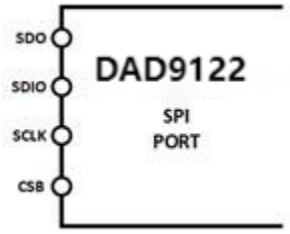
Pin No.	Symbol	Function Description
1, 71, 72	CVDD18	The clock circuit is powered by a 1.8V power supply
2, 3	DACCLKP, DACCLKN	DAC clock input positive and negative terminals
4	CVSS	Clock power common terminal
5, 6	FRAMEP, FRAMEN	If the frame input pins are not used, FRAMEP must be connected to DVSS and FRAMEN must be connected to DVDD18
7	IRQB	Interrupt request. Open-drain, active low output. Pull-up to IOVDD via a 10kΩ resistor
8, 9	D15P, D15N	Data bit 15 (MSB)
10, 55	NC	Suspended
11	IOVDD	Power supply pins for the serial pin, RESET, and IRQ. Voltages from 1.8V to 3.3V can be supplied to these pins.
12, 29, 43, 49	DVDD18	1.8V digital power supply
13, 14	D14P, D14N	Data bit 14
15, 16	D13P, D13N	Data bit 13
17, 18	D12P, D12N	Data bit 12
19, 20	D11P, D11N	Data bit 11
21, 22	D10P, D10N	Data bit 10
23, 24	D9P, D9N	Data bit 9
25, 26	D8P, D8N	Data bit 8
27, 28	DCIP, DCIN	Data clock input
30, 44	DVSS	Digital ground
31, 32	D7P, D7N	Data bit 7
33, 34	D6P, D6N	Data bit 6
35, 36	D5P, D5N	Data bit 5
37, 38	D4P, D4N	Data bit 4
39, 40	D3P, D3N	Data bit 3
41, 42	D2P, D2N	Data bit 2
45, 46	D1P, D1N	Data bit 1
47, 48	D0P, D0N	Data bit 0
50	SDO	Serial data output
51	SDIO	Serial data input/output
52	SCLK	Serial clock input
53	CSB	Serial chip select, active low
54	RESETB	Reset, active low
56, 61, 64	AVSS	Analog ground
57, 60, 65, 68	AVDD33	3.3V analog power supply
58, 59	IOUT2P , IOUT2N	Q DAC positive and negative current output
62	REFIO	Reference voltage. 1.2V output
63	FSADJ	Full-scale current output adjustment. Place a 10 kΩ resistor between this pin and AVSS
66, 67	IOUT1N, IOUT1P	I DAC negative and positive current output
69, 70	REFCLKN、REFCLKP	PLL reference clock input, negative and positive pins. This pin also has an auxiliary function, namely, synchronization input
	EPAD	The bottom pad must be connected to AVSS

SPI Serial Interface Operation



The Serial Port (SPI) is a flexible synchronous serial communication port that can easily interface with various industry-standard microcontrollers and microprocessors. Users can read and write to the DAD9122 via the SPI port and access all configuration registers. It supports single-byte and multi-byte data transmission, as well as high-order and low-order transmission modes. Serial data input/output can be achieved through a bidirectional SDIO pin or two unidirectional SDIO and SDO pins.

The working mode of the serial interface is controlled by register 0x00 [7]. The configuration takes effect immediately after the last bit of the register is written.

SPI communication cycle of the DAD9122 consists of two phases. The first phase is the instruction cycle (i.e., writing an instruction byte to the device), which is synchronized with the first eight rising edges of SCLK. The instruction byte provides the serial port controller with information about the data transmission cycle (i.e., the second phase of the communication cycle). The instruction byte in the first phase defines whether the upcoming data transmission is a read or write operation and specifies the starting register address of the first byte of the data transmission. The first eight rising edges of SCLK in each communication cycle are used to write the instruction byte to the device.

When the CS pin transitions from logic high to logic low, the serial port timing is reset to the initial state of the instruction cycle. In this state, the subsequent eight rising edges of SCLK represent the instruction bits for the current I/O operation.

The remaining SCLK edges are used for the second phase of the communication cycle. This phase is the actual data transfer process between the device and the system controller, involving the transfer of one or more data bytes. Except for the frequency tuning word and NCO phase offset, all other registers are updated immediately when the last bit of each transferred byte is written; while the frequency tuning word and NCO phase offset are only changed when the frequency tuning word (FTW) update bit (register 0x36, bit 0) is set.

Data Format

The instruction bytes for the SPI port are shown in the table below:

I7(LSB)	I6	I5	I4	I3	I2	I1	I0(LSB)
R/W	A6	A5	A4	A3	A2	A1	A0

R /W : Bit 7 determines whether a read or write operation is performed after the instruction byte write cycle ends. 1 indicates a read operation, and 0 indicates a write operation.

Bits [6:0]: Determine the registers accessed during the data transmission portion of the communication cycle. For multi-byte transmissions, A6 is the starting byte address. The remaining register addresses are generated by the device based on the setting of the LSB_FIRST bit (register 0x00, bit 6).

Serial Port (SPI) Pin Function Description

- **Serial clock (SCLK)**

The serial clock pin is used to synchronize data input to and output to the device and to run the internal state machine. SCLK supports a frequency of 40MHz. All data input occurs on the rising edge of SCLK, and output occurs on the falling edge of SCLK.

- **Film Selection (CSB)**

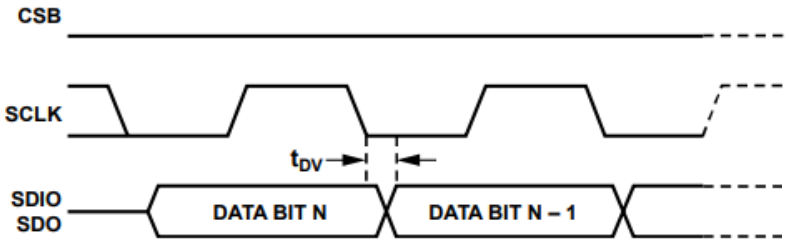
A low-level active input signal is used to initiate and control the communication cycle. It allows multiple devices to share the same set of serial communication lines. When the CS pin is high, the SDO and SDIO pins will enter a high-impedance state. During the communication cycle, the CS pin should remain low.

- **Serial Data Input/ Output (SDIO)**

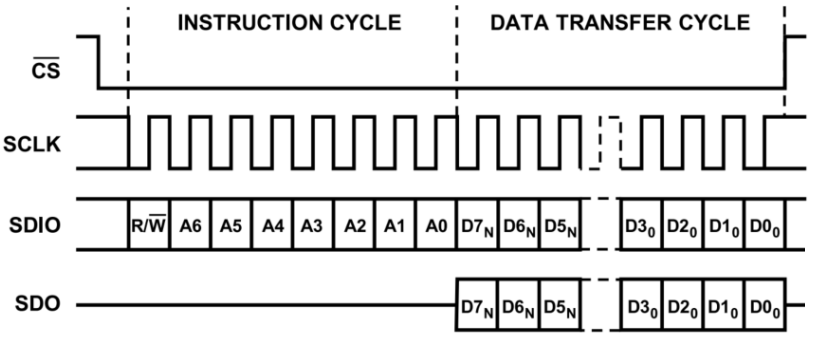
Data is always written to the device through this pin, but it can also be configured as a bidirectional data line. Its configuration is controlled by bit 7 of register 0x00. The default value is logic 0, in which case the SDIO pin is configured as a unidirectional input.

- **Serial Data Output (SDO)**

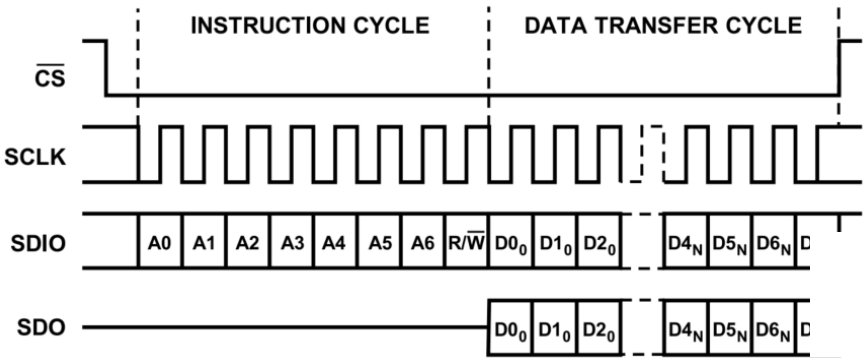
In protocols that use independent data transceiver lines, data is read through this pin. If the device is operating in single-wire bidirectional I/O mode, this pin does not output data and remains in a high-impedance state.



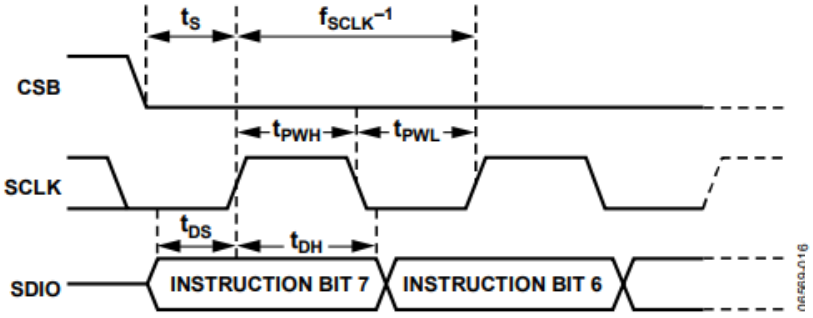
Timing Diagram for SPI Register Read



Serial Register Interface Timing (MSB Priority)



Serial Register Interface Timing (Least Significant Bit First)



Timing Diagram for SPI Register Write

Register List

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x00	Comm	SDIO	LSB_FIRST	Reset						0x00
0x01	Power control	Power down I DAC	Power down Q DAC	Power down data receiver	Power down aux ADC					0x10
0x03	Data format	Binary data format	Q data1	MSB swap				Data Bus Width[1:0]		0x00
0x04	Interrupt enable	Enable PLL lock lost	Enable PLL locked	Enable sync signal lost	Enable sync signal locked			Enable FIFO Warning 1	Enable FIFO Warning 2	0x00
0x05	Interrupt enable	0	0	0	Enable AED compare pass	Enable AED compare fail	Enable SED compare fail	0	0	0x00
0x06	Event flag	PLL lock lost	PLL locked	Sync signal lost	Sync signal locked			FIFO Warning 1	FIFO Warning 2	N/A
0x07	Event flag				AED compare pass	AED compare fail	SED compare fail			N/A
0x08	Clock receiver control	DACCLK duty correction	REFCLK duty correction	DACCLK cross-correction	REFCLK cross-correction	1	1	1	1	0x3F
0x0A	PLL control	PLL enable	PLL manual enable	Manual VCO Band [5:0]						0x40
0x0C	PLL control	PLL Loop Bandwidth[1:0]			PLL Charge Pump Current[4:0]					0xD1
0x0D	PLL control	N2[1:0]			PLL cross-control enable	N0[1:0]		N1[1:0]		0xD9
0x0E	PLL status	PLL locked				VCO Control Voltage [3:0]				N/A
0x0F	PLL status			VCO Band Readback [5:0]						N/A
0x10	Sync control	Sync enable	Data/FIFO rate toggle			Rising Edge Sync	Sync Averaging[2:0]			0x48
0x11	Sync control			Sync Phase Request[5:0]						0x00
0x12	Sync status	Sync lost	Sync locked							N/A
0x13	Sync status	Sync Phase Readback[7:0] (6.2 format)								N/A
0x15	Data receiver status			LVDS FRAME level high	LVDS FRAME level low	LVDS DCI level high	LVDS DCI level low	LVDS data level high	LVDS data level low	N/A
0x16	DCI delay							DCI Delay[1:0]		0x00

0x17	FIFO control						FIFO Phase Offset[2:0]			0x04
0x18	FIFO status	FIFO Warning 1	FIFO Warning 2				FIFO soft align ack	FIFO soft align request		N/A
0x19	FIFO status	FIFO Level [7:0]								N/A
0x1B	Datapath control	Bypass premod	Bypass sinc $^{-1}$	Bypass NCO		NCO gain	Bypass phase comp and dc offset	Select sideband	Send I data to Q data	0xE4
0x1C	HB1 control						HB1[1:0]		Bypass HB1	0x00
0x1D	HB2 control		HB2[5:0]						Bypass HB2	0x00
0x1E	HB3 control		HB3[5:0]						Bypass HB3	0x00
0x1F	Chip ID	Chip ID[7:0]								0x08
0x30	FTW LSB	FTW[7:0]								0x00
0x31	FTW	FTW[15:8]								0x00
0x32	FTW	FTW[23:16]								0x00
0x33	FTW MSB	FTW[31:24]								0x00
0x34	NCO phase offset LSB	NCO Phase Offset[7:0]								0x00
0x35	NCO phase offset MSB	NCO Phase Offset[7:0]								0x00
0x36	NCO FTW update			FRAME FTW ack	FRAME FTW request			Update FTW ack	Update FTW request	0x00
0x38	I phase adj LSB	Phase I Adj[7:0]								0x00
0x39	I phase adj MSB							Phase I Adj[9:8]		0x00
0x3A	Q phase adj LSB	Q Phase Adj[7:0]								0x00
0x3B	Q phase adj MSB							Q Phase Adj[9:8]		0x00
0x3C	I DAC offset LSB	I DAC Offset[7:0]								0x00
0x3D	I DAC offset MSB	I DAC Offset[15:8]								0x00
0x3E	Q DAC offset LSB	Q DAC Offset[7:0]								0x00
0x3F	Q DAC offset MSB	Q DAC Offset[15:8]								0x00
0x40	I DAC FS adjust	I DAC FS Adj[7:0]								0xF9
0x41	I DAC control	I DAC sleep						I DAC FS Adj[9:8]		0x01
0x42	I aux DAC data	I Aux DAC[7:0]								0x00

0x43	I aux DAC control	I aux DAC sign	I aux DAC current direction	I aux DAC sleet				I Aux DAC[9:8]	0x00
0x44	Q DAC FS adjust	Q DAC FS Adj[7:0]							0xF9
0x45	Q DAC control	Q DAC sleep						Q DAC FS Adj[9:8]	0x01
0x46	Q aux DAC data	Q Aux DAC[7:0]							0x00
0x47	Q aux DAC control	Q aux DAC sign	Q aux DAC current direction	Q aux DAC sleep				Q Aux DAC[9:8]	0x00
0x48	Die temp range control		FS Current[2:0]			Reference Current[2:0]		Capacitor value	0x02
0x49	Die temp LSB	Die Temp[7:0]							N/A
0x4A	Die temp MSB	Die Temp[15:8]							N/A
0x67	SED control	SED compare enable		Sample error detected		Autoclear enable		Compare fail	Compare pass	0x00
0x68	Compare I0 LSBs	Compare Value I0[7:0]							0xB6
0x69	Compare I0 MSBs	Compare Value I0[15:8]							0x7A
0x6A	Compare Q0 LSBs	Compare Value Q0[7:0]							0x45
0x6B	Compare Q0 MSBs	Compare Value Q0[15:8]							0xEA
0x6C	Compare I1 LSBs	Compare Value I1[7:0]							0x16
0x6D	Compare I1 MSBs	Compare Value I1[15:8]							0x1A
0x6E	Compare I1 LSBs	Compare Value Q1[7:0]							0xC6
0x6F	Compare Q1 MSBs	Compare Value Q1[15:8]							0xAA
0x70	SED I LSBs	Errors detected: I_BITS[7:0]							0x00
0x71	SED I MSBs	Error detected: I_BITS[15:8]							0x00
0x72	SED Q LSBs	Errors detected: Q_BITS[7:0]							0x00
0x73	SED Q MSBs	Error detected Q_BITS[15:8]							0x00
0x7F	Revision	0	0	Revision[3:0]				0	0	N/A

LVDS Input Data Port

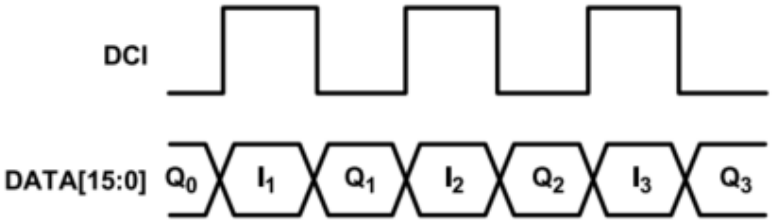
The DAD9122 has one LVDS data port for receiving data from the I and Q transmit channels. This device can receive data in word, byte, and nibble formats. In word, byte, and nibble modes, data is transmitted via 16-bit, 8-bit, and 4-bit LVDS data buses, respectively. The pin assignments for each mode are shown in the table below.

Mode	
Word mode	D15, D14, … , D0
Byte mode	D14, D12, D10, D8, D7, D5, D3, D1
Half-byte mode	D10, D8, D7, D5

The data includes a reference bit (DCI signal) used to generate a dual data rate (DDR) clock. In byte and nibble modes, the FRAME signal controls which digital-to-analog converter (DAC) the data is sent to. All interface signals are time-aligned, therefore a maximum skew requirement exists on the bus.

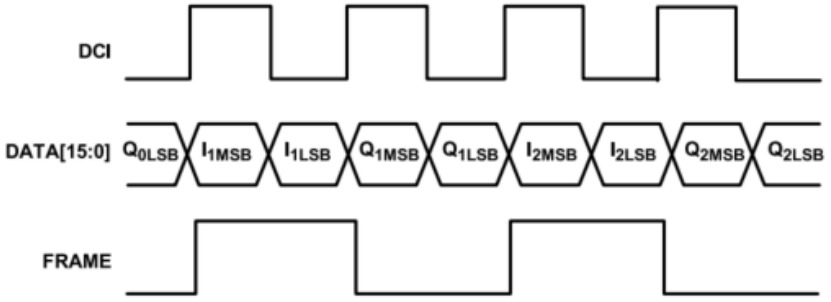
Word Interface Mode

In word mode, the DCI signal is a reference bit used to generate the data sampling clock. The DCI signal should be time-aligned with the data signal. The data from the I-DC converter should correspond to a high level of the DCI signal, and the data from the Q-DC converter should correspond to a low level of the DCI signal, as shown in the figure below .



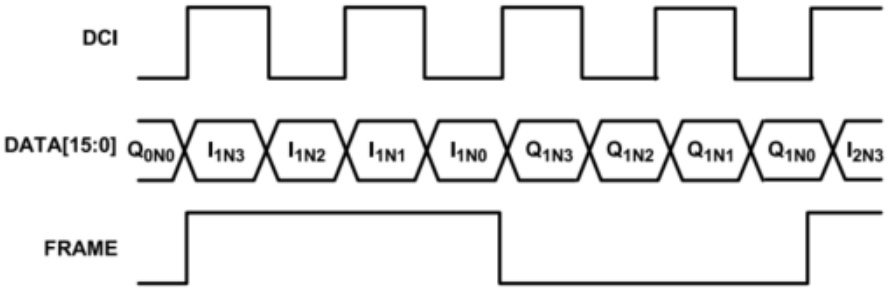
Byte Interface Mode

In the byte mode, the DCI signal serves as a reference bit to generate the data sampling clock. The DCI signal should be time-aligned with the data signal. The most significant byte of the data should correspond to the high level of the DCI signal, and the least significant byte should correspond to the low level of the DCI signal. The FRAME signal indicates which digital-to-analog converter the data is sent to. When FRAME is at a high level, the data is sent to the I digital-to-analog converter; when FRAME is at a low level, the data is sent to the Q digital-to-analog converter. The complete timing diagram is shown in the following figure.



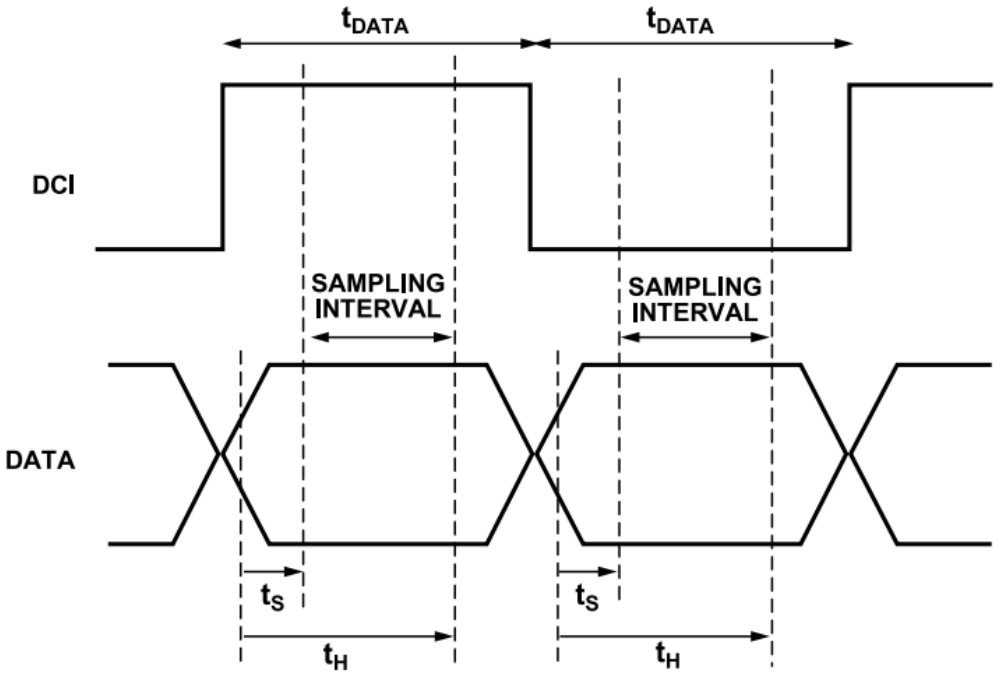
Half-Byte Interface Mode

In the half-byte mode, the DCI signal serves as a reference bit to generate the data sampling clock. The DCI signal should be time-aligned with the data signal. The FRAME signal indicates which digital-to-analog converter the data is sent to. When FRAME is at a high level, the data is sent to the I digital-to-analog converter; when FRAME is at a low level, the data is sent to the Q digital-to-analog converter. All four half-bytes must be written to the device to ensure normal operation. For a 12-bit resolution device, the data of the fourth half-byte serves as a placeholder for the data frame structure. The complete timing diagram is shown in the following figure.



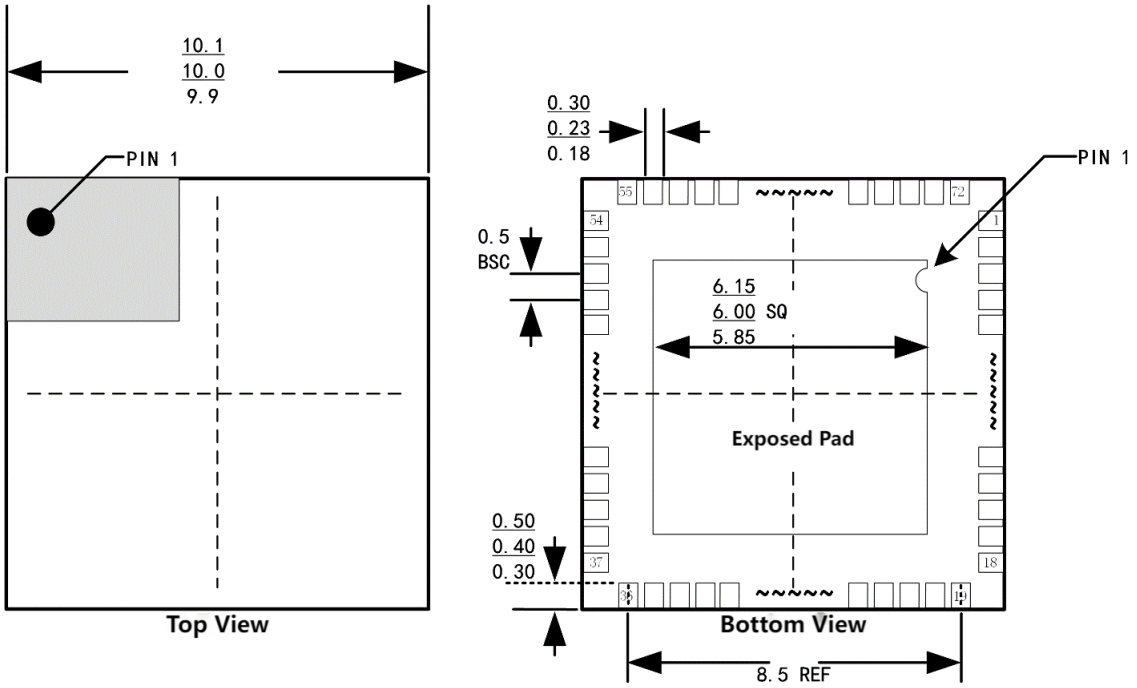
Interface Timing

The timing diagram for the digital interface port is shown in Figure 46. The data bus sampling point nominally occurs 350 ps after each DCI signal edge, with an uncertainty of ±300 ps, as shown in the sampling interval in Figure 46. The data and FRAME signals must be valid throughout the entire sampling interval. The data and FRAME signals can change at any time between sampling intervals. The setup time (t_S) and hold time (t_H) for the edges are shown in Figure 46. The minimum setup and hold times are shown in the table below.



DCI Delay Register 0x16, bits [1:0]	Minimum setup time t_S (ns)	Minimum hold time t_H (ns)	Sampling interval (ns)
00	-0.05	0.65	0.6
01	-0.23	0.95	0.72
10	-0.38	1.22	0.84
11	-0.47	1.38	0.91

Package Information



Device Ordering Information

Product Model	Temperature Range	Packaging Type	Package Quantity	RoHS
DAD9122	-40 ° C ~ +85 ° C	QFN72	168/Reel	Y