DAD7960, 18-Bit, 5 MSPS, SAR ADC

1. FEATURES

- Sampling Rate: 5 MSPS
- 18-bit resolution with no missing codes
- Excellent ac and dc performance(Typical value):
  Dynamic Range (DR): 100dB;
  Signal to Noise Ratio (SNR): 99dB;
- Spurious Free Dynamic Range (SFDR): 115dB;
- Total Harmonic Distortion (THD): -117dB;
- Integral Non-Linearity (INL): ±2.0LSB (maximum)
- Difference Non Linear (DNL): ±0.99LSB (maximum);
- Low power dissipation: 64.5mW;
- Supply voltage: 1.8V/5.0V;
- Differential simulation input range:
- Allow ±VREF (within 0V to +VREF) any input range, VREF maximum value 5V, typical value 4.096V to 5V
- SAR architecture: No latency/pipeline delay
- Digital logic interface: 1.8V
- Serial LVDS interface
- Operating temperature range of −40°C to +85°C
- QFN32 Package

2. APPLICATIONS

- Digital imaging systems
- Digital X-rays
- Computed tomography
- IR cameras
- MRI gradient control
- High speed data acquisition
- Spectroscopy

3. GENERAL DESCRIPTION

The DAD7960 is an 18-bit, 5 MSPS, charge redistribution successive approximation (SAR), analog-to-digital converter (ADC). The SAR architecture allows unmatched performance both in noise and in linearity. The DAD7960contains a low power, high speed, 18-bit sampling ADC, an internal conversion clock, and an internal reference buffer. On the CNV± edge, the DAD7960 samples the voltage difference between the IN+ and IN− pins. The voltages on these pins swing in opposite phase between 0 V and 4.096 V and between 0 V and 5 V. The reference voltage is applied to the part externally. All conversion results are available on a single LVDS self clocked or echoed clock serial interface. The DAD7960 is available in a 32-lead LFCSP (QFN) with operation specified from −40°C to +85°C.

4. Device packaging information

Model	Package Description	Package size
DAD7960	QFN32	5mm×5mm

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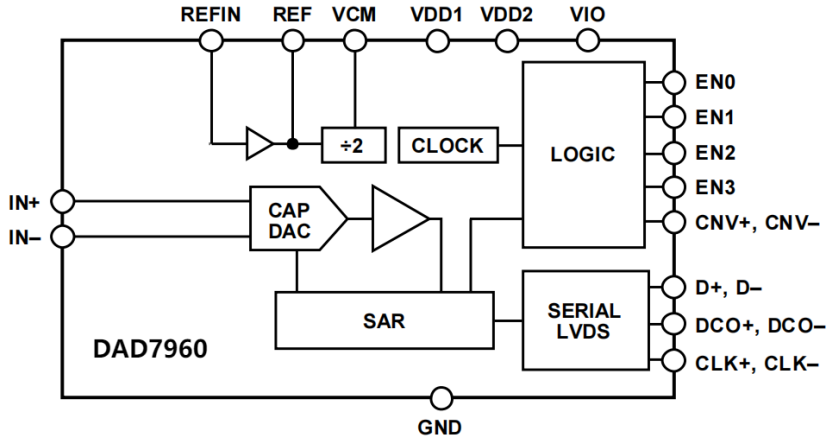
5. FUNCTIONAL BLOCK DIAGRAM



6. PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

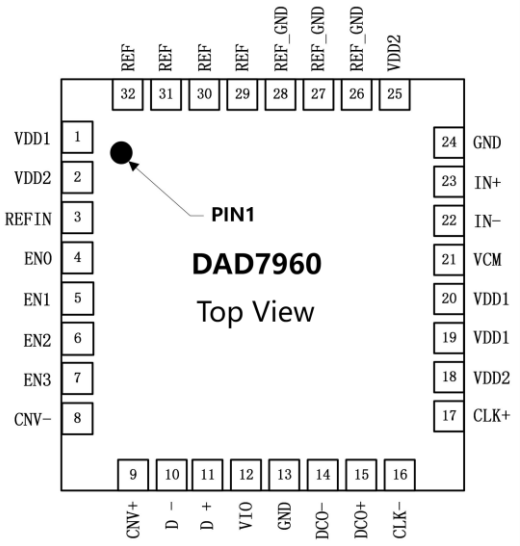


Figure 1. Pin Configuration

Table. Pin Function Description

Mnemonic	Pin No.	Type	Description
VDD1	1, 19, 20	Power	Analog 5 V Supply. Decouple the 5 V supply with a 100 nF capacitor.
VDD2	2, 18, 25	Power	Analog 1.8 V Supply. Decouple this pin with a 100 nF capacitor.
VIO	12	Power	Input/Output Interface Supply. Use a 1.8 V supply and decouple this pin with a 100 nF capacitor.
GND	13, 24	Ground	Ground.
REF_GND	26, 27, 28	Ground	Reference Ground. Connect the capacitors on the REF pin between REF and REF_GND. Tie REF_GND to GND.
REFIN	3	Analog Input	Prebuffer Reference Voltage. It is driven with an external reference voltage of 2.048 V. When driving an external 2.048 V reference, a 100 nF capacitor is required. If using an external 5 V or 4.096 V reference (connected to REF), connect this pin to ground.
EN0, EN1, EN2, EN3	4, 5, 6, 7	Digital Input	The logic levels of these pins can set the operation mode of the device.
CNV−, CNV+	8, 9	Digital Input	Convert Input. These pins act as the conversion control pin. On the rising edge of these pins, the analog inputs are sampled and a conversion cycle is initiated. CNV+ works as a CMOS input when CNV− is grounded; otherwise, CNV+ and CNV− are differential LVDS inputs.
D−, D+	10, 11	Digital Output	LVDS Data Outputs. The conversion data is output serially on these pins.
DCO−, DCO+	14, 15	Digital Output	LVDS Buffered Clock Outputs. When DCO+ is grounded, the self clocked interface mode is selected. In this mode, the 18-bit results on D± are preceded by an initial 0 (which is output at the end of the previous conversion), followed by a 2-bit header (10) to allow synchronization of the data by the digital host with extra logic. The 1 in this header provides the reference to acquire the subsequent conversion result correctly. When DCO+ is not grounded, the echoed clock interface mode is selected. In this mode, DCO± is a copy of CLK±. The data bits are output on the falling edge of DCO+ and can be captured in the digital host on the next rising edge of DCO+.
CLK−, CLK+	16, 17	Digital Input	LVDS Clock Inputs. This clock shifts out the conversion results on the falling edge of CLK+.
VCM	21	Analog Output	Common-Mode Output. When using any reference scheme, this pin produces one-half the voltage present on the REF pin, which can be useful for driving the common mode of the input amplifiers.
IN−	22	Analog Input	Differential Negative Analog Input. Referenced to and must be driven 180° out of phase with IN+.
IN+	23	Analog Input	Differential Positive Analog Input. Referenced to and must be driven 180° out of phase with IN−.
REF	29, 30, 31, 32	Analog Input/ Analog Output	Buffered Reference Voltage. When using the 2.048 V external reference (REFIN input), the 4.096 V system reference is produced at this pin. When using an external reference of 4.096 V or 5 V on this pin, the internal reference buffer must be disabled. Connect the REF pins with the shortest trace possible to a single 10 µF, low ESL, low ESR capacitor. The other side of the capacitor must be placed close to GND.

7.Electrical Specification

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution	RES	V_{DD1}=5V, V_{DD2}=1.8V, V_{IO}=1.8V,		18		Bits
VDD1	I_{VDD1}	EN0-EN3=1001, REFIN=0		0.9	2.0	mA
VDD2	I_{VDD2}	EN0-EN3=1001, REFIN=0		7.8	15	mA
VIO	I_{VIO}	EN0-EN3=1001, REFIN=0		9.0	15	mA
Power Dissipation	PD	EN0-EN3=1001, REFIN=0		35	75	mW
No Missing Codes①	——	f_{IN}=1kHz, V_{REF}=5V		18		Bits
Integral Linearity Error	E_L	f_{IN}=1kHz, V_{REF}=5V	-6.0	+1.5/-1.5	+6.0	LSB
Differential Linearity Error	E_{DL}	f_{IN}=1kHz, V_{REF}=5V	-0.99	+0.85/-0.60	+1.75	LSB
Transition Noise	N_{TRA}	f_{IN}=DC, V_{REF}=5V		1.25	+5.0	LSB
Offset Error	E_O		-25	+1.00	+25	LSB
Offset Error Drift	ΔE_O	f_{IN}=DC, V_{REF}=5V	-8	+0.20	+8	ppm/℃
Gain Error	E_G		-50	-10	+50	LSB
Gain Error Drift	ΔE_G	f_{IN}=DC, V_{REF}=5V	-16	+0.20	+16	ppm/℃
Digital Input in High Level	V_{IH}		1.5	1.5		V
Digital Input in Low Level	V_{IL}	V_{DD1}=5V, V_{DD2}=1.8V, V_{IO}=1.8V		0.3	0.3	V
Dynamic Range	DR	f_{IN}=DC, V_{REF}=5V	94	97.5		dB
		f_{IN}=DC, V_{REF}=4.096V	93	96.0		
Signal-to-Noise Ratio	SNR	f_{IN}=1kHz, V_{REF}=5V	93	95.5		dB
		f_{IN}=1kHz, V_{REF}=4.096V	92	95.0		
Effective Number of Bits	ENOB	f_{IN}=1kHz, V_{REF}=5V	14.9	15.70		bits
		f_{IN}=1kHz, V_{REF}=4.096V	14.8	15.60		
Signal-to-Noise-and-Distortion Ratio	SINAD	f_{IN}=1kHz, V_{REF}=5V	92	95.0		dB
		f_{IN}=1kHz, V_{REF}=4.096V	91.5	94.5		
Spurious-Free Dynamic Range	SFDR	f_{IN}=1kHz, V_{REF}=5V	105	115.0		dB
		f_{IN}=1kHz, V_{REF}=4.096V	101	107.0		
Total Harmonic Distortion	THD	f_{IN}=1kHz, V_{REF}=5V		-113.0	-101	dB
		f_{IN}=1kHz, V_{REF}=4.096V		-108.0	-98	
Sampling Rate	S_{Rmax}	f_{IN}=1kHz, V_{REF}=5V			5	MSPS
Conversion Time Interval	t_{CYC}	f_{IN}=1kHz, V_{REF}=5V	200	200		ns
CNV High Pulse Width	t_{CNVH}	f_{IN}=1kHz, V_{REF}=5V	10	20	120	ns
Output Data Sampling Frequency	f_{CLK}	f_{IN}=1kHz, V_{REF}=5V	150	100	250	MHz
CLK-to-DCO Delay	t_{DCO}	V_{DD1}=5V, V_{DD2}=1.8V, V_{IO}=1.8V,	0	2.8	10	ns

Note: ①No missing codes are characterized by the differential linearity error (EDL). When EDL > -1 LSB, the converter is considered to have no missing codes.

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8.ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Analog Inputs/Outputs	
IN+, IN− to GND	−0.3V to REF +0.3V
REF to GND	−0.3V to +6V
VCM to GND	−0.3V to +6V
REFINto GND	−0.3V to +6V
Supply Voltages	
VDD1	−0.3V to +6V
VDD2, VIO	−0.3V to +2.1V
Digital Inputs to GND	−0.3V to VIO +0.3V
Digital Outputs to GND	−0.3V to VIO +0.3V
Input Current to Any Pin Except Supplies	±10mA
Operating Temperature Range (Commercial)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

8.1Power-Up

As is best practice for all ADCs, power on the core supplies prior to applying an external reference. Apply the analog inputs last. When powering up the DAD7960 device, first apply 1.8 V (VDD2, VIO) to the device, then ramp 5 V (VDD1).

9.TIMING SPECIFICATIONS

VDD1 = 5 V; VDD2 = 1.8 V; VIO = 1.71 V to 1.89 V; REF = 5 V or 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Conversions	t_{CYC}	200			ns
Acquisition Time	t_{ACQ}		t_{CYC} − 115		ns
CNV± High Time	t_{CNVH}	10		0.6 × t_{CYC}	ns
CNV± to D± (MSB) Ready	t_{MSB}			200	ns
CNV± to Last CLK± (LSB) Delay	t_{CLKL}			160	ns
CLK± Period[1]	t_{CLK}	3.33	4	(t_{CYC}−t_{MSB}+t_{CLKL})/n	ns
CLK± Frequency	f_{CLK}		250	300	MHz
CLK± to DCO± Delay (Echoed Clock Mode)	t_{DCO}	0	3	5	ns
DCO± to D± Delay (Echoed Clock Mode)	t_D		0	1	ns
CLK± to D± Delay	t_{CLKD}	0	3	5	ns

Note: 1. For the maximum CLK± period, the window available to read data is t_{CYC} − t_{MSB} + t_{CLKL}. Divide this time by the number of bits (n) to be read, giving the maximum CLK± frequency that can be used for a given conversion CNV± frequency. In echoed clock interface mode, n = 18; in self clocked interface mode, n = 20.

Timing Diagrams

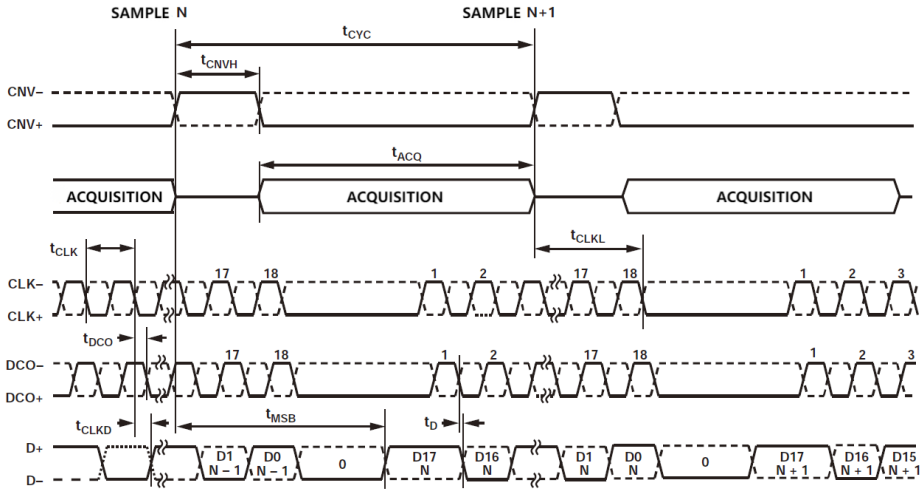

Figure 2. Echoed Clock Interface Mode Timing Diagram

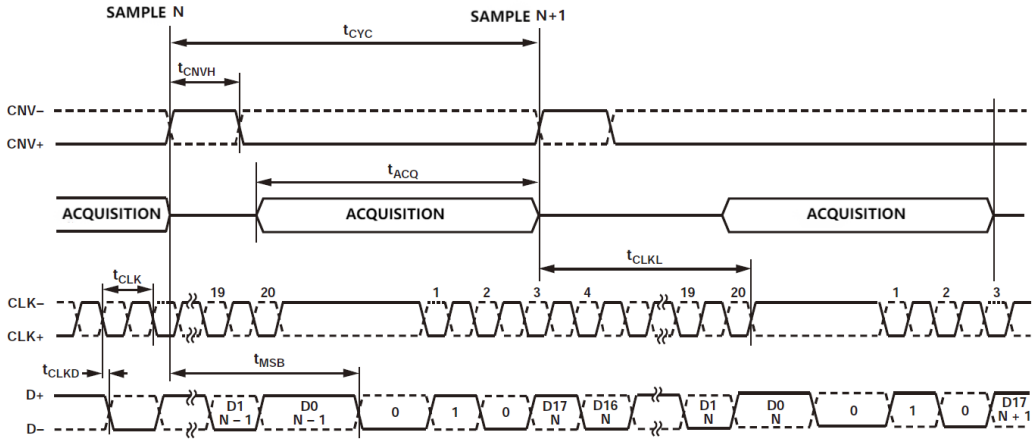

Figure 3. Self Clocked Interface Mode Timing Diagram

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10. TERMINOLOGY

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the rms noise measured for an input typically at −60 dB. The value for dynamic range is expressed in decibels.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

Gain Error

The first transition (from 100 … 000 to 100 …001) should occur at a level ½ LSB above nominal negative full scale (−4.0959844 V for the ±4.096 V range). The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.095953 V for the ± 4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift

The ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million.

Least Significant Bit (LSB)

The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\mathrm{V}) = \frac{V_{INp\text{-}p}}{2^N}$$

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal (including harmonics).

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Zero Error

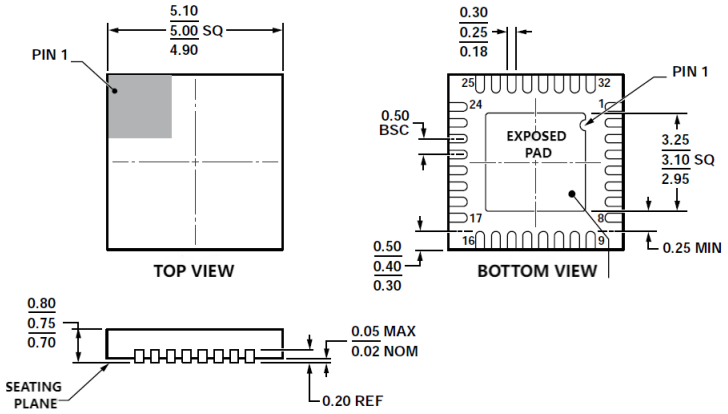
Zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Zero Error Drift

The ratio of the zero error change due to a temperature change of 1°C and the full-scale code range (2^N). It is expressed in parts per million.

11. OUTLINE DIMENSIONS

QFN32 Package



12. ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
DAD7960	-40℃~85℃	QFN32	490/tray

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