DAD7616 16-Channel DAS with 16-Bit, Bipolar Input, Dual Simultaneous Sampling ADC

FEATURES

- 16-channel, dual, simultaneously sampled inputs
- Independently selectable channel input ranges
- True bipolar: ±10 V, ±5 V, ±2.5 V
- Single 5 V analog supply and 2.3 V to 5.5 V V Drive supply
- Fully integrated data acquisition solution
  Analog input clamp protection
  Input buffer with 1 MΩ analog input impedance
  First-order anti-aliasing analog filter
  On-chip accurate reference voltage and reference voltage buffer
  Dual 16-bit successive approximation register (SAR) ADC
  Throughput rate: 2 × 1 MSPS
  Oversampling capability with digital filter
  Flexible sequencer with burst mode
- Flexible parallel/serial interface
  SPI/QSPI/MICROWIRE/DSP compatible
  Optional Cyclic Redundancy Check (CRC) error checking
- Hardware/software configuration
- Performance
  90.5 dB SNR
  −101 dB THD
  ±1 LSB INL (typical), ±0.99 LSB DNL (maximum)
  8 kV ESD rating on analog input channels
- On-chip self detect function
- Low power consumption: 150mW
- 80-lead LQFP package

APPLICATIONS

- Power line monitoring
- Protective relays
- Multiphase motor control
- Instrumentation and control systems
- Data acquisition systems (DAS)

GENERAL DESCRIPTION

The DAD7616 is a 16-bit, DAS that supports dual simultaneous sampling of 16 channels. The DAD7616 operates from a single 5 V supply and can accommodate ±10 V, ±5 V, and ±2.5 V true bipolar input signals while sampling at throughput rates up to 2 MSPS per channel pair with 90.5 dB SNR. Higher SNR performance can be achieved with the on-chip oversampling mode (91.1 dB for an oversampling ratio (OSR) of 2). The input clamp protection circuitry can tolerate voltages up to ±16 V. The DAD7616 has 1 MΩ analog input impedance, regardless of sampling frequency. The single-supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies.

The device contains analog input clamp protection, a dual, 16-bit charge redistribution SAR analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.

The DAD7616 is serial peripheral interface (SPI)/QSPI/DSP/ MICROWIRE compatible.

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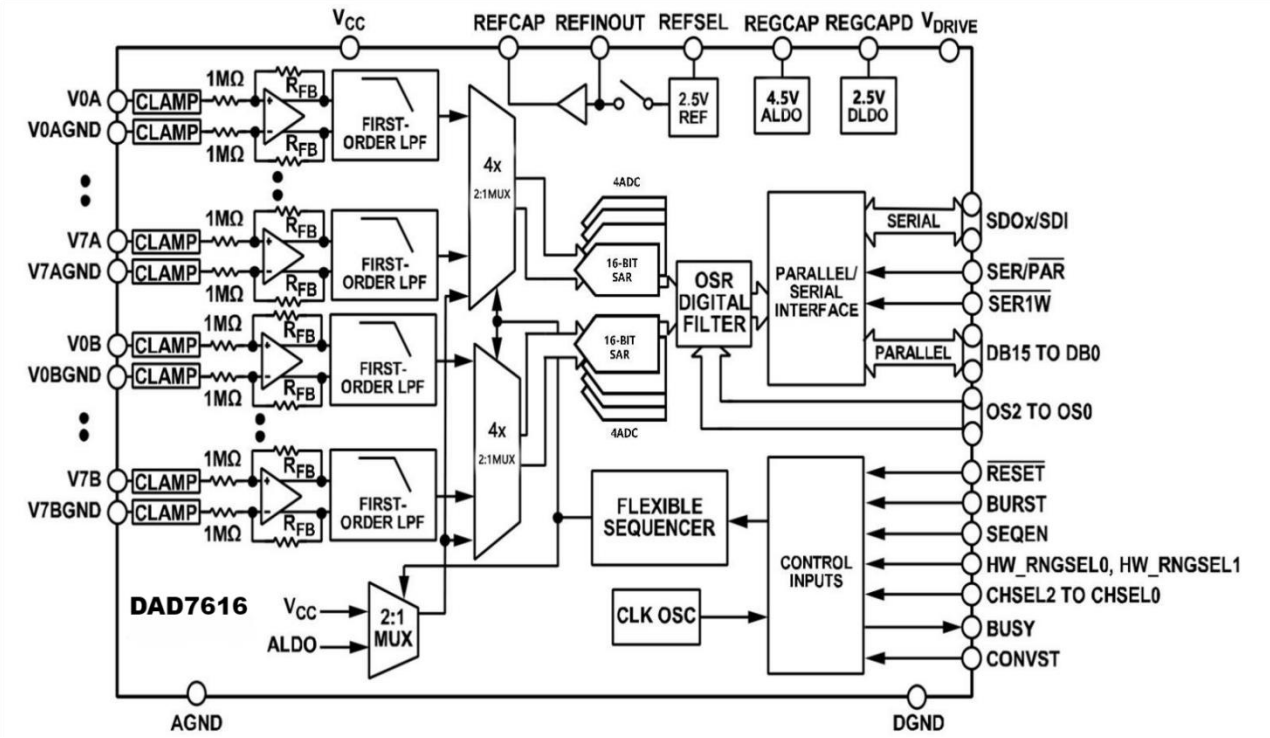
FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS

V_{REF} = 2.5 V external/internal, V_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.5 V, f_{SAMPLE} = 1 MSPS, T_A = −40°C to +125°C, unless otherwise noted.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	fIN = 1 kHz sine wave unless otherwise noted				
Signal-to-Noise Ratio (SNR) 1	No oversampling, ±10 V range	89	89.5		dB
	OSR = 2, ±10 V range3		91		dB
	OSR = 4, ±10 V range3		92		dB
	No oversampling, ±5 V range	88	88.5		dB
	No oversampling, ±2.5 V range	85.5	86		dB
Signal-to-Noise-and-Distortion (SINAD)	No oversampling, ±10 V range	88.5	90		dB
	No oversampling, ±5 V range	87.5	89		dB
	No oversampling, ±2.5 V range	85	87		dB
Dynamic Range	No oversampling, ±10 V range		92		dB
	No oversampling, ±5 V range		90.5		dB
	No oversampling, ±2.5 V range		88		dB
Total Harmonic Distortion (THD)	No oversampling, ±10 V range		− 104	−93.5	dB
	No oversampling, ±5 V range		− 101		dB
	No oversampling, ±2.5 V range		−98		dB
Peak Harmonic or Spurious Noise			− 103		dB
Intermodulation Distortion (IMD)	fa = 1 kHz , fb = 1.1 kHz				
Second-Order Terms			− 105		dB
Third-Order Terms			− 113		dB
Channel to Channel Isolation	f_{IN} on unselected channels up to 5 kHz		− 106		dB
ANALOG INPUT FILTER					
Full Power Bandwidth	−3 dB, ±10 V range		39		kHz
	−3 dB , ±5 V/2.5 V range		33		kHz
	−0.1 dB		5.5		kHz
Phase Delay2	±10 V range		4.4	6	µs
	±5 V range		5		µs
	±2.5 V range		4.9		µs
Phase Delay Drift3	±10 V range		±0.55	5	ns/°C
Phase Delay Matching (Dual Simultaneous Pair)2	±10 V range		4.4	100	ns
	±5 V range		4.7		ns
	±2.5 V range		4.1		ns

DC ACCURACY					
Resolution	No missing codes	16			Bits
Differential Nonlinearity (DNL)			±0.5	±0.99	LSB4
Integral Nonlinearity (INL)			±1	±2	LSB
Total Unadjusted Error (TUE)	±10 V range		±6		LSB
	±5 V range		±8		LSB
	±2.5 V range		±10		LSB
Positive Full-Scale Error4					
External reference	±10 V range		±5	±32	LSB
	±5 V range		± 4		LSB
	±2.5 V range		± 2		LSB
Internal reference	±10 V range		±5		LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Positive Full-Scale (PFS) Error Drift2	External reference		±2	±5	ppm/°C
	Internal reference		±3	±10	ppm/°C
Positive Full-Scale Error Matching	±10 V range		3	11	LSB
	±5 V range		4		LSB
	±2.5 V range		8		LSB
Bipolar Zero Code Error	±10 V range		±0.8	±8	LSB
	±5 V range		±1	±10	LSB
	±2.5 V range		±3	±15	LSB
Bipolar Zero Code Error Drift3	±10 V range		±1.3	±20.4	µV/°C
	±5 V range		±0.9		µV/°C
	±2.5 V range		±0.5		µV/°C
Bipolar Zero Code Error Matching	±10 V range		±2	±10	LSB
	±5 V range		±3		LSB
	±2.5 V range		±3		LSB
Negative Full-Scale (NFS) Error4	External reference			±32	
	±10 V range		±4		LSB
	±5 V range		±3		LSB
	±2.5 V range		±6		LSB
	Internal reference			±5	
	±10 V range		±3		LSB
Negative Full-Scale Error Drift2	External reference		±2	12	ppm/°C
	Internal reference		±4		ppm/°C
Negative Full-Scale Error Matching	±10 V range		4		LSB
	±5 V range		4		LSB
	±2.5 V range		8		LSB

ANALOG INPUT					
Input Voltage Ranges	Software/hardware selectable			±10	V
	Software/hardware selectable			±5	V
	Software/hardware selectable			±2.5	V
Analog Input Current	±10 V range，see Figure 34		±10.5		μA
	±5 V range，see Figure 34		±6.5		μA
	±2.5 V range，see Figure 34		±4		μA
Input Capacitance			10		pF
Input Impedance	See the Analog Input section	0.85	1		MΩ
Input Impedance Drift3				25	ppm/°C
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range	See the ADC Transfer Function section	2.498	2.5	2.501	V
DC Leakage Current				±1	μA
Input Capacitance	REFSEL = 1		7.5		pF
Reference Output Voltage	REFINOUT	2.498		2.501	V
Reference Temperature Coefficient3			±2	±15	ppm/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Voltage					
High (V INH)	V DRIVE = 2.7 V to 5.5 V	2			V
	V DRIVE = 2.3 V to 2.7 V	1.7			V
Low (V INL)	V DRIVE = 2.7 V to 5.5 V			0.8	V
	V DRIVE = 2.3 V to 2.7 V			0.7	V
Input Current (I IN)				±1	μA
Input Capacitance (C IN)			5		pF
LOGIC OUTPUTS					
Output Voltage					
High (VOH)	I SOURCE = 100 μA	VDRIVE − 0.2			V
Low (VOL)	I SINK = 100 μA			0.4	V
Floating State Leakage Current			±0.005	±1	μA
Floating State Output Capacitance			5		pF
Output Coding	Twos complement				
CONVERSION RATE					
Conversion Time	Per channel pair		4		μs
Acquisition Time	Per channel pair		0.5		μs
Throughput Rate	Per channel pair			2 x 200	KSPS
Conversion Time	Burst Sequencer Mode (8-Pair Channel Acquisition)		14u		
Acquisition Time	Burst Sequencer Mode (8-Pair Channel Acquisition)		0.5u		
Throughput Rate	Burst Sequencer Mode (8-Pair Channel Acquisition)			2 x 550	KSPS

POWER REQUIREMENTS					
V_{CC}		4.75		5.25	V
V DRIVE		2.3		5.5	V
IVCC					
Normal Mode Current	f_{SAMPLE} (1MSPS) [5]		28	32	mA
Shutdown Mode Current			2		mA
Power Consumption in Normal Mode	f_{SAMPLE} (1MSPS) [5]		140		mW
Power Consumption in Shutdown Mode			11		mW

1 Not production tested. Samples were tested during the initial release to ensure compliance with standard specifications.

2 LSB means least significant bit. With a ±2.5 V input range, 1 LSB = 76.293 μV. With a ±5 V input range, 1 LSB = 152.58 μV. With a ±10 V input range, 1 LSB = 305.175 μV.

3 Positive and negative full-scale error for the internal reference excludes reference errors.

4 Supported by simulation data.

5 The DAD7616 integrates eight 250 KSPS simultaneous-sampling cores, delivering a total throughput of 2 MSPS.

TIMING SPECIFICATIONS

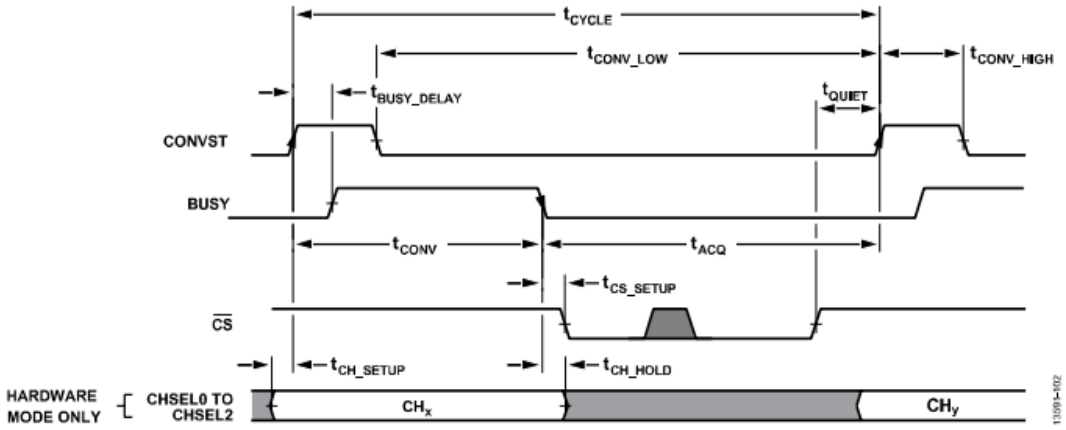
Universal Timing Specifications

V_{CC}= 4.75 V to 5.25 V, V_{DRIVE}= 2.3 V to 5.5V, V_{REF}= 2.5 V external reference/internal reference, T_A= −40°C to +125°C, unless otherwise noted. Interface timing tested using a load capacitance of 30pF, dependent on V_{DRIVE} and load capacitance for serial interface.

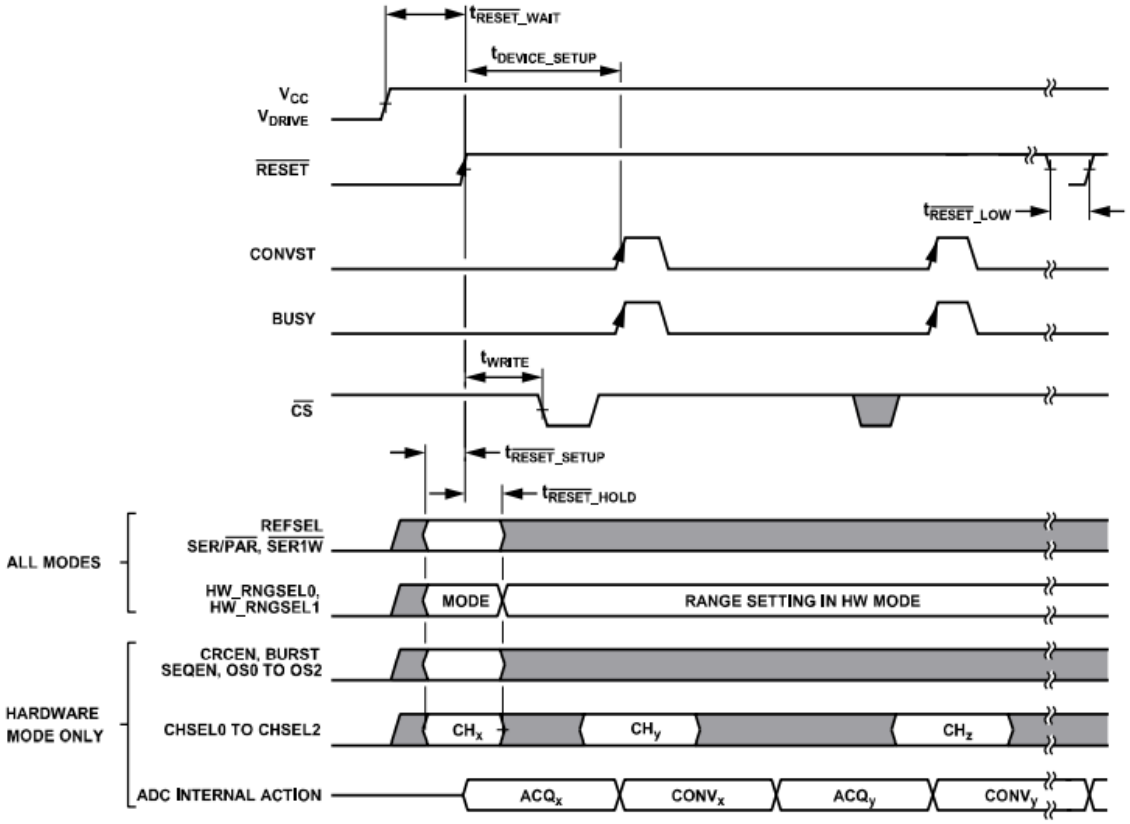
Table.

Parameter1	Min	Typ	Max	Unit	Description
t_{CYCLE}	4.5			µs	Minimum time between consecutive CONVST rising edges (excluding burst and oversampling modes)
t_{CONV_LOW}	50			ns	CONVST low pulse width
t_{CONV_HIGH}	50			ns	CONVST high pulse width
t_{BUSY_DELAY}			32	ns	CONVST high to BUSY high (manual mode)
t_{CS_SETUP}	20			ns	BUSY falling edge to CS falling edge setup time
t_{CH_SETUP}	50			ns	Channel select setup time in hardware mode for CHSELx
t_{CH_HOLD}	20			ns	Channel select hold time in hardware mode for CHSELx
t_{CONV}			4	us	Conversion time for the selected channel pair
t_{ACQ}	480			ns	Acquisition time for the selected channel pair
t_{QUIET}	50				CS rising edge to next CONVST rising edge
t_{RESET_LOW}			500	ns	
Partial Reset	150			µs	Partial RESET low pulse width
Full Reset	1.2				Full RESET low pulse width
t_{DEVICE_SETUP}					
Partial Reset	50			ns	Time between partial RESET high and CONVST rising edge
Full Reset	15			ms	Time between full RESET high and CONVST rising edge
t_{WRITE}				ns	
Partial Reset	50			µs	Time between partial RESET high and CS for write operation
Full Reset	240			ms	Time between full RESET high and CS for write operation
t_{RESET_WAIT}	1				Time between stable V_{CC}/V_{DRIVE} and release of RESET (see Figure 50)
t_{RESET_SETUP}					Time prior to release of $\overline{\text{RESET}}$ that queried hardware inputs must be stable for (see Figure 50)
Partial Reset	10			ns	
Full Reset	0.05			ms	
t_{RESET_HOLD}					Time after release of RESET that queried hardware inputs must be stable for (see Figure 50)
Partial Reset	10			ns	
Full Reset	0.24			ms	

Universal Timing Diagram Across All Interfaces



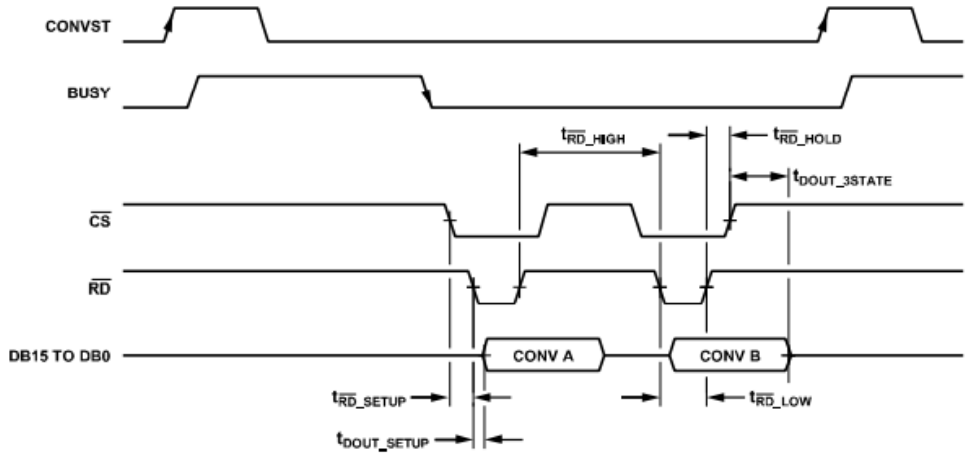
Reset Timing Diagram



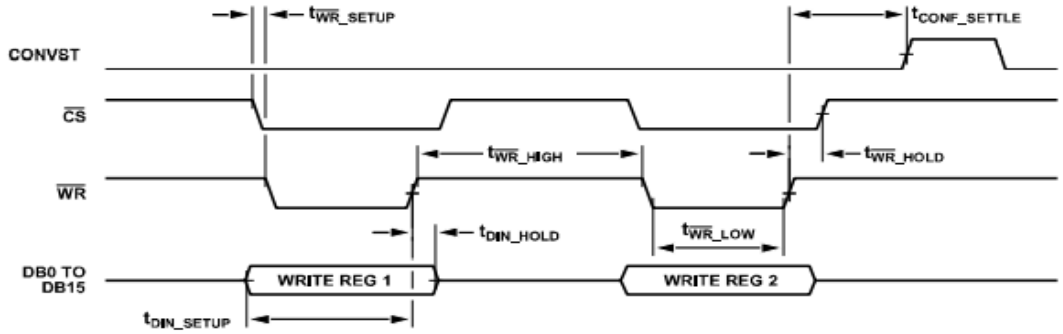
Parallel Mode Timing Specifications

Parameter	Min	Typ	Max	Unit	Description
t_{RD_SETUP}	10			ns	CS falling edge to RD falling edge setup time
t_{RD_HOLD}	10			ns	RDb rising edge to CS rising edge hold time
t_{RD_HIGH}	10			ns	RDb high pulse width
t_{RD_LOW}	30			ns	RDb low pulse width
t_{DOUT_SETUP}	30			ns	Data access time after falling edge of RDb
t_{DOUT_3STATE}	11			ns	CS rising edge to DBx high impedance
t_{WR_SETUP}	10			ns	CS to WR setup time
t_{WR_HIGH}	20			ns	WRb high pulse width
t_{WR_LOW}	30			ns	WRb low pulse width
t_{WR_HOLD}	10			ns	WRb hold time
t_{DIN_SETUP}	30			ns	Configuration data to WRb setup time
t_{DIN_HOLD}	10			ns	Configuration data to WRb hold time
t_{CONF_SETTLE}	20			ns	Configuration data settle time, WRb rising edge to CONVST rising edge

Parallel Read Timing Diagram



Parallel Write Timing Diagram

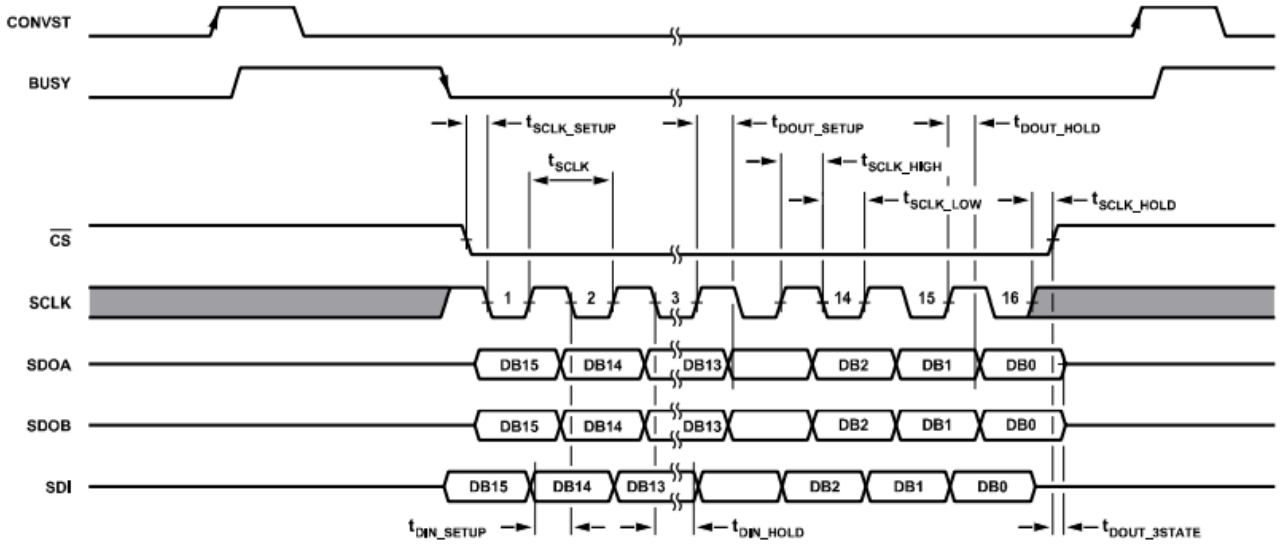


Serial Mode Timing Specifications

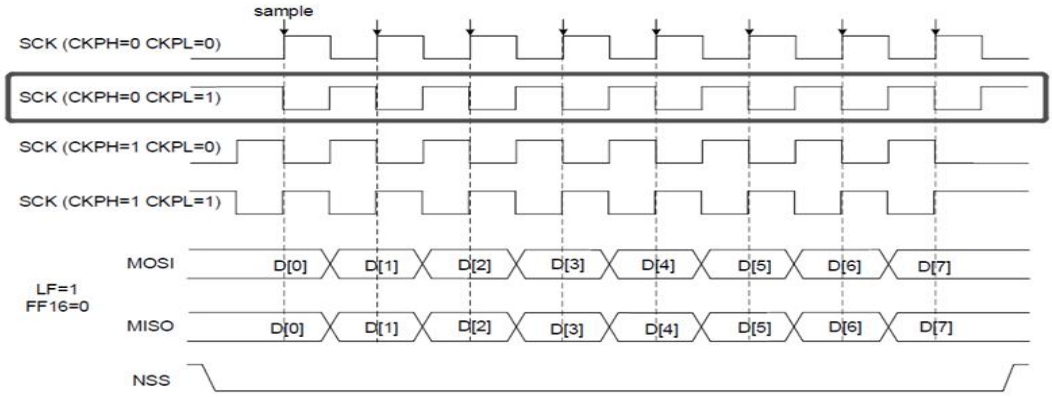
Parameter	Min	Typ	Max	Unit	Description
f_{SCLK}[1]			35	MHz	SCLK frequency
t_{SCLK}	1/fSCLK				Minimum SCLK period
t_{SCLK_SETUP}[1]	10.5			ns	CS to SCLK falling edge setup time, VDRIVE above 3 V
	13.5			ns	CS to SCLK falling edge setup time, VDRIVE above 2.3 V
t_{SCLK_HOLD}	10			ns	SCLK to CS rising edge hold time
t_{SCLK_LOW}	14			ns	SCLK low pulse width
t_{SCLK_HIGH}	14			ns	SCLK high pulse width
t_{DOUT_SETUP}[1]			9	ns	Data out access time after SCLK rising edge, VDRIVE above 3 V
			11	ns	Data out access time after SCLK rising edge, VDRIVE above2.3 V
t_{DOUT_HOLD}	4			ns	Data out hold time after SCLK rising edge
t_{DIN_SETUP}	10			ns	Data in setup time before SCLK falling edge
t_{DIN_HOLD}	8			ns	Data in gold time after SCLK falling edge
t_{DOUT_3STATE}			10		CS rising edge to SDOx high impedance

1 Dependent on VDRIVE and load capacitance (see Table 14).

Serial Timing Diagram



Recommended Host-Side Sampling Method for UART Data Read/Write Operations



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Parameter	Rating
V_{CC} to AGND	−0.3 V to+7 V
V_{DRIVE} to AGND	−0.3 V to V_{CC} + 0.3 V
Analog Input Voltage to AGND1	±21 V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFINOUT to AGND	−0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies 1	±10 mA
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Soldering Reflow	
Pb/Sn Temperature (10 sec to 30 sec)	240 (+0)°C
Pb/-free Temperature	260 (+0)°C
ESD	
All Pins Except Analog Inputs	2 kV
Analog Input Pins Only	8 kV

Transient currents below 100 mA will not trigger latch-up in the silicon-controlled rectifier (SCR).

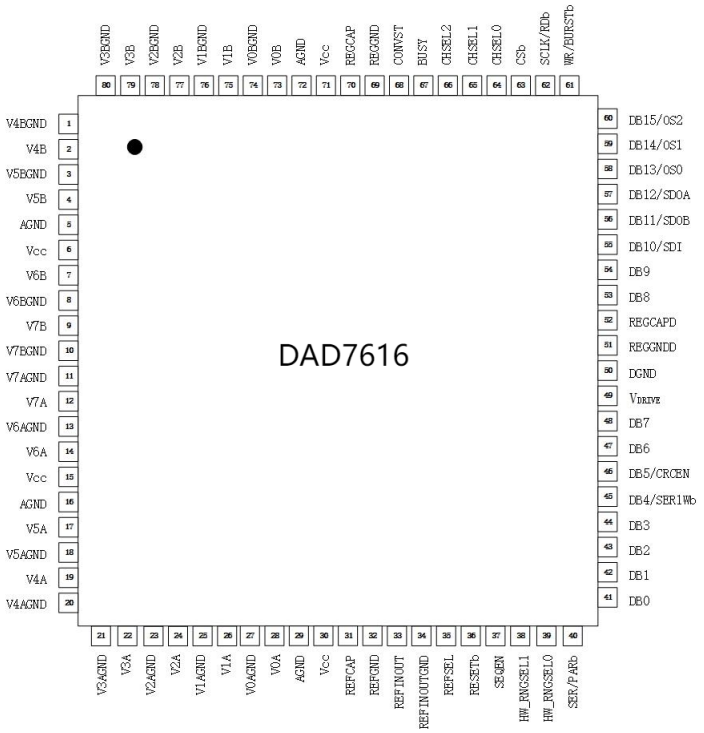
Note: Exceeding or operating at the absolute maximum ratings may result in permanent damage to the device. These ratings are stress limits only and do not imply functional operation under these or any other conditions beyond those specified in the operational sections of this datasheet. Prolonged exposure to conditions exceeding the maximum ratings may affect device reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS(Note: The letter "b" is equivalent to a blank line)



Pin Function Descriptions

Pin No.	Type[1]	Mnemonic[2]	Description
1	AI GND	V4BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V4B.
2	AI	V4B	Analog Input for Channel 4, ADC B.
3	AI GND	V5BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V5B.
4	AI	V5B	Analog Input for Channel 5, ADC B.
5, 16, 29, 72	P	AGND	Analog Supply Ground Pins.
6, 15, 30, 71	P	V_{CC}	Analog Supply Voltage, 4.7 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. Decouple these pins to AGND using 0.1 µF and 10 µF capacitors in parallel.
7	AI	V6B	Analog Input for Channel 6, ADC B.
8	AI GND	V6BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V6B.
9	AI	V7B	Analog Input for Channel 7, ADC B.
10	AI GND	V7BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V7B.
11	AI GND	V7AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V7A.
12	AI	V7A	Analog Input for Channel 7, ADC A.
13	AI GND	V6AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V6A.
14	AI	V6A	Analog Input for Channel 6, ADC A.
17	AI	V5A	Analog Input V5A.
18	AI GND	V5AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V5A.
19	AI	V4A	Analog Input V4A.
20	AI GND	V4AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V4A.

Pin No.	Type[1]	Mnemonic[2]	Description
21	AIGND	V3AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V3A.

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22	AI	V3A	Analog Input for Channel 3, ADC A.
23	AIGND	V2AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V2A.
24	AI	V2A	Analog Input for Channel 2, ADC A.
25	AIGND	V1AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V1A.
26	AI	V1A	Analog Input for Channel 1, ADC A.
27	AIGND	V0AGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V0A.
28	AI	V0A	Analog Input for Channel 0, ADC A.
31	CAP	REFCAP	Reference Buffer Output Force/Sense Pin. Decouple this pin to AGND using a low effective series resistance (ESR), 10 µF, X5R ceramic capacitor, as close to the REFCAP pin as possible. The voltage on this pin is typically 4.096 V.
32	CAP	REFGND	Reference Ground pin. Connect this pin to AGND.
33	REF	REFINOUT	Reference Input/Reference Output. The on-chip reference of 2.5 V is available on this pin for external use when the REFSEL pin is set to logic high. Alternatively, the internal reference can be disabled by setting the REFSEL pin to logic low, and an external reference of 2.5 V can be applied to this input. Decoupling is required on this pin for both the internal and external reference options. Connect a 100 nF, X8R capacitor between the REFINOUT and REFINOUTGND pins, as close to the REFINOUT pin as possible. If using an external reference, connect a 10 kΩ series resistor to this pin to band limit the reference signal.
34	CAP	REFINOUTGND	Reference Input, Reference Output Ground Pin.
35	DI	REFSEL	Internal/External Reference Selection Input. REFSEL is a logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFINOUT pin. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
36	DI	RESETb	Reset Input. Full and partial reset options are available. The type of reset is determined by the length of the RESET pulse. Keeping RESET low places the device into shutdown mode. See the Reset Functionality section for further details.
37	DI	SEQEN	Channel Sequencer Enable Input (Hardware Mode Only). When SEQEN is tied low, the sequencer is disabled. When SEQEN is high, the sequencer is enabled (with restricted functionality in hardware mode). See the Sequencer section for further details. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. In software mode, this pin must be connected to DGND.
38,39	DI	HW_RNGSEL1, HW_RNGSEL0	Hardware/Software Mode Selection, Hardware Mode Range Select Inputs. Hardware/software mode selection is latched at full reset. Range selection in hardware mode is not latched. HW_RNGSELx = 00: software mode; DAD7616 is configured via the software registers. HW_RNGSELx = 01: hardware mode; analog input range is ±2.5 V. HW_RNGSELx = 10: hardware mode; analog input range is ±5 V. HW_RNGSELx = 11: hardware mode; analog input range is ±10 V.

40	DI	SER/PARb	Serial/Parallel Interface Selection Input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to logic high, the serial interface is selected. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
41,42,43,44	DO/DI	DB0,DB1,DB2,DB3	Parallel Output/Input Data Bit 0 to Data Bit 3. In parallel mode, these pins are output/input parallel data bits, DB7 to DB0. Refer to the Parallel Interface section for further details. In serial mode, these pins must be tied to DGND.
45	DO/DI	DB4/SER1Wb	Parallel Output/Input Data Bit 4/Serial Output Selection. In parallel mode, this pin acts as a threestate parallel digital output/input pin. Refer to the Parallel Interface section for further details. In serial mode, this pin determines whether the serial output operates over SDOA and SDOB or just SDOA. When SER1W is low, the serial output operates over SDOA only. When SER1W is high, the serial output operates over both SDOA and SDOB. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure.
46	DO/DI	DB5/CRCEN	Parallel Output/Input Data Bit 5/CRC Enable Input. In parallel mode, this pin acts as a three-state parallel digital input/output. While in serial mode, this pin acts as a CRC enable input. The CRCEN signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. Refer to the Digital Interface section for further details. In serial mode, when CRCEN is low, there is no CRC word following the conversion results; when CRCEN is high, an extra CRC word follows the last conversion word configured by CHSELx. See the CRC section for further details. In software mode, this pin must be connected to DGND.
47,48	DO/DI	DB6,DB7	Parallel Output/Input Data Bit 6 and Data Bit 7. When SER/PAR = 0, these pins act as threestate parallel digital input/outputs. Refer to the Parallel Interface section for further details. In serial mode, when SER/PAR = 1, these pins must be tied to DGND.
49	P	V_{DRIVE}	Logic Power Supply Input. The voltage (2.3 V to 5.5 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface. Decouple this pin with 0.1 µF and 10 µF capacitors in parallel.
50	P	DGND	Digital Ground. This pin is the ground reference point for all digital circuitry on the DAD7616. The DGND pin must connect to the DGND plane of a system.
51	CAP	REGGNDD	Ground for the Digital Low Dropout (LDO) Regulator Connected to REGCAPD (Pin 52).
52	CAP	REGCAPD	Decoupling Capacitor Pin for Voltage Output from Internal Digital Regulator. Decouple this output pin separately to REGGNDD using a 10 µF capacitor. The voltage at this pin is 2.6 V typical.
53,54	DO/DI	DB8、DB9	Parallel Output/Input Data Bit 9 and Data Bit 8. When SER/PAR = 0, these pins act as threestate parallel digital input/outputs. Refer to the Parallel Interface section for further details. In serial mode, when SER/PAR = 1, these pins must be tied to DGND.
55	DO/DI	DB10/SDI	Parallel Output/Input Data Bit DB10/Serial Data Input. When SER/PAR = 0, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface

			section for further details. In hardware serial mode, tie this pin to DGND. In serial mode, when SER/PAR = 1, this pin acts as the data input of the SPI interface.
56	DO/DI	DB11/SDOB	Parallel Output/Input Data Bit 11/Serial Data Output B. When SER/PAR = 0, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface section for further details. In serial mode, when SER/PAR = 1, this pin functions as SDOB and outputs serial conversion data.
57	DO/DI	DB12/SDOA	Parallel Output/Input Data Bit 12/Serial Data Output A. When SER/PAR = 0, this pin acts as a three-state parallel digital input/output. Refer to the Parallel Interface section for further details. In serial mode, when SER/PAR = 1, this pin functions as SDOA and outputs serial conversion data.
58,59,60	DO/DI	DB13/OS0 DB14/OS1 DB15/OS2	Parallel Output/Input Data Bit 13, Data Bit 14, and Data Bit 15/Oversampling Ratio Selection. When SER/PAR = 0, these pins act as three-state parallel digital input/outputs. Refer to the Parallel Interface section for further details. In serial hardware mode, these pins control the oversampling settings. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. See the Digital Filter section for further details. In software serial mode, these pins must be connected to DGND.
61	DI	WRb/BURST	Write/Burst Mode Enable. In software parallel mode, this pin acts as WR for a parallel interface. In hardware parallel or serial mode, this pin enables BURST mode. The signal state is latched on the release of a full reset, and requires an additional full reset to reconfigure. Refer to the Burst Sequencer section for further information. In software serial mode, connect this pin to DGND.
62	DI	SCLK/RDb	Serial Clock Input/Parallel Data Read Control Input. In serial mode, this pin acts as the serial clock input for data transfers. The CSb falling edge takes the SDOA and SDOB data output lines out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the SDOA and SDOB serial data outputs. When CSb is logic low in parallel mode, the output bus is enabled.
63	DI	CSb	Chip Select. This active low logic input frames the data transfer. In parallel mode, when CSb is logic low, the DBx output bus is enabled and the conversion result is output on the parallel data bus lines. In serial mode, CSb frames the serial read transfer and output the MSB of the serial output data.
64,65,66	DI	CHSEL0,CHSEL1,CHSEL2	Channel Selection Input 0 to Input 2. In hardware mode, these inputs select the input channels for the next conversion in Channel Group A and Channel Group B. For example, CHSELx = 0x000 selects V0A and V0B for the next conversion; CHSELx = 0x001 selects V1A and V1B for the next conversion. In software mode, these pins must be connected to DGND.
67	DO	BUSY	Busy Output. This pin transitions to a logic high after a CONVST rising edge and indicates that the conversion process has started. The BUSY output remains high

			until the conversion process for the current selected channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and is available to read. Data must be read after BUSY returns to low. Rising edges on CONVST have no effect while the BUSY signal is high.
68	DI	CONVST	Conversion Start Input for Channel Group A and Channel Group B. This logic input initiates conversions on the analog input channels. A conversion is initiated when CONVST transitions from low to high for the selected analog input pair. When burst mode and oversampling mode are disabled, every CONVST transition from low to high converts one channel pair. In sequencer mode, when burst mode or oversampling is enabled, a single CONVST transition from low to high is necessary to perform the required number of conversions.
69	CAP	REGGND	Internal Analog Regulator Ground. This pin must connect to the AGND plane of a system.
70	CAP	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Analog Regulator. Decouple this output pin separately to REGGND using a 10 µF capacitor. The voltage at this pin is 4.5 V typical.
73	AI	V0B	Analog Input for Channel 0, ADC B.
74	AI GND	V0BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V0B.
75	AI	V1B	Analog Input for Channel 1, ADC B.
76	AI GND	V1BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V1B.
77	AI	V2B	Analog Input for Channel 2, ADC B.
78	AI GND	V2BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V2B.
79	AI	V3B	Analog Input for Channel 3, ADC B.
80	AI GND	V3BGND	Analog Input Ground Pin. This pin corresponds to Analog Input Pin V3B.

1 AI is analog input, GND is ground, P is power supply, REF is reference input/output, DI is digital input, DO is digital output, and CAP is decoupling capacitor pin.

2 Note that throughout this datasheet, multifunction pins, such as SER/PAR, are referred to either by the entire pin name or by a single function of the pin, for example, SER, when only that function is relevant.

Functional Description

The DAD7616 is a high-speed, low-power, charge-redistribution Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)–based data acquisition system capable of dual simultaneous sampling across 16 analog input channels. The analog inputs of the DAD7616 support true bipolar input signals, with selectable input ranges of ±10 V, ±5 V, and ±2.5 V. The device operates from a single 5 V analog power supply.

The DAD7616 integrates input clamp protection, input signal scaling amplifiers, a first-order anti-aliasing filter, an on-chip reference voltage source with reference buffer, dual high-speed ADC cores, digital filters, a flexible sequencer, and high-speed parallel and serial interfaces.

By controlling the HW_RNGSELx pins, the DAD7616 can operate in either hardware mode or software mode. In hardware mode, device configuration is managed through dedicated hardware pins. In software mode, configuration is performed via control registers accessed through the serial or parallel interface.

Analog Inputs

Analog Input Channel Selection

The DAD7616 integrates two 16-bit ADC cores that perform simultaneous sampling. Each ADC supports 8 analog input channels, providing a total of 16 analog input channels. In addition, the DAD7616 includes on-chip diagnostic channels for monitoring the VCC power supply and the on-chip adjustable low dropout (LDO) regulator.

Channel selection for conversion can be made either through CHSELx pins in hardware mode or via channel selection registers in software mode. Sampling of the diagnostic channels is only available in software mode.

The converter allows dynamic channel selection or predefined channel sequencing using the internal sequencer of the DAD7616.

In hardware mode, only corresponding A and B channel pairs can be sampled simultaneously (for example, channel V0A is always sampled together with V0B). In software mode, any A-channel can be paired with any B-channel for synchronous sampling.

Analog Input Range

The DAD7616 supports true bipolar and single-ended analog input voltages. The logic levels on the HW_RNGSEL0 and HW_RNGSEL1 range selection pins determine the analog input range for all input channels. If both range selection pins are held low, the analog input range in software mode is determined by the Input Range Register (refer to the Register Summary section for details). In software mode, each channel can be individually configured with its own input range.

In hardware mode, any change in the logic state of these range selection pins immediately affects the analog input range. However, in addition to the normal acquisition time requirement, a typical settling time of approximately 120 µs is required.It is recommended to hardware the range selection pins according to the desired system input range.

Analog Input Impedance

The DAD7616 features a fixed analog input impedance of 1 MΩ, which remains constant regardless of the ADC sampling rate. The high input impedance eliminates the need for a front-end driver amplifier, allowing the DAD7616 to be directly connected to signal sources or sensors for analog input.

Analog Input Clamp Protection

Figure 41 illustrates the analog input circuitry of the DAD7616. Each analog input channel includes an input clamp protection circuitry. Although the device operates from a single 5 V analog power supply, the input clamp protection allows the analog inputs to tolerate overvoltage conditions from –16 V to +16 V.

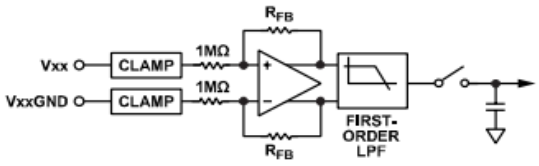


Table 8. Analog Input Range Selection

Analog Input Range	HW RNGSEL1	HW RNGSEL0
Configured Via the Input Range Registers	0	0
±2.5 V	0	1
±5 V	1	0
±10 V	1	1

Analog Input Channel Characteristics

The figure below illustrates the relationship between the input clamp current and the source voltage of the clamp circuit. For source voltages between –16 V and +16 V, no current flows through the clamp circuit. When the input voltage exceeds +16 V or falls below –16 V, the DAD7616 input clamp protection circuit becomes active.

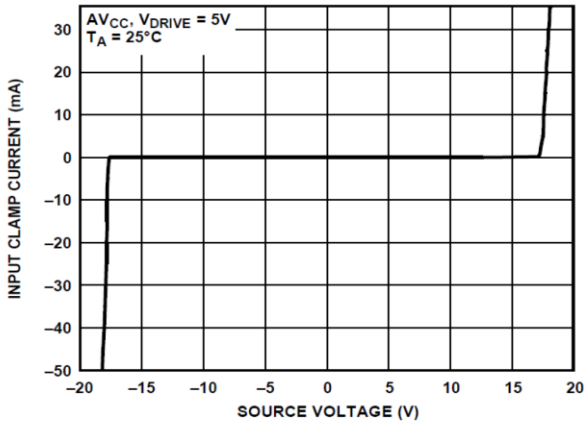


Figure — Input Protection Clamp Curve: Relationship Between Input Clamp Current and Source Voltage

Place a series resistor on the analog input channels to limit the current to ±10 mA for input voltages greater than +16 V and less than −16 V. In an application where there is a series resistance on an analog input channel, VxA or VxB, a corresponding resistance is required on the analog input ground channel, VxAGND or VxBGND (see Figure 43). If there is no corresponding resistor on the VxAGND or VxBGND channel, an offset error occurs on that channel. Use the input overvoltage clamp protection circuitry to protect the DAD7616 against transient overvoltage events. It is not recommended to leave the DAD7616 in a condition where the clamp protection circuitry is active in normal or power-down conditions for extended periods.

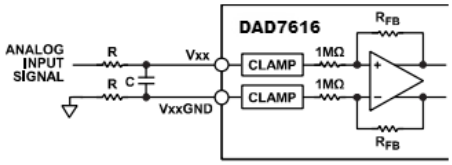


Figure 43. Input Resistance Matching on the Analog Input

Analog Input Antialiasing Filter

An analog antialiasing filter (a first-order Butterworth) is also provided on the DAD7616. Figure 44 and Figure 45 show the frequency and phase response, respectively, of the analog antialiasing filter. The typical corner frequency in the ±10 V range is 39 kHz, and 33 kHz in the ±5 V range.

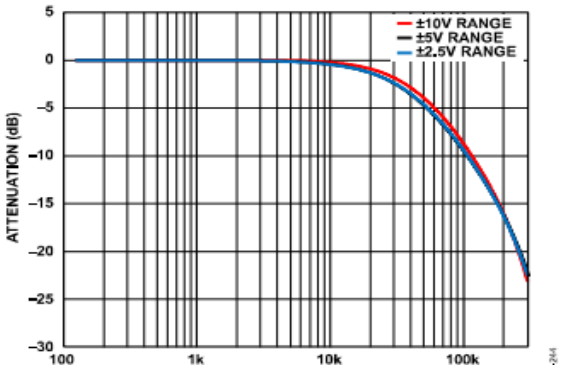


Figure 44. Analog Antialiasing Filter Frequency Response

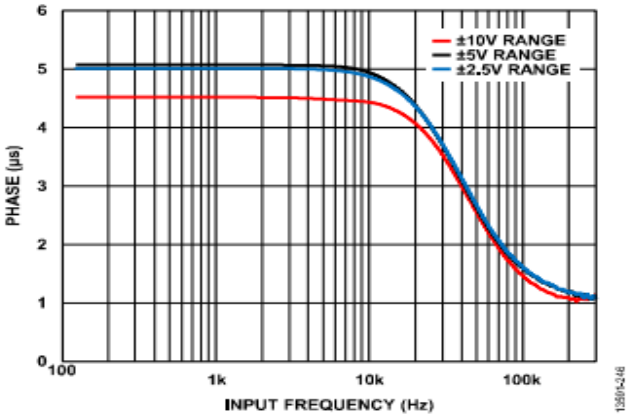
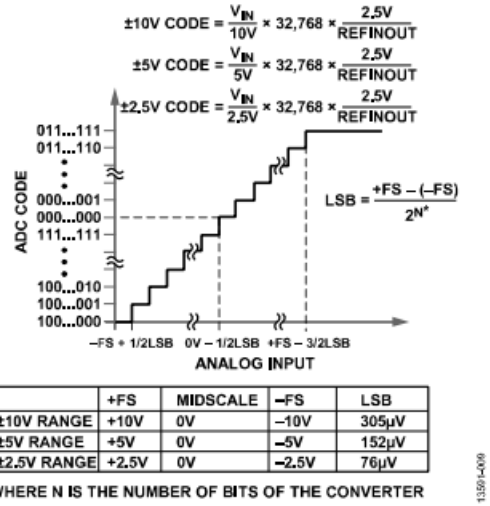


Figure 45. Analog Antialiasing Filter Phase Response



	+FS	MIDSCALE	–FS	LSB
±10V RANGE	+10V	0V	–10V	305µV
±5V RANGE	+5V	0V	–5V	152µV
±2.5V RANGE	+2.5V	0V	–2.5V	76µV

*WHERE N IS THE NUMBER OF BITS OF THE CONVERTER

Figure 46. Transfer Characteristics

ADC TRANSFER FUNCTION

The output coding of the DAD7616 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB and 3/2 LSB. The LSB size is full-scale range ÷ 65,536 for the DAD7616. The ideal transfer characteristics for the DAD7616 are shown in Figure 46. The LSB size is dependent on the analog input range selected.

INTERNAL/EXTERNAL REFERENCE

The DAD7616 can operate with either an internal or external reference. The device contains an on-chip 2.5 V band gap reference. The REFINOUT pin allows access to the 2.5 V reference that generates the on-chip 4.096 V reference internally, or it allows an external reference of 2.5 V to be applied to the DAD7616. An externally applied reference of 2.5 V is also amplified to 4.096 V using the internal buffer. This 4.096 V buffered reference is the reference used by the SAR ADC.

The REFSEL pin is a logic input pin that allows the user to select between the internal reference and an external reference. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFINOUT pin.

The internal reference buffer is always enabled. After a full reset, the DAD7616 operates in the reference mode selected by the REFSEL pin. Decoupling is required on the REFINOUT pin for both the internal and external reference options. A 100 nF, X8R ceramic capacitor is required on the REFINOUT pin to REFINOUTGND.

The DAD7616 contains a reference buffer configured to amplify the reference voltage to ~4.096 V. A 10 µF, X5R ceramic capacitor is required between REFCAP and REFGND. The reference voltage available at the REFINOUT pin is 2.5 V. When the DAD7616 is configured in external reference mode, the REFINOUT pin is a high input impedance pin. If the internal reference is to be applied elsewhere within the system, it must first be buffered externally.

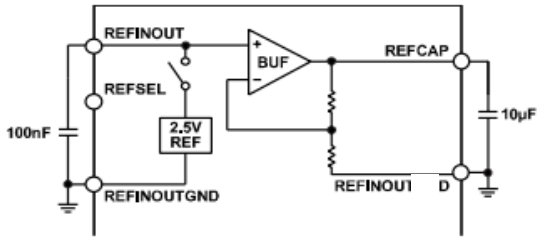


Figure. Reference Circuitry

SHUTDOWN MODE

The DAD7616 enters shutdown mode by keeping the RESET pin low for greater than 1.2 µs. When the RESET pin is set from low to high, the device exits shutdown mode and enters normal mode.

When the DAD7616 is placed in shutdown mode, the current consumption is typically 78 µA and the power-up time to perform a write to the device is approximately 240 µs. Power-up time to perform a conversion is 15 ms. In shutdown mode, all circuitry is powered down and all registers are cleared and reset to their default values.

DIGITAL FILTER

The DAD7616 contains an optional digital first-order sinc filter for use in applications where slower throughput rates are in use or where higher SNR or dynamic range is desirable. The OSR of the digital filter is controlled in hardware using the oversampling pins, OS2 to OS0 (OSx), or in software via the OS bits within the configuration register. In software mode, oversampling is enabled for all channels after the OS bits are set in the configuration register. In hardware mode, the OSx signals at the time a full reset is released determine the OSR to be used. Below table provides the oversampling bit decoding to select the different oversample rates. In addition to the oversampling function, the output result is decimated to 16-bit resolution.

If the OSx pins/OS bits are set to select an OS ratio of eight, the next CONVST rising edge takes the first sample for the selected channel, and the remaining seven samples for that channel are taken with an internally generated sampling signal. These samples are then averaged to yield an improvement in SNR performance. As the OS ratio increases, the −3 dB frequency is reduced, and the allowed sampling frequency is also reduced. The conversion time extends as the oversampling rate is increased, and the BUSY signal scales with oversampling rates. Acquisition and conversion time increase linearly with oversampling ratio.

If oversampling is enabled with the sequencer or in burst mode, the extra samples are gathered for a given channel before the sequencer moves on to the next channel.

Below table shows the typical SNR performance of the device for each permissible oversampling ratio. The input tone used was a 100 Hz sine wave for the three input ranges of the device. A plot of SNR vs. OSR is shown in Figure 48.

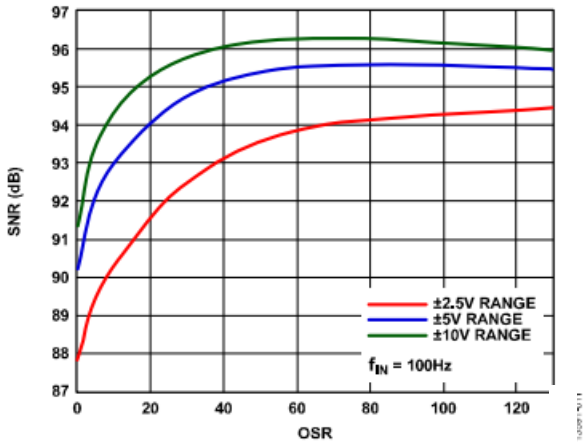


Figure 48. Typical SNR vs. OSR for all Analog Input Ranges

Table. Oversampling Bit Decoding

OSx Pins/OS Bits	OSR	Typical SNR (dB)			−3 dB Bandwidth (kHz)
		±2.5 V Range	±5 V Range	±10 V Range	All Ranges
000	No oversampling	86.8	88.7	90.5	37
001	2	87.1	89.6	91.1	36.5
010	4	88	90.6	92.2	35
011	8	88.9	91.6	93.2	30.5
100	16	90	92.6	94.2	22
101	32	91.6	93.8	95.1	13.2
110	64	92.9	94.5	95.4	7.2
111	128	93.4	94.4	95.1	3.6

APPLICATIONS INFORMATION

FUNCTIONALITY OVERVIEW

The DAD7616 has two main modes of operation: hardware mode and software mode. Additionally, the communications interface for hardware or software mode can be serial or parallel. Depending on the mode of operation and interface chosen, certain functionality may not be available. Full functionality is available in both software serial and software parallel mode with restricted functionality in hardware serial mode and hardware parallel mode. Table 10 shows the functionality available in the different modes of operation.

POWER SUPPLIES

The DAD7616 has two independent power supplies, V_{CC} and V_{DRIVE}, that supply the analog circuitry and digital interface,respectively. Decouple both the V_{CC} supply and the V_{DRIVE} supply with a 10 µF capacitor in parallel with a 100 nF capacitor. Additionally, these supplies are regulated by two internal LDO regulators. The analog LDO (ALDO) typically supplies 4.5 V. Decouple the ALDO with a 10 µF capacitor between the REGCAP and REGCAPGND pins. The digital LDO (DLDO) typically supplies 2.6 V. Decouple the DLDO with a 10 µF capacitor between the REGCAPD and REGCAPDGND pins.

POWER-ON TIME REQUIREMENT

The DAD7616 is robust to power supply sequencing. The recommended sequence is to power up V_{DRIVE} first, followed by V_{CC}. Hold RESET

low until both supplies are stabilized.

TYPICAL CONNECTIONS

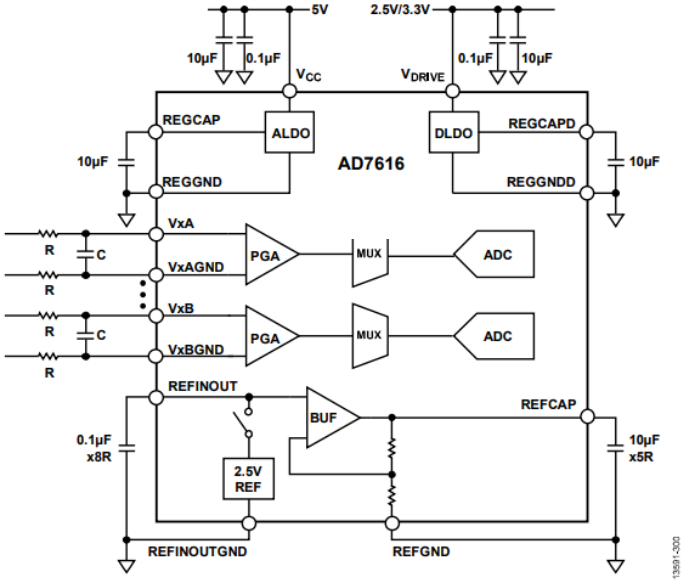
The typical connection figure shows typical connections required for the normal operation of DAD7616. Decouple the V_{CC} and V_{DRIVE} supplies as shown in Figure. Place the smaller, 0.1 µF capacitor as close to the supply pin as possible, with the larger 10 µF bulk capacitor in parallel. Decouple the reference and LDO regulators as shown in Figure and as described in Table 10.

The analog input pins require a matched resistance, R, on both the VxA and VxAGND (similarly, VxB and VxBGND) inputs to avoid a gain error on the analog input channels caused by an impedance mismatch.

Table 10. Functionality Matrix

1 "Yes" means available; "No" means not available.

Functionality	Operation Mode1			
	Software Mode, HW_RNGSELx = 00		Hardware Mode, HW_RNGSELx ≠ 00	
	Serial, SER/PAR = 1	Parallel, SER/PAR = 0	Serial, SER/PAR = 1	Parallel, SER/PAR = 0
Internal/External Reference	Yes	Yes	Yes	Yes
Selectable Analog Input Ranges				
Individual Channel Configuration	Yes	Yes	No	No
Common Channel Configuration	No	No	Yes	Yes
Sequential Sequencer	Yes	Yes	Yes	Yes
Fully Configurable Sequencer	Yes	Yes	No	No
Burst Mode	Yes	Yes	Yes	Yes
On-Chip Oversampling	Yes	Yes	Yes	No
CRC	Yes	Yes	Yes	No
Diagnostic Channel Conversion	Yes	Yes	No	No
Hardware Reset	Yes	Yes	Yes	Yes
Serial 1-Wire Mode	Yes	No	Yes	No
Serial 2-Wire Mode	Yes	No	Yes	No
Register Access	Yes	Yes	No	No



Typical External Connections

DEVICE CONFIGURATION

OPERATIONAL MODE

The mode of operation, hardware mode or software mode, is configured when the DAD7616 is released from full reset. The logic level of the HW_RNGSELx pins when the RESET pin transitions from low to high determines the operational mode. The HW_RNGSELx pins are dual function. If HW_RNGSELx = 0b00, the DAD7616 enters software mode. Any other combination of the HW_RNGSELx configures the DAD7616 to hardware mode and the analog input range is configured as per Table 8. After software mode is configured, the logic level of the HW_RNGSELx signals is ignored. After an operational mode is configured, a full reset via the RESET pin is required to exit the operational mode and to set up an alternative mode. If hardware mode is selected, all further device configuration is via pin control. Access to the on-chip registers is prohibited in hardware mode. In software mode, the interface and reference configuration must be configured via pin control but all further device configuration is via register access only.

INTERNAL/EXTERNAL REFERENCE

The internal reference is enabled or disabled when the DAD7616 is released from a full reset. The logic level of the REFSEL signal when the RESET pin transitions from low to high configures the reference. After the reference is configured, changes to the logic level of the REFSEL signal are ignored. If the REFSEL signal is set to 1, the internal reference is enabled. If REFSEL is set to Logic 0, the internal reference is disabled and an external reference must be supplied to the REFINOUT pin for correct operation of the DAD7616. A full reset via the RESET pin is required to exit the operational mode and set up an alternative mode. Connect a 100 nF capacitor between the REFINOUT and REFINOUTGND pins. If using an external reference, place a 10 kΩ band limiting resistor in series between the reference and the REFINOUT pin of the DAD7616.

DIGITAL INTERFACE

The digital interface selection, parallel or serial, is configured when the DAD7616 is released from a full reset. The logic level of the SER/PAR signal when the RESET pin transitions from low to high configures the interface. If the SER/PAR signal is set to 0, the parallel interface is enabled. If the SER/PAR signal is set to 1,the serial interface is selected. Additionally, if the serial interface is selected, the SER1W signal is monitored when the RESET pin is released to determine if serial 1-wire or 2-wire mode is selected. After the interface is configured, changes to the logic level of the SER/PAR signal or the SER1W signal (when the serial interface is enabled) are ignored. A full reset via the RESET pin is required to exit the operation mode and set up an alternative mode.

HARDWARE MODE

If hardware mode is selected, the available functionality is restricted and all functionality is configured via pin control. The logic level of the following signals is checked after a full reset to configure the functionality of the DAD7616: CRC, BURST, SEQEN, and OSx. Table 11 provides a summary of the signals that are latched by the device on the release of a full reset, depending on the mode of operation chosen. After the device is configured, a full reset via the RESET pin is required to exit the configuration and set up an alternative configuration. Functionality availability is restricted depending on the interface type selected. See Table 10 for a full list of the functionality available in hardware parallel or serial mode. The CHSELx pins are queried at reset to determine the initial analog input channel pair to acquire for conversion or to configure the initial settings for the sequencer. The channel pair selected for conversion or the hardware sequencer can be reconfigured during normal operation by setting and maintaining the CHSELx signal level before the CONVST rising edge until the BUSY falling edge.

The HW_RNGSELx signals control the analog input range for all 16 analog input channels. A logic change on these pins has an immediate effect on the analog input range; however, the typical settling time is approximately 120 µs, in addition to the normal acquisition time requirement. The recommended practice is to hardwire the range select pins according to the desired input range for the system signals. Access to the on-chip registers is prohibited in hardware mode.

Table. Summary of Latched Hardware Signals

Signal	Latched at Full Reset		Read at Reset		Read During Busy		Edge Driven	
	HW Mode	SW Mode	HW Mode	SW Mode	HW Mode	SW Mode	HW Mode	SW Mode
REFSEL	Yes	Yes						
SEQEN	Yes	No	Yes	Yes			Yes	No
HW_RNGSELx (Range Change)								
HW_RNGSELx (HW or SW Mode)	Yes	Yes						
SER/PAR								
CRCEN	Yes	Yes						
OSx	Yes	No						
BURST	Yes	No						
CHSELx	Yes	No	Yes	No	Yes	No		
SER1W	Yes	Yes						

Blank cells in Table mean not applicable.

SOFTWARE MODE

If software mode is selected and the reference and interface type is configured, all other configuration settings in the DAD7616 are controlled via the on-chip registers. All functionality of the DAD7616 is available when software mode is selected. Table 11 provides a summary of the signals that are latched by the device on the release of a full reset, depending on the mode of operation chosen.

RESET FUNCTIONALITY

The DAD7616 has two reset modes: full or partial. The reset mode selected is dependent on the length of the reset low pulse. A partial reset requires the RESET pin to be held low between 150 ns and 500 ns. After 50 ns from release of RESET, the device is fully functional and a conversion can be initiated. A full reset requires the RESET pin to be held low for a minimum of 1.2 µs.

After 15 ms from release of RESET, the devices is completely reconfigured and a conversion can be initiated.A partial reset re-initializes the following modules:

- Sequencer
- Digital filter
- SPI
- Both SAR ADCs

The current conversion result is discarded on completion of a partial reset. The partial reset does not affect the register values programmed in software mode or the latches that store the user configuration in both hardware and software modes. A dummy conversion is required in software mode after a partial reset.

A full reset returns the device to its default power-on state. The following features are configured when the DAD7616 is released from full reset:

- Hardware mode or software mode
- Internal/external reference
- Interface type

On power-up, the RESET signal can be released as soon as both the V_{CC} and V_{DRIVE} supplies are stable. The logic level of the HW_RNGSELx, REFSEL, SER/PAR and DB4/SER1W pins when the RESET pin is released after a full reset determines the configuration.

If hardware mode is selected, the functionality determined by the CRC, BURSTEN, SEQEN, and OSx signals is also latched when the RESET pin transitions from low to high in full resetmode. After the functionality is configured, changes to these signals are ignored. In hardware mode, the analog input range (HW_RNGSELx signals) can be configured during either a full or partial reset or during normal operation, but hardware/software mode selection requires a full reset to reconfigure while this setting is latched.

In hardware mode, the CHSELx and HW_RNGSELx pins are queried at release from both a full and a partial reset to perform the following actions:

- Determine the initial analog input channel pair to acquire for conversion.
- Configure the initial settings for the sequencer.
- Select the analog input voltage range.

The CHSELx and HW_RNGSELx signals are not latched. The channel pair selected for conversion, or the hardware sequencer, can be reconfigured during normal operation by setting and maintaining the CHSELx signal level before the CONVST rising edge, and ensuring the signal level remains constant until after BUSY transitions low again. See the Channel Selection section for further details.

In software mode, all additional functionality is configured by controlling the on-chip registers.

PIN FUNCTION OVERVIEW

There are several dual function pins on the DAD7616. Their functionality is dependent on the mode of operation selected by the HW_RNGSELx pins. Table 12 outlines the pin functionality in the different modes of operation and interface modes.

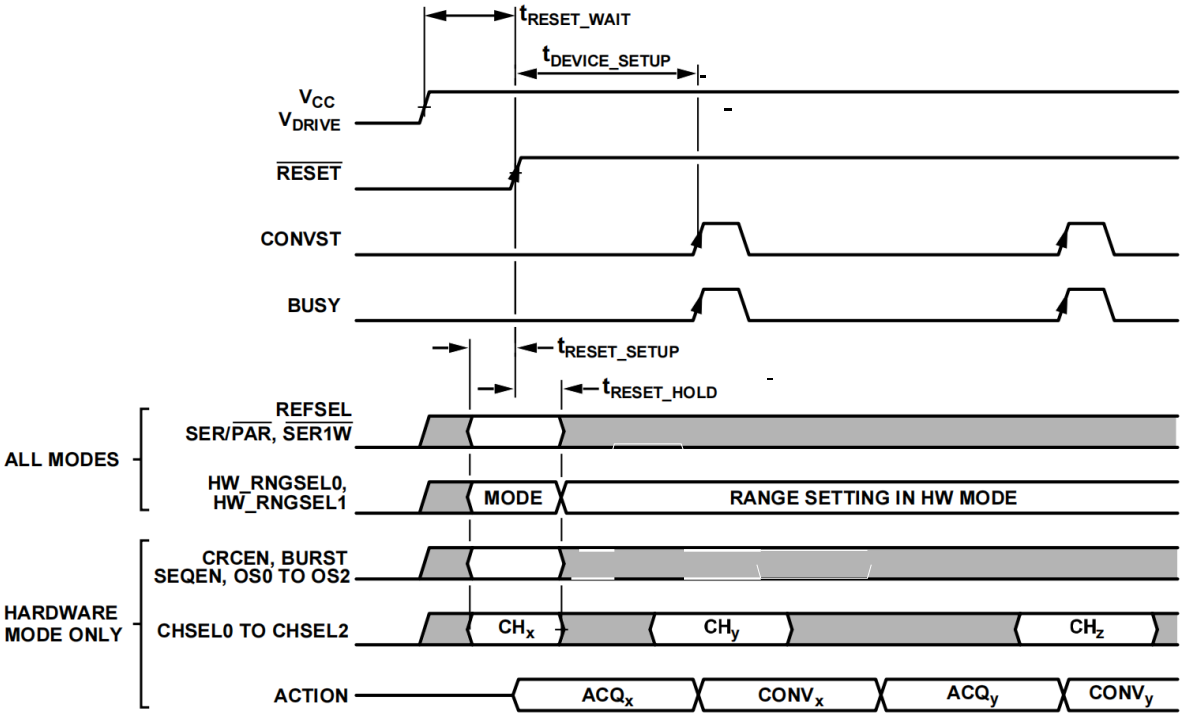


Figure 50. DAD7616 Configuration at Reset

Table 12. Pin Functionality Overview

	Operation Mode			
	Software, HW_RNGSELx = 00		Hardware, HW_RNGSELx ≠ 00	
Pins	Serial, SER/$\overline{PAR}$ = 1	Parallel, SER/$\overline{PAR}$ = 0	Serial, SER/$\overline{PAR}$ = 1	Parallel, SER/$\overline{PAR}$ = 0
CHSELx	No function, connect to DGND	No function, connect to DGND	CHSELx	CHSELx
SCLK/$\overline{RD}$	SCLK	$\overline{RD}$	SCLK	$\overline{RD}$
$\overline{WR}$/BURST	Connect to DGND	$\overline{WR}$	BURST	BURST
DB15/OS0 to DB13/OS2	Connect to DGND	DB15 to DB13	OSx	DB15 to DB13
DB12/SDOA	SDOA	DB12	SDOA	DB12
DB11/SDOB	SDOB, leave floating for serial 1-wire mode	DB11	SDOB	DB11
DB10/SDI	SDI	DB10	Connect to DGND	DB10
DB9 to DB6, DB3 to DB0	Connect to DGND	DB9 to DB6, DB3 to DB0	Connect to DGND	DB9 to DB6, DB3 to DB0
DB5/CRCEN	Connect to DGND	DB5	CRCEN	DB5
DB4/$\overline{SER1W}$	$\overline{SER1W}$	DB4	$\overline{SER1W}$	DB4
HW_RNGSELx	HW_RNGSELx, connect to DGND	HW_RNGSELx, connect to DGND	HW_RNGSELx, configure analog input range	HW_RNGSELx, configure analog input range
SEQEN	No function, connect to DGND	No function, connect to DGND	SEQEN	SEQEN
REFSEL	REFSEL	REFSEL	REFSEL	REFSEL

DIGITAL INTERFACE

CHANNEL SELECTION

Hardware Mode

The logic level of the CHSELx signals determine the channel pair for conversion; see Table 13 for signal decoding information. The CHSELx signals at the time that either full or partial reset is released determine the initial channel pair to sample. After a reset, the logic levels of the CHSELx signals are examined during the BUSY high period to set the channel pair for the next conversion. The CHSELx signal level must be set before CONVST goes from low to high and be maintained until BUSY goes from high to low to indicate a conversion is complete. See Figure 51 for further details.

Software Mode

In software mode, the channels for conversion are selected by control of the channel register. On power-up or after a reset, the default channels selected for conversion are Channel V0A and Channel V0B.

Table 13. CHSELx Pin Decoding

Channel Selection Input Pin			Analog Input Channels for Conversion
CHSEL2	CHSEL1	CHSEL0	
0	0	0	V0A, V0B
0	0	1	V1A, V1B
0	1	0	V2A, V2B
0	1	1	V3A, V3B
1	0	0	V4A, V4B
1	0	1	V5A, V5B
1	1	0	V6A, V6B
1	1	1	V7A, V7B

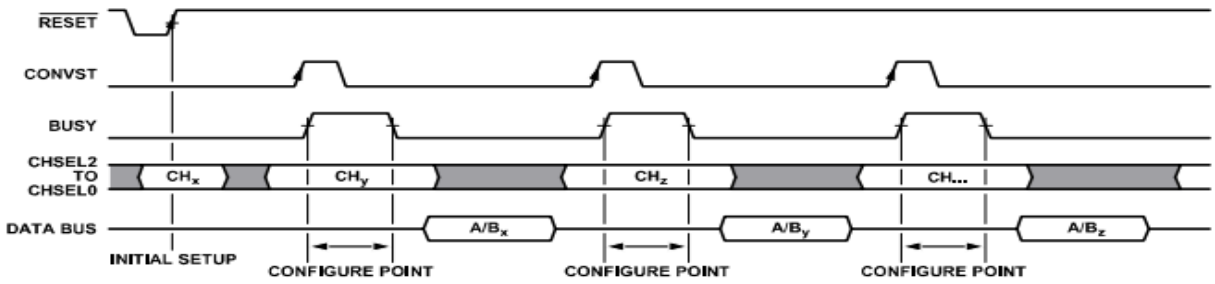


Figure. Hardware Mode Channel Conversion Setting

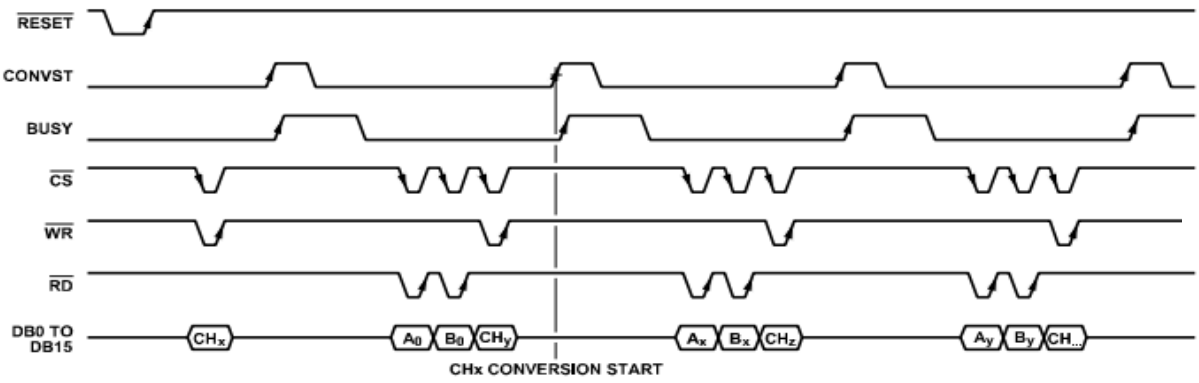


Figure. Software Serial Mode Channel Conversion Setting

PARALLEL INTERFACE

The parallel interface reads the conversion results, and configures and reads back the on-chip registers. Data can be read from the DAD7616 via the parallel data bus with standard CS, RD, and WR signals. To read the data over the parallel bus, tie the SER/PAR pin low.

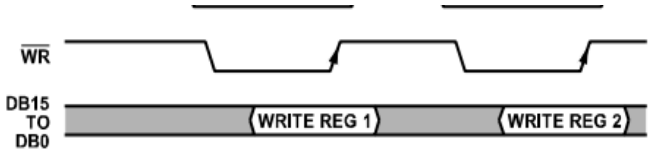


Figure. Parallel Interface Register Write

Reading Conversion Results

The CONVST signal initiates the conversion process. A low to high transition on the CONVST signal initiates a conversion of the selected inputs. The BUSY signal goes high to indicate a conversion is in progress. When the BUSY signal transitions from high to low to indicate that a conversion is complete, it is possible to read back conversion results on the parallel interface.

Data can be read from the DAD7616 via the parallel data bus with standard CS and RD signals. The CS and RD input signals are internally gated to enable the conversion result onto the data bus. When the CSb is in a logic low level state, the data lines DB15 to DB0 are out of the high-impedance state.
The rising edge of the CSb input signal three-states the bus, and the falling edge of the CSb input signal takes the bus out of the high impedance state. CS is the control signal that enables the data lines; it is the function that allows multiple DAD7616 devices to share the same parallel data bus.

The number of required read operations depends on the device configuration. A minimum of two reads are required to read the conversion result for the simultaneously sampled A and B channels. If additional functions such as CRC, status, and burst mode are enabled, the number of required readbacks increases accordingly.
The RDb pin reads data from the output conversion results register. Applying a sequence of RDb pulses to the RDb pin of the DAD7616 clocks the conversion results out from each channel onto the parallel bus, DB15 to DB0. The first RDb falling edge after BUSY goes low clocks out the conversion result from Channel AX. The next RDb falling edge updates the bus with the Channel BX conversion result.

Writing Register Data

In software mode, all the read/write registers in the DAD7616 can be written to over the parallel interface. A register write command is performed by a single 16-bit parallel access via the parallel bus (DB15 to DB0), CS, and WR signals. Provide data written to the DAD7616 on the DB15 to DB0 inputs, with DB0 being the LSB of the data-word. The format for a write command is shown in Figure. Bit D15 must be set to 1 to select a write command. Bits[D14:D9] contain the register address. The subsequent nine bits (Bits[D8:D0]) contain the data to be written to the selected register. See the Register Summary section for the complete list of register addresses. Data is latched into the device on the rising edge of WR.

Reading Register Data

All the registers in the device can be read over the parallel interface. A register read is performed by first writing the address of the register to be read to the DAD7616. The format for a register read command is shown in Figure. Bit D15 must be set to 0 to select a read command. Bits[D14:D9] contain the register address. The subsequent nine bits (Bits[D8:D0]) are ignored. The read command is latched into the DAD7616 on the rising edge of WR.

This latch transfers the relevant register data to the output register. The register data can then be read on the DB15 to DB0 pins by using a standard read command. See Below Figure for additional information.

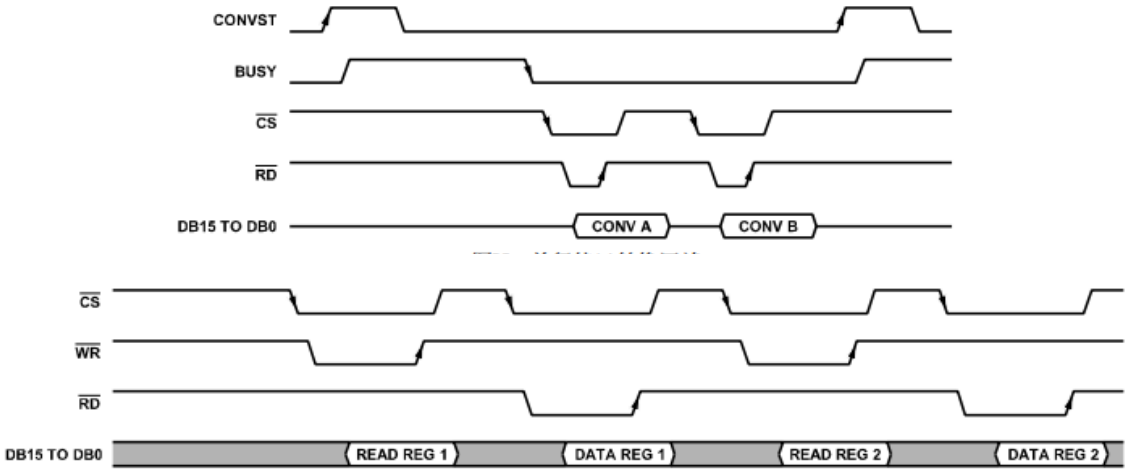


Figure 56. Parallel Interface Register Read

SERIAL INTERFACE

To interface to the DAD7616 over the SPI, the SER/PAR pin must be tied high. The CSb and SCLK signals transfer data from the DAD7616. The DAD7616 has two serial data output pins, SDOA and SDOB. Data is read back from the DAD7616 using serial 1-wire or serial 2-wire mode. In serial 2-wire mode for the DAD7616, conversion results from Channel V0A to Channel V7A appear on SDOA, and conversion results from Channel V0B to Channel V7B appear on SDOB. In serial 1-wire mode, conversion results from Channel V0B to Channel V7B are interlaced with conversion results from Channel V0A to Channel V7A. To achieve the maximum throughput, it is required to use 2-wire mode.

To read back data over both SDOA and SDOB, the SER1W pin must be tied high. If data is to be read back over SDOA only, the SER1Wb pin must be tied low. Serial 1-wire or 2-wire mode is configured when the DAD7616 is released from full reset.

Reading Conversion Results

The CONVST signal initiates the conversion process. A low to high transition on the CONVST signal initiates a conversion of the selected inputs. The BUSY signal goes high to indicate a conversion is in progress. When the BUSY signal transitions from high to low to indicate that a conversion is complete, it is possible to read back conversion results on the serial interface.

The CSb falling edge takes the data output lines, SDO and SDOB, out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs, SDOA and SDOB. Below Figure shows a read of two simultaneous conversion results using two SDOx lines on the DAD7616. If the status register is appended to the conversion results or operating in sequencer burst mode where multiples of 16 SCLK transfers access data from the DAD7616, hold CS low to frame the entire data. Data can also be clocked out using just one SDOx line, in which case SDOA must be used to access all conversion data. For the DAD7616 to access both Channel VxA and Channel VxB conversion results on one SDOx line, a total of 32 SCLK cycles is required. Frame these 32 SCLK cycles using one CS signal, or individually frame each group of 16 SCLK cycles using the CS signal.

The disadvantage of using just one SDOx line is that the throughput rate is reduced. Leave the unused SDOB line unconnected in serial 1-wire mode. If using SDOA as a single serial data output line, the channel results are output in the following order: VxA and VxB. Below Figure shows a 1-wire, serial readback operation.

The speed at which the data can be read back in serial interface mode is dependent on SPI frequency, V_{DRIVE} supply, and the capacitance of the load on the SDO line, C_{LOAD}. Table 14 shows a summary of the maximum speed achievable for various conditions.

Table 14. SPI Frequency vs. Load Capacitance and V_{DRIVE}

V_{DRIVE} (V)	C_{LOAD} (pF)	SPI Frequency (MHz)
2.3 to 3	20	30
3 to 5.5	30	35

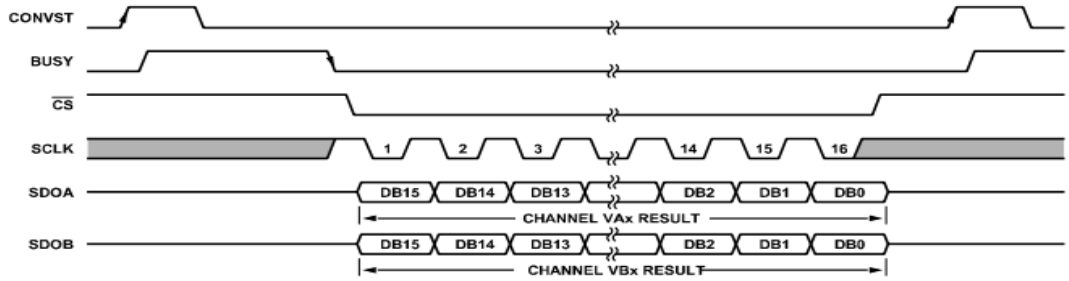


Figure. Serial Interface, 2-Wire Mode

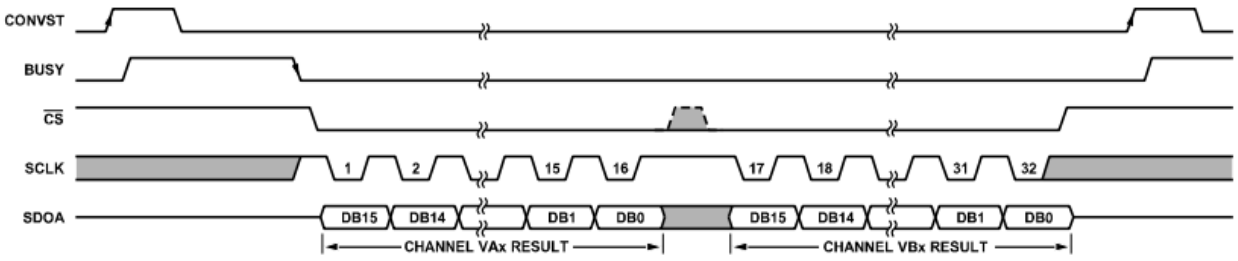


Figure. Serial Interface, 1-Wire Mode

Writing Register Data

All the read/write registers in the DAD7616 can be written to over the serial interface. A register write command is performed by a single 16-bit SPI access. The format for a write command is shown in Table. Bit D15 must be set to 1 to select a write command. Bits[D14:D9] contain the register address. The subsequent nine bits (Bits[D8:D0]) contain the data to be written to the selected register. Below Figure shows a typical serial write command.

Reading Register Data

All the registers in the device can be read over the serial interface. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or no operation (NOP). The format for a read command is shown in Table. Bit D15 must be set to 0 to select a read command. Bits[D14:D9] contain the register address. The subsequent nine bits (Bits[D8:D0]) are ignored. See the Register Summary section for the complete list of register addresses. Below Figure shows a typical serial read command.

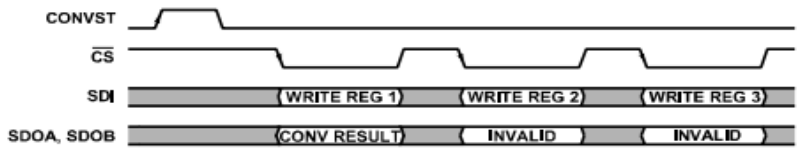


Figure. Serial Interface Register Write

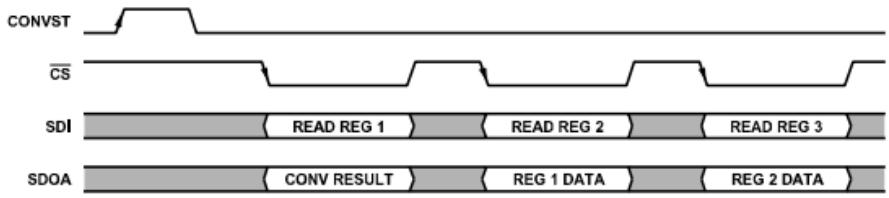


Figure. Serial Interface Register Read

Table. Write Command Message Configuration

MSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W/R	REGADDR[5:0]						Data [8:0]								
1	Register address						Data to write								

Table. Read Command Message Configuration

MSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W/R	REGADDR[5:0]						Data [8:0]								
0	Register address						Do not care								

SEQUENCER

The DAD7616 features a highly configurable on-chip sequencer. The functionality and configuration of the sequencer is dependent on the mode of operation of the DAD7616.

In hardware mode, the sequencer is sequential only. The sequencer always starts converting at Channel V0A and Channel V0B and converts each subsequent channel up to the configured end channel.

In software mode, the sequencer has additional functionality and configurability. The sequencer stack has 16 uniquely configurable sequence steps, allowing any channel order to be programmed. Additionally, any Channel VxA input can be paired with any Channel VxB input or diagnostic channe

The sequencer can be operated with or without the burst function enabled. With the burst function enabled, only one CONVST pulse is required to convert every channel in a sequence. With burst mode disabled, one CONVST pulse is required for every conversion step in the sequence. See the Burst Sequencer section for additional details on operating in burst mode.

HARDWARE MODE SEQUENCER

In hardware mode, the sequencer is controlled by the SEQEN pin and the CHSELx pins. The sequencer is enabled or disabled when the DAD7616 is released from full reset. The logic level of the SEQEN pin when the RESET pin is released determines whether the sequencer is enabled or disabled. After the RESET pin is released, the function is fixed and a full reset via the RESET pin is required to exit the function and set up an alternative configuration.

Table. Hardware Mode Sequencer Configuration

SEQEN	Interface Mode
0	Sequencer disabled
1	Sequencer enabled

When the sequencer is enabled, the logic levels of the CHSELx pins determine the channels selected for conversion in the sequence. The CHSELx pins at the time RESET is released determine the initial settings for the channels to convert in the sequence. To reconfigure the channels selected for conversion thereafter, set the CHSELx pins to the required setting for the duration of the final BUSY pulse before the current conversion sequence is complete. See Below Figure for further details.

Table. CHSELx Pin Decoding Sequencer

Channel Selection Input Pin			Analog Input Channels for Sequential Conversion
CHSEL0	CHSEL1	CHSEL2	
0	0	0	V0x only
0	0	1	V0x to V1x
0	1	0	V0x to V2x
0	1	1	V0x to V3x
1	0	0	V0x to V4x
1	0	1	V0x to V5x
1	1	0	V0x to V6x
1	1	1	V0x to V7x

SOFTWARE MODE SEQUENCER

In software mode, the DAD7616 contains a 16-layer fully configurable sequencer stack. Control of the sequencer is achieved by programming the configuration register and sequencer stack registers via the parallel or serial interface. Each stack step can be individually programmed to pair any input from Channel VxA to any input from Channel VxB, or any diagnostic channel can be selected for conversion. The sequencer depth can be set to any length from 1 to 16 layers. The sequencer depth is controlled via the SSRENx bit. Set the SSRENx bit in the sequencer stack register corresponding to the last step required. The channels to convert are selected by programming the ASELx and BSELx bits in each sequence stack register for the depth required.

The sequencer is activated by setting the SEQEN bit in the configuration register to 1.

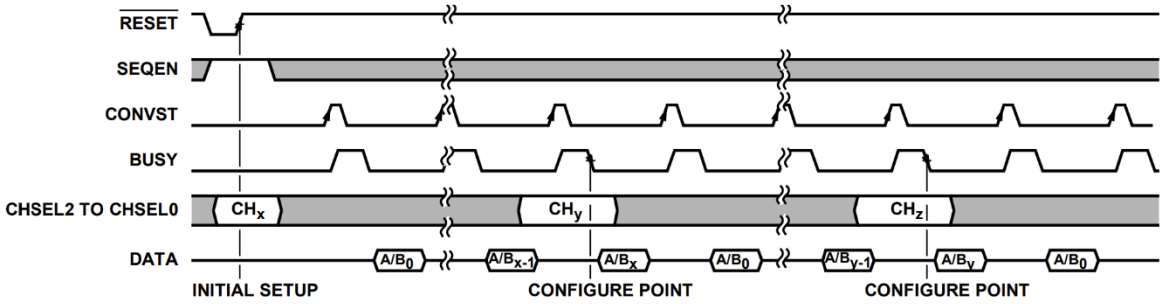


Figure. Hardware Mode Sequencer Configuration

To configure and enable the sequencer, it is recommended to complete the following procedure (see Below Figure):

1. Configure the analog input range for the required analog input channels.
2. Program the sequencer stack registers to select the channels for the sequence.
3. The position 1 of the SSRENx in the last sequence step required.
4. Set the SEQEN bit in the configuration register to position 1.
5. Provide a dummy CONVST pulse.
6. Cycle through CONVST pulses and conversion reads to step through each element of the sequencer stack.

The sequence automatically restarts from the first element in the sequencer stack with the next CONVST pulse.

Following a partial reset, the sequencer pointer is repositioned to the first layer of the stack, but the register programmed values remain unchanged.

BURST SEQUENCER

Burst mode avoids generating a CONVST pulse for each step in a sequence of conversions. One CONVST pulse converts every step in the sequence.

The burst sequencer is an additional feature that works in conjunction with the sequencer. If the burst function is enabled, one CONVST pulse initiates a conversion of all the channels configured in the sequencer. The burst function avoids generating a CONVST pulse for each step in a sequence of conversions, as is the case when the burst function is disabled.

Configuration of the burst function varies depending on the mode of operation: hardware or software mode. See the Hardware Mode Burst section and the Software Mode Burst section for specific details on configuring the burst function in the each mode.

When configured, the burst sequence is initiated at the rising edge of CONVST. The BUSY pin goes high to indicate that a conversion is in progress. The BUSY pin remain highs until all conversions in the sequence are complete. The conversion results are available for readback after the BUSY pin goes low. The number of data reads required to read all the data in the burst sequence is dependent on the length of the sequence configured.

The conversion results are presented on the data bus (parallel or serial) in the same order as the programmed sequence. The throughput rate of the DAD7616 is limited in burst mode and dependent on the length of the sequence. Each channel pair requires an acquisition, conversion, and readback time. The time taken to complete a sequence with number of channel pairs, N, is estimated by

$$t_{BURST} = (t_{CONV} + 25\ ns) + (N - 1)(t_{ACQ} + t_{CONV}) + N(t_{RB})$$

where:

tCONV is the typical conversion time.

tACQ is typical acquisition time.

tRB is the time required to read back the conversion results in either serial 1-wire, serial 2-wire, or parallel mode.

Hardware Mode Burst

Burst mode is enabled in hardware mode by setting the BURST pin to 1. The SEQEN pin must also be set to 1 to enable the sequencer. In hardware mode, the burst sequencer is controlled by the BURST, SEQEN, and CHSELx pins. The burst sequencer is enabled or disabled when the DAD7616 is released from full reset. The logic level of the SEQEN pin and the BURST pin when the RESET pin is released determines whether the burst sequencer is enabled or disabled. After the RESET pin is released, the function is fixed and a full reset via the RESET pin is required to exit the function and set up an alternative configuration.

When the burst sequencer is enabled, the logic levels of the CHSELx pins determine the channels selected for conversion in the burst sequence. The CHSELx pins at the time RESET is released determines the initial settings for the channels to convert in the burst sequence. To reconfigure the channels selected for conversion after a reset, set the CHSELx pins to the required setting for the duration of the next BUSY pulse (see Figure 63 for further details).

Software Mode Burst

In software mode, the burst function is enabled by setting the BURST bit in the configuration register to 1. This action must be performed when setting the SEQEN bit in the configuration register as outlined in the steps described in the Software Mode Sequencer section to configure the sequencer (see Below Figure for additional information)

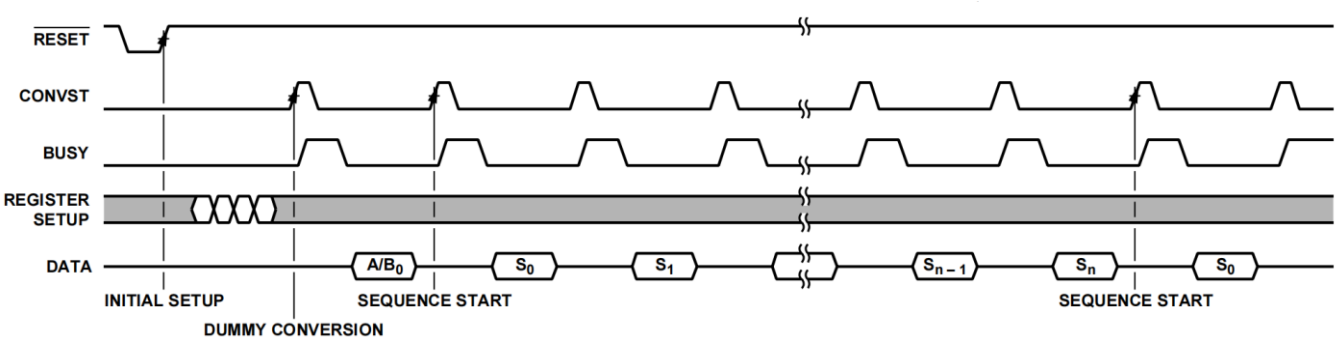


Figure. Software Mode Sequencer Configuration

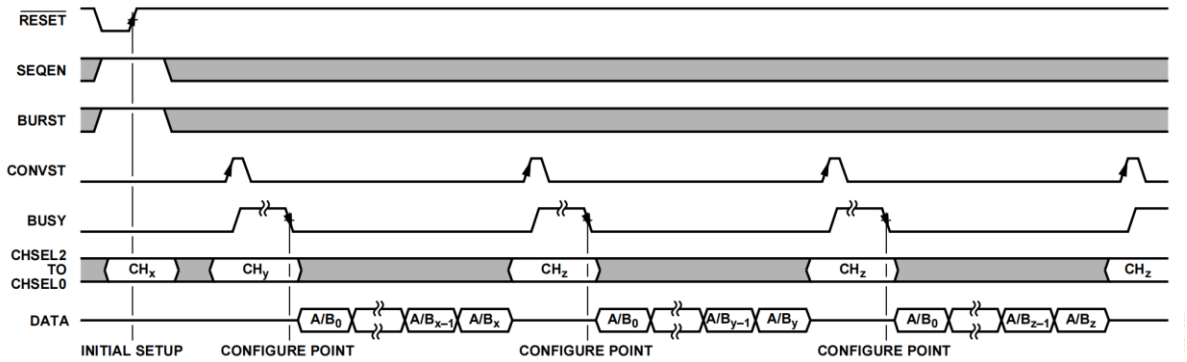


Figure. BURST Sequencer, Hardware Mode

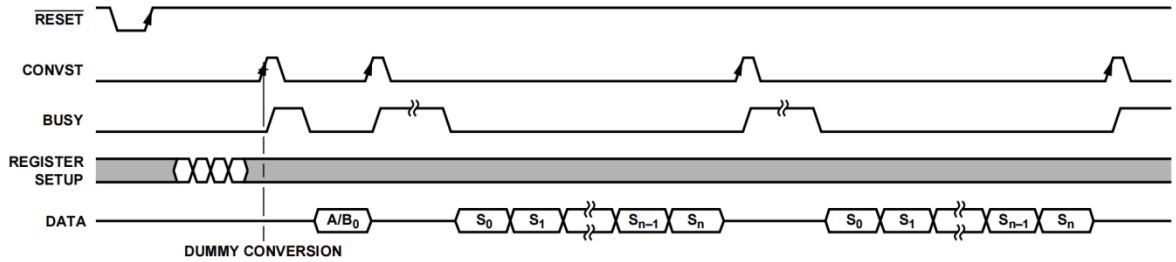


Figure. BURST Sequencer, Software Mod

DIAGNOSTICS

DIAGNOSTIC CHANNELS

In addition to the 16 analog inputs, VxA and VxB, the DAD7616 can also convert the following diagnostic channels: VCC (The typical value is 5V) and the analog ALDO voltage (The typical value is 2.6V). The diagnostic channels are selected for conversion by programming the channel register (see the Channel Register section) to the corresponding channel identifier. In software mode, diagnostic channels can also be added to the sequencer stack, but to obtain accurate readings, the throughput rate must be less than 250 kSPS. The expected output of each channel is determined by the following transfer function (represented by signed decimal output): In the formula, VREF refers to the voltage on the REFCAP pin, and its typical value is 4.096 V.

$$Vcc(code) = \frac{Vcc*0.557}{Vref} * 32768$$

$$Valdo(code) = -\frac{Valdo*0.37}{Vref} * 3276$$

INTERFACE SELF TEST

It is possible to test the integrity of the digital interface by selecting the communication self test channel in the channel register (see the Channel Register section). Selecting the communication self test for conversion forces the conversion result register to a known fixed output. When conversion code is read, Code 0xAAAA is output as the conversion code of ADC A, and Code 0x5555 is output as the conversion code of ADC B.

CRC

The DAD7616 has a cyclic redundancy check (CRC) checksum mode to improve interface robustness by detecting errors in data. The CRC feature is available in both software (serial and parallel) mode and hardware (serial only) mode. The CRC feature is not available in hardware parallel mode. The CRC result is contained within the status register. Enabling the CRC feature enables the status register and vice versa.

In hardware mode, the CRCEN pin controls the CRC feature. The CRC feature is enabled or disabled when the DAD7616 is released from full reset. The logic level of the CRCEN pin when the RESET pin is released determines whether the CRC feature is enabled or disabled. Set the CRCEN pin to 1 to enable the CRC feature. After the RESET pin is released, the function is fixed and a full reset via the RESET pin is required to exit the function and set up an alternative configuration. See the Reset Functionality section for additional information. After being enabled, the CRC result is appended to the conversion result and consists of a 16-bit word, where the first eight bits contain the channel ID of the last channel pair converted and the last eight bits are the CRC result. The result is accessed via an extra read command, as shown in Figure 68.

In software mode, the CRC function is enabled by setting either the CRCEN bit or the STATUSEN bit in the configuration register to 1 (see the section).

If the CRC function is enabled, a CRC is calculated on the conversion results for Channel VxA and Channel VxB. The CRC is calculated and transferred on the serial or parallel interface after the conversion results are transmitted, depending on the configuration of the device. The Hamming distance varies relative to the number of bits in the conversion result. For conversions with ≤119 bits, the Hamming distance is 4. For >119 bits, the Hamming distance is 1, that is, 1-bit errors are always detected.

The following is a pseudocode description of how the CRC is implemented in the DAD7616:

```
crc = 8'  b0;
i = 0;
x = number of conversion channel pairs;
for (i=0, i<x, i++) begin
crc1 = crc_out(An,Crc);
crc = crc_out(Bn,Crc1);
i = i +1;
end
```

Where the function crc_out(data, crc) is

```
crc_out[0] = data[14] ^ data[12] ^ data[8] ^ data[7] ^ data[6]
^ data[0] ^ crc[0] ^      crc[4] ^ crc[6];
crc_out[1] = data[15] ^ data[14] ^ data[13] ^ data[12] ^
data[9] ^ data[6] ^ data[1] ^ data[0] ^ crc[1] ^ crc[4] ^ crc[5]
^ crc[6] ^ crc[7];
crc_out[2] = data[15] ^ data[13] ^ data[12] ^ data[10] ^
data[8] ^ data[6] ^ data[2] ^  data[1] ^ data[0] ^ crc[0] ^ crc[2]
^ crc[4] ^ crc[5] ^ crc[7];
crc_out[3] = data[14] ^ data[13] ^ data[11] ^ data[9] ^ data[7]
^ data[3] ^ data[2] ^   data[1] ^ crc[1] ^ crc[3] ^ crc[5] ^ crc[6];
crc_out[4] = data[15] ^ data[14] ^ data[12] ^ data[10] ^
data[8] ^ data[4] ^ data[3] ^  data[2] ^ crc[0] ^ crc[2] ^ crc[4]
^ crc[6] ^ crc[7];
crc_out[5] = data[15] ^ data[13] ^ data[11] ^ data[9] ^
data[5] ^ data[4] ^ data[3] ^  crc[1] ^ crc[3] ^ crc[5] ^
crc[7];
crc_out[6] = data[14] ^ data[12] ^ data[10] ^ data[6] ^
data[5] ^ data[4] ^ crc[2] ^   crc[4] ^ crc[6];
crc_out[7] = data[15] ^ data[13] ^ data[11] ^ data[7] ^
data[6] ^ data[5] ^ crc[3] ^crc[5] ^ crc[7];
```

The initial CRC word used by the DAD7616 is an 8-bit word equal to zero. The XOR operation described in the preceding code is executed to calculate each bit of the CRC word for the conversion result, AN. This CRC word (crc1) is then used as the starting point for calculating the CRC word (crc) for the conversion result, BN. The process repeats cyclically for each channel pair converted. Depending on the mode of operation of the DAD7616, the status register value is appended to the conversion data and read out via an extra read command over the serial or parallel interface. The user can then repeat the XOR calculation described in the preceding code for the received conversion results to check whether both CRC words match. See Figure 68 or a description of how the CRC word is appended to the data for each mode of Operation.

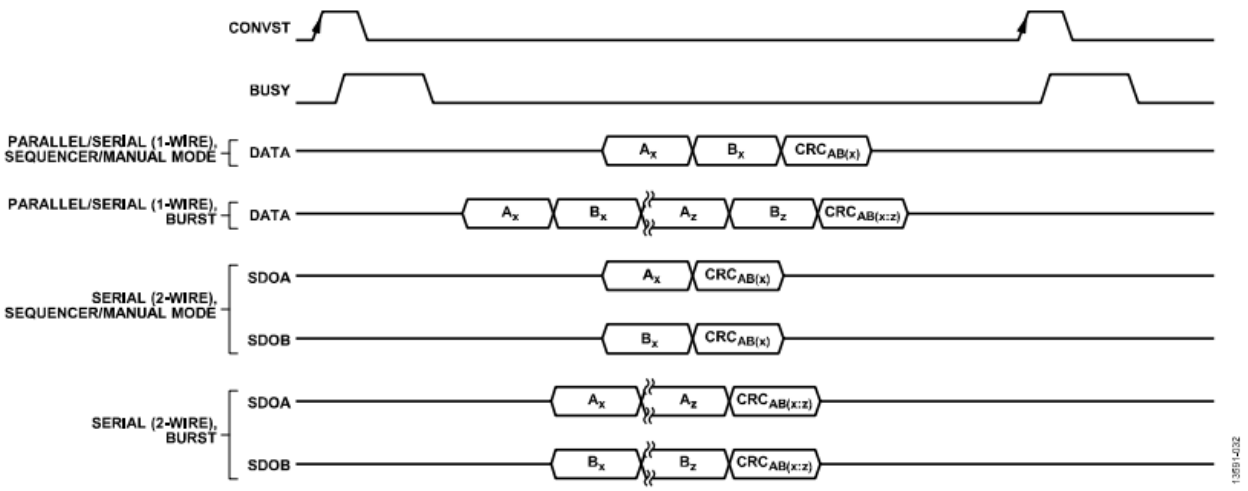


Figure. CRC Readback for All Modes

REGISTER SUMMARY

The DAD7616 has six read/write registers used for configuring the device in software mode and an additional 16 sequencer stack registers for programming the flexible on-chip sequencer and a read only status register. Below Table shows an overview of the read/write registers available on the DAD7616. The status register is an additional read only register than contains information on the channel pair previously converted and the CRC result.

Table. Register Summary1

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x02	Configuration Register	[15:8]	Addressing							Reserved	0x0000	R/W
		[7:0]	SDEF	BURSTEN	SEQEN	OS			STATUSEN	CRCEN		
0x03	Channel Register	[15:8]	Addressing							Reserved	0x0000	R/W
		[7:0]	CHB				CHA					
0x04	Input Range RegisterA1	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V3A		V2A		V1A		V0A			
0x05	Input Range RegisterA2	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V7A		V6A		V5A		V4A			
0x06	Input Range RegisterB1	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V3B		V2B		VB1		V0B			
0x07	Input Range RegisterB2	[15:8]	Addressing							Reserved	0x00FF	R/W
		[7:0]	V7B		V6B		VB5		V4B			
0x20 to 0x2F	Sequencer Stack Registers [0:15]	[15:8]	Addressing							SSRENx	0x00002	R/W
		[7:0]	BSELx				ASELx					
N/A	Status Register	[15:8]	A[3:0]				B[3:0]				N/A	R
		[7:0]	CRC[7:0]									

1 N/A means not applicable.
2 After a full or partial rest is issued, the sequencer stack register is reinitialized to cycle through Channel V0A and Channel V0B to Channel V7A and Channel V7B. The remaining 8 layers of the stack are reinitialized to 0x0.

ADDRESSING REGISTERS

The seven MSBs written to the device are decoded to determine which register is addressed. The seven MSBs consist of the register address (REGADDR), Bits[5:0], and the read/write bit. The register address bits determine which on-chip register is selected. The read/write bit determines if the remaining nine bits of data on the DB10/SDI lines are loaded into the addressed register. If the read/write bit is 1, the bits load into the register addressed by the register select bits. If the read/write bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

MSB **LSB**

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8 to D0**
W/R	REGADDR[5]	REGADDR[4]	REGADDR[3]	REGADDR[2]	REGADDR[1]	REGADDR[0]	DATA[8:0]

Table.

Bits	Mnemonic	Description
D15	W/R	If a 1 is written to this bit, Bits[D8:D0] of this register are written to the register specified by REGADDR[5:0]. Alternatively, if a 0 is written, the next operation is a read from the designated register.
D14	REGADDR[5]	If a 1 is written to this bit, the contents of REGADDR[4:0] specifies the 16 sequencer stack registers. Alternatively, if a 0 is written to this bit, a register is selected as defined by REGADDR[4:0].
[D13:D9]	REGADDR[4:0]	When W/R =1, the contents of REGADDR[4:0] determine register for selection as follows: 00001: reserved. 00010: selects the configuration register. 00011: selects the channel register. 001000: selects Input Range Register A1. 00101: selects Input Range Register A2. 00110: selects Input Range Register B1. 00111: selects Input Range Register B2. 01000: selects the status register. When W/R = 0, and REGADDR[4:0] contains 00000, the conversion codes are read.
[D8:D0]	DATA[8:0]	These bits are written into the corresponding register specified by Bits REGADDR[5:0]. See the following sections for detailed descriptions of each register.

CONFIGURATION REGISTER

The configuration register is used in software mode to configure many of the main functions of the ADC, including the sequencer, burst mode, oversampling, and CRC options. Address: 0x02, Reset: 0x0000, Name: Configuration Register

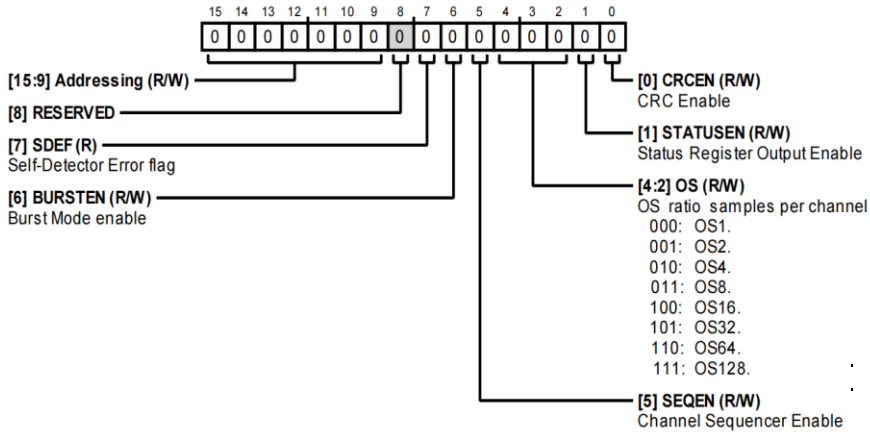


Table. Bit Descriptions for the Configuration Register

Bits	Bit Name	Settings	Description	Reset1	Access
[15:9]	Addressing	0	Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	RW
8	RESERVED		Reserved.	0x0	R/W
7	SDEF		Self detector error flag.	N/A	R
		0	Test passed. The DAD7616 has configured itself successfully after power-up.		
		1	Test failed. An issue was detected during device configuration. A reset is required.		
6	BURSTEN		Burst mode enable.	0x0	RW
		0	Burst mode is disabled. Each channel pair to be converted requires a CNVST pulse.		
		1	A single CNVST pulse converts every channel pair programmed in the 16-layer sequencer stack registers up to and including the layer defined by the SSRENx bit. See the Software Mode Sequencer section and the Software Mode Burst section for further details.		
5	SEQEN		Channel sequencer enable.	0x0	RW
		0	The channel sequencer is disabled.		
		1	The channel sequencer is enabled.		
[4:2]	OS		Oversampling (OS) ratio, samples per channel.	0x0	RW
		000	Oversampling disabled.		
		001	Oversampling enabled, OSR = 2.		
		010	Oversampling enabled, OSR = 4.		
		011	Oversampling enabled, OSR = 8.		
		100	Oversampling enabled, OSR = 16.		
		101	Oversampling enabled, OSR = 32.		
		110	Oversampling enabled, OSR = 64.		
		111	Oversampling enabled, OSR = 128.		
1	STATUSEN		Status register output enable.	0x0	RW
		0	The status register is not read out when reading the conversion result.		
		1	The status register is read out at the end of all the conversion words (including the self test channel if enabled in sequencer mode) if all the selected channels are read out. The CRC result is included in the last eight bits.		
0	CRCEN		CRC enable. The STATUSEN and CRCEN bits have identical functionality.	0x0	RW

1 N/A means not applicable.

CHANNEL REGISTER

Address: 0x03, Reset: 0x0000, Name: Channel Register

In software manual mode, the channel register selects the input channel or self test channel for the next conversion.

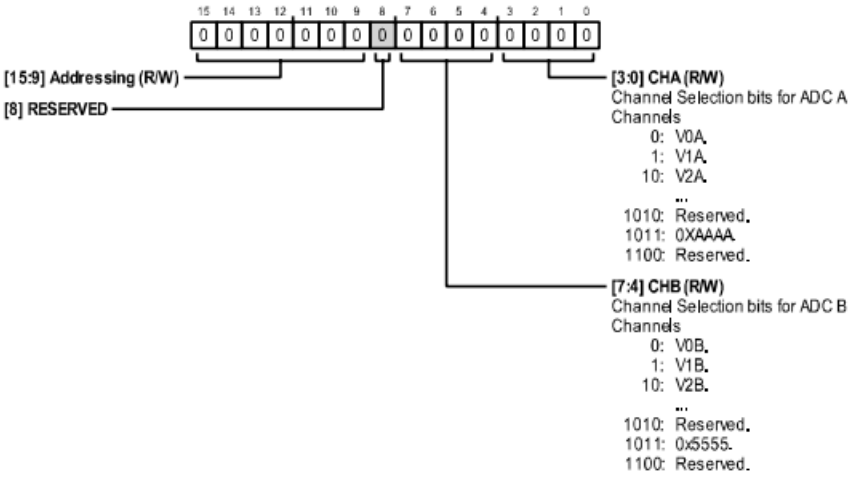


Table 22. Bit Descriptions for the Channel Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:4]	CHB		Channel selection bits for ADC B channels.		
		0000	V0A/V0B		
		0001	V1A/V1B		
		0010	V2A/V2B		
		0011	V3A/V3B		
		0100	V4A/V4B		
		0101	V5A/V5B		
		0110	V6A/V6B		
		0111	V7A/V7B		
		1000	Vcc		
		1001	ALDO		
		1010	Reserved.		
		1011	Set the dedicated bits for digital interface communication self test function. When conversion codes are read, Code 0xAAAA is read out as the conversion code of Channel A, and Code 0x5555 is output as the conversion code of Channel B. When using the communication self-test mode, the chip's normal channel conversion accuracy decreases.		
		1100	Reserved.		
[3:0]	CHA		Channel selection bits for ADC A Channels. Settings are the same as for ADC B.	0x0	R/W

INPUT RANGE REGISTERS

Input Range Register A1 and Input Range Register A2 select from one of the three possible input ranges (±10 V, ±5 V, or ±2.5 V) for analog input Channel V0A to Channel V7A. Input Range Register B1 and Input Range Register B2 select from one of the three possible input ranges (±10 V, ±5 V, or ±2.5 V) for analog input Channel V0B to Channel V7B.

INPUT RANGE REGISTER A1

Address: 0x04, Reset: 0x00FF, Name: Input Range Register A1

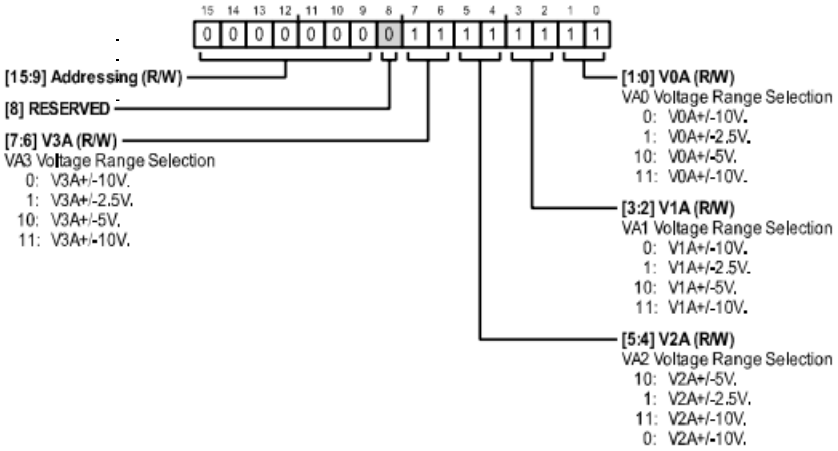


Table. Bit Descriptions for Input Range Register A1

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V3A	00 01 10 11	V3A voltage range selection. V3A ± 10 V. V3A ± 2.5 V. V3A ± 5 V. V3A ± 10 V.	0x3	R/W
[5:4]	V2A	00 01 10 11	V2A voltage range selection. V2A ± 10 V. V2A ± 2.5 V. V2A ± 5 V. V2A ± 10 V.	0x3	R/W
[3:2]	V1A	00 01 10 11	V1A voltage range selection. V1A ± 10 V. V1A ± 2.5 V. V1A ± 5 V. V1A ± 10 V.	0x3	R/W
[1:0]	V0A	00 01 10 11	V0A voltage range selection. V0A ± 10 V. V0A ± 2.5 V. V0A ± 5 V. V0A ± 10 V.	0x3	R/W

INPUT RANGE REGISTER A2

Address: 0x05, Reset: 0x00FF, Name: Input Range Register A2

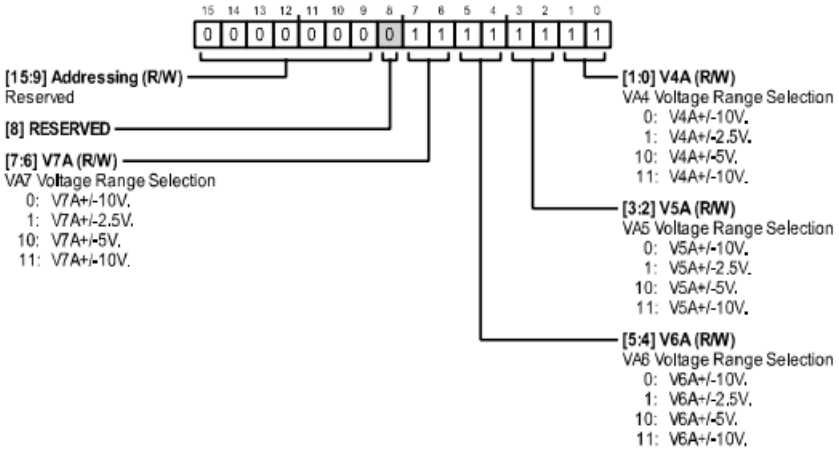


Table. Bit Descriptions for Input Range Register A2

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V7A		V7A voltage range selection.	0x3	R/W
		00	V7A ± 10 V.		
		01	V7A ± 2.5 V.		
		10	V7A ± 5 V.		
		11	V7A ± 10 V.		
[5:4]	V6A		V6A voltage range selection.	0x3	R/W
		00	V6A ± 10 V.		
		01	V6A ± 2.5 V.		
		10	V6A ± 5 V.		
		11	V6A ± 10 V.		
[3:2]	V5A		V5A voltage range selection.	0x3	R/W
		00	V5A ± 10 V.		
		01	V5A ± 2.5 V.		
		10	V5A ± 5 V.		
		11	V5A ± 10 V.		
[1:0]	V4A		V4A voltage range selection.	0x3	R/W
		00	V4A ± 10 V.		
		01	V4A ± 2.5 V.		
		10	V4A ± 5 V.		
		11	V4A ± 10 V.		

INPUT RANGE REGISTER B1

Address: 0x06, Reset: 0x00FF, Name: Input Range Register B1

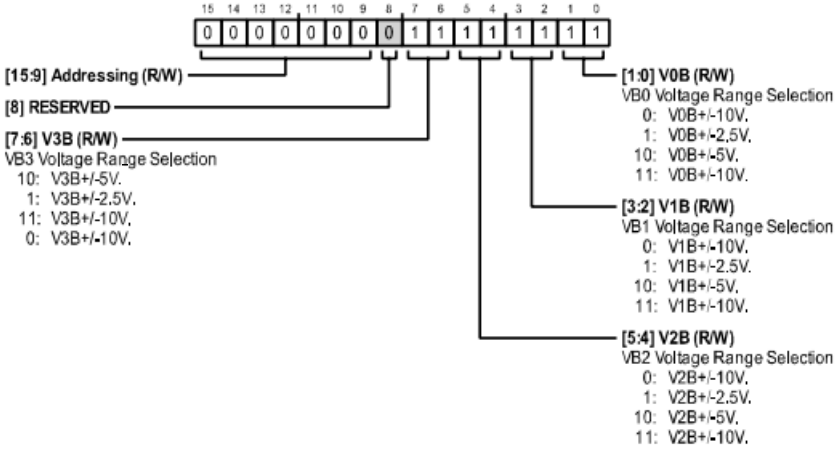


Table. Bit Descriptions for Input Range Register B1

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V3B		V3B voltage range selection.	0x3	R/W
		00	V3B ± 10 V.		
		01	V3B ± 2.5 V.		
		10	V3B ± 5 V.		
		11	V3B ± 10 V.		
[5:4]	V2B		V2B voltage range selection.	0x3	R/W
		00	V2B ± 10 V.		
		01	V2B ± 2.5 V.		
		10	V2B ± 5 V.		
		11	V2B ± 10 V.		
[3:2]	VB1		VB1 voltage range selection.	0x3	R/W
		00	VB1 ± 10 V.		
		01	VB1 ± 2.5 V.		
		10	VB1 ± 5 V.		
		11	VB1 ± 10 V.		
[1:0]	V0B		V0B voltage range selection.	0x3	R/W
		00	V0B ± 10 V.		
		01	V0B ± 2.5 V.		
		10	V0B ± 5 V.		
		11	V0B ± 10 V.		

INPUT RANGE REGISTER B2

Address: 0x07, Reset: 0x00FF, Name: Input Range Register B2

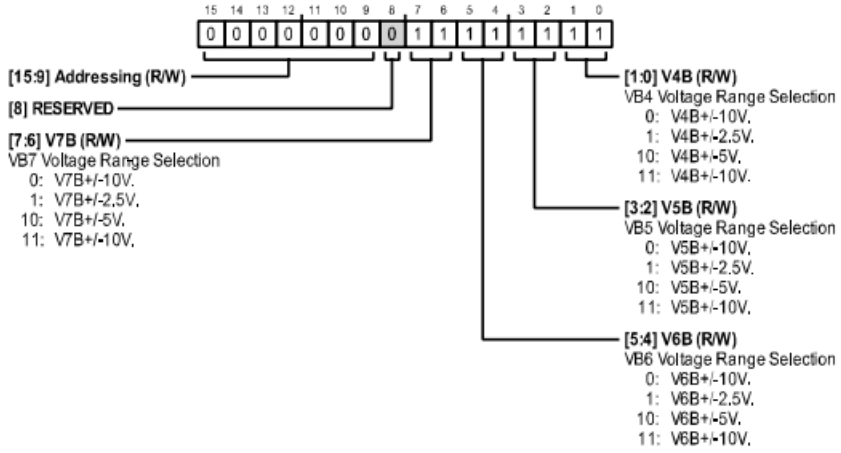


Table. Bit Descriptions for Input Range Register B2

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	RESERVED		Reserved.	0x0	R/W
[7:6]	V7B		V7B voltage range selection.	0x3	R/W
		00	V7B ± 10 V.		
		01	V7B ± 2.5 V.		
		10	V7B ± 5 V.		
		11	V7B ± 10 V.		
[5:4]	V6B		V6B voltage range selection.	0x3	R/W
		00	V6B ± 10 V.		
		01	V6B ± 2.5 V.		
		10	V6B ± 5 V.		
		11	V6B ± 10 V.		
[3:2]	V5B		V5B voltage range selection.	0x3	R/W
		00	V5B ± 10 V.		
		01	V5B ± 2.5 V.		
		10	V5B ± 5 V.		
		11	V5B ± 10 V.		
[1:0]	V4B		V4B voltage range selection.	0x3	R/W
		00	V4B ± 10 V.		
		01	V4B ± 2.5 V.		
		10	V4B ± 5 V.		
		11	V4B ± 10 V.		

SEQUENCER STACK REGISTERS

Although the channel register defines the next channel for conversion (be it a diagnostic channel or pair of analog input channels), to sample numerous analog input channels, the 16 sequencer stack registers offer a convenient solution. Within the communication register, when the REGADDR5 bit is set to Logic 1, the contents of REGADDR[4:0] specifies 1 of the 16 sequencer stack registers. Within each sequencer stack register, the user can define a pair of analog inputs to sample simultaneously.

The structure of the sequence forms a stack, in which each row represents two channels to convert simultaneously. The sequence begins with Sequencer Stack Register 1 and cycles through to Sequencer Stack Register 16. If Bit D8 (the enable bit, SSRENx) within a sequencer stack register is set to 1, the sequence ends with the pair of analog inputs defined by that register, then returns to the first sequencer stack register, and resumes the cycle again. By default, the sequencer stack registers are programmed to cycle through Channel V0A and Channel V0B to Channel V7A and Channel V7B. After a full or partial reset is issued, the sequencer stack register reinitializes to cycle through Channel V0A and Channel V0B to Channel V7A and Channel V7B.

Address: 0x20 to 0x2F, Reset: 0x0000, Name: Sequencer Stack Registers[0:15]

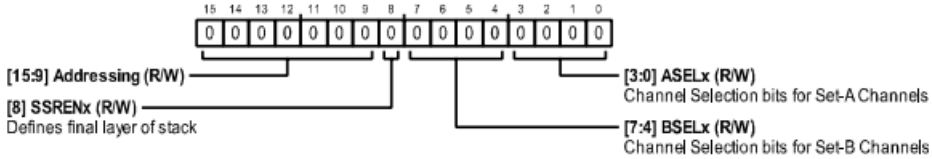


Table. Bit Descriptions for Sequencer Stack Registers[0:31]

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Addressing		Bits[15:9] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
8	SSREN[0:31]		Setting this bit to 0 instructs the ADC to move to the next layer of the sequencer stack after converting the present channel pair. Setting this bit to 1 defines that layer of the sequencer stack as the final layer in the sequence. Thereafter, the sequencer loops back to the first layer of the stack.	0x0	R/W
[7:4]	BSEL[0:31]		Channel selection bits for ADC B channels.	0x01	R/W
		0000	V0B.		
		0001	V1B.		
		0010	V2B.		
		0011	V3B.		
		0100	V4B.		
		0101	V5B.		
		0110	V6B.		
		0111	V7B.		
		1000	V_{CC}.		
		1001	ALDO.		
		1010	Reserved.		
		1011	Set the dedicated bits for digital interface communication self test function. When the conversion codes is read, Code 0xAAAA is read out as the conversion code of Channel A, and Code 0x5555 is output as the conversion code of Channel B. When using the communication self-test mode, the chip's normal channel conversion accuracy decreases.		
		1100	Reserved.		
[3:0]	ASEL[0:31]		Channel selection bits for ADC A channels. Settings are the same as for ADC B.	0x01	R/W

1 After a full or partial reset is issued, the sequencer stack register is reinitialized to cycle through Channel V0A and Channel V0B to Channel V7A and Channel V7B. The remaining 8 layers of the stack are reinitialized to 0x0.

STATUS REGISTER

The status register is a 16-bit read only register. If the STATUSEN bit or the CRCEN bit is set to Logic 1 in the configuration register, the status register is read out at the end of all conversion words for the selected channels, including the self test channel if enabled in sequencer mode. Consult the CRC section and Figure 68.

MSB **LSB**

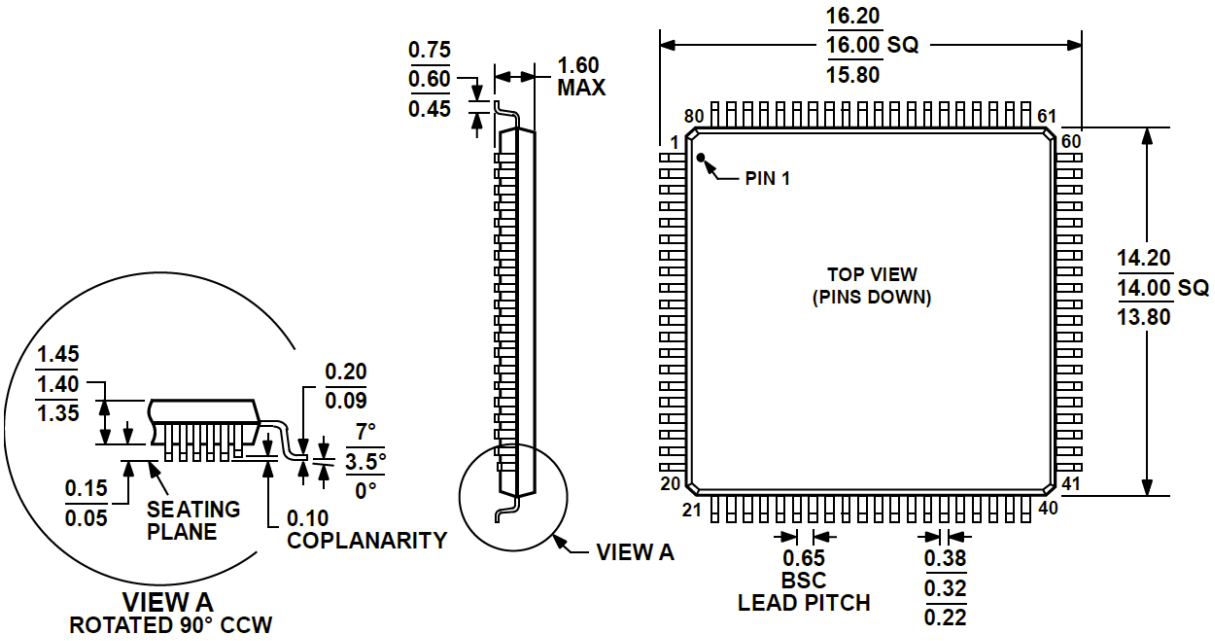
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A[3:0]				B[3:0]				CRC[7:0]							

Table. Bit Descriptions for Status Register

Bits	Bit Name	Settings	Description	Reset1	Access
[D15:D12] [D11:D8] [D7:D0]	A[3:0] B[3:0] CRC[7:0]		Channel index for previous conversion result on Channel A. Channel index for previous conversion result on Channel B. CRC calculation for the previous conversion result(s). Refer to the CRC section for further details.	N/A N/A N/A	R R R

1 N/A means not applicable.

OUTLINE DIMENSIONS



ORDERING GUIDE

Model	Temperature Range	Package Type	Packaging	ROHS
DAD7616LFP	–40°C to +125°C	80-LQFP	900/tray	Y