DAD7608 8-Channel DAS with 18-Bit, Bipolar Input, Simultaneous Sampling ADC

OVERVIEW

- The DAD7608 is an 18-bit, 8-channel simultaneous sampling data acquisition system (DAS). Each device integrates an analog input clamp protection circuit, a second-order anti-aliasing filter, a track-and-hold amplifier, an 18-bit charge-redistribution successive approximation ADC, a flexible digital filter, a 2.5 V reference voltage source, a reference buffer, and a high-speed serial interface.
- The DAD7608 operates from a single 5 V power supply and can handle true bipolar input signals of ±10 V and ±5 V, while all channels can sample at throughput rates up to 200 kSPS. The input clamp protection circuitry can withstand voltages up to ±16.5 V. Regardless of the sampling rate, the DAD7608 features an analog input impedance of 1 MΩ. It operates from a single power supply and, with its on-chip filtering and high input impedance, eliminates the need for a driver operational amplifier or an external bipolar power supply.
- The DAD7608 features an anti-aliasing filter with a 3 dB cutoff frequency of 22 kHz. When operating at a sampling rate of 200 kSPS, it provides 40 dB of anti-aliasing attenuation. The flexible digital filter is pin-configurable and can improve the signal-to-noise ratio (SNR) while reducing the 3 dB bandwidth.

APPLICATIONS

- Multiphase motor controls
- Power line monitoring and protection systems
- Instrumentation and control systems
- Data acquisition systems (DAS)
- Multiaxis positioning systems

FEATURES AND BENEFITS

- Single power supply operation +2.5V~+5.5V
- 8 simultaneously sampled inputs
- True bipolar analog input ranges: ±10 V, ±5 V
- Single 5 V analog supply and 2.3 V to 5 V VDRIVE
- Analog input clamp protection
- Input buffer with 1 MΩ analog input impedance
- Second-order antialiasing analog filter
- On-chip precision reference voltage and buffer with a temperature coefficient of 5 ppm/℃
- 18-bit ADC with 200 kSPS on all channels
- Oversampling capability with digital filter
- Flexible serial interface

SPI/QSP/MICROWIR/DSP compatible

- 7 kV ESD rating on analog input channels

97 dB SNR, −107 dB THD

- ±0.5 LSB INL, ±0.5 LSB DNL
- Low power: 130 mW, Standby mode: 35 mW
- Temperature range: −40°C to +85°C/−40°C to +125°C
- 64-lead LQFP package

1. DEVICE INFORMATION

Model	Package	Size
DAD7608-C	LQFP-64	12mm×12mm
DAD7608-E	LQFP-64	12mm×12mm

*For more information, please refer to the ordering information

FUNCTIONAL BLOCK DIAGRAM

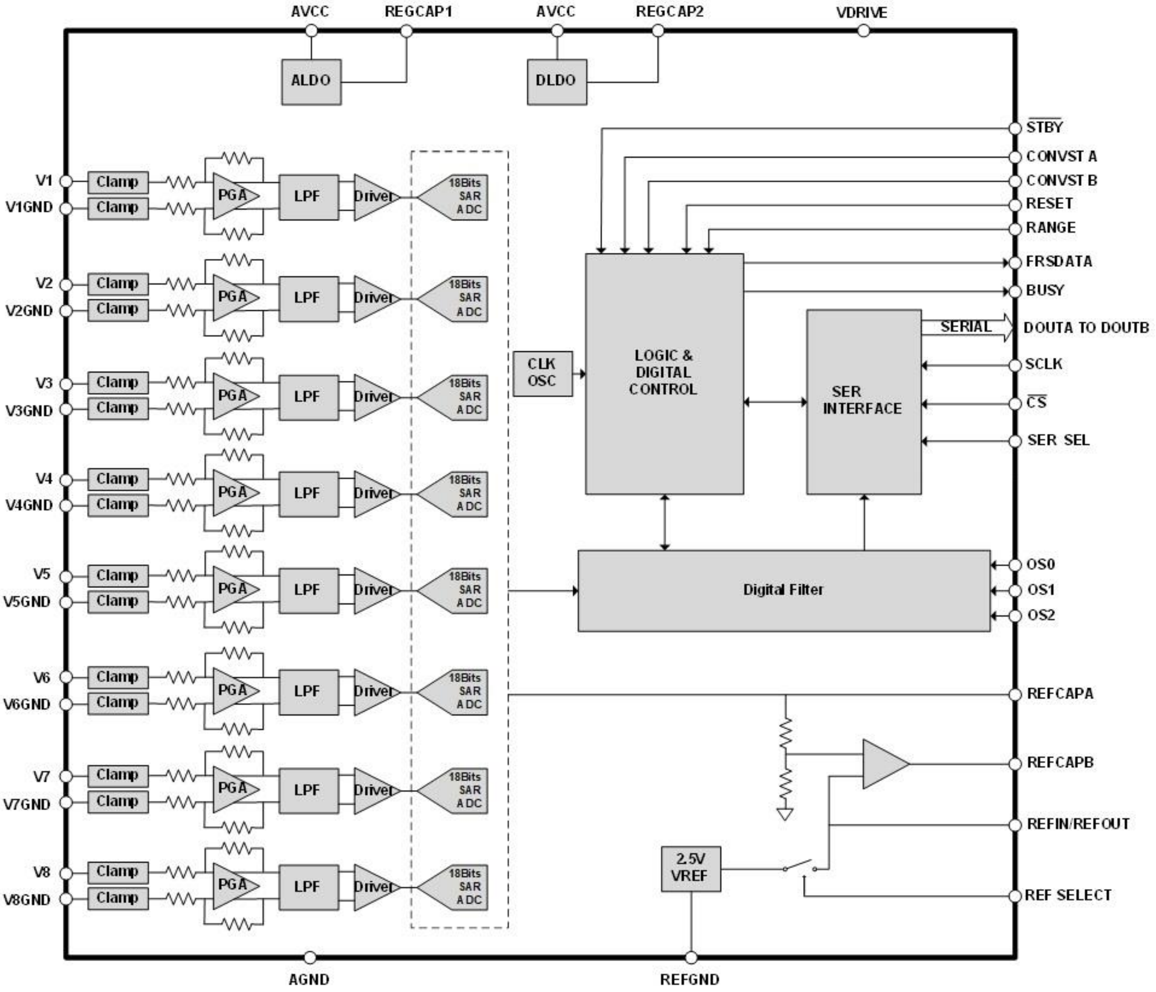

Figure1. Typical Principle Block Diagram

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SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the following absolute maximum rated values may cause permanent damage to the device.

Mnemonic	Parameter	Min	Max	Unit
AVCC	AVCC to AGND	–0.3	7.0	V
VDRIVE	VDRIVE to DGND	–0.3	7.0	V
	AGND to DGND	–0.3	0.3	V
VAIN	Analog Input Voltage to AGND	–15	15	V
VD	Digital Input Voltage to DGND	–0.3	VDRIVE + 0.3	V
Vref	REFIN to AGND	–0.3	AVCC + 0.3	V
Iin	Input Current to Any Pin Except Supplies	–10	10	mA
TA	Operating Temperature Range	–40	85	°C
TJ	Junction Temperature	150		
Tstg	Storage Temperature Range	–65	150	

Electrostatic Level

Mnemonic	Parameter	Conditions	Rating	Unit
VESD-HBM	The human body model (HBM) complies with ANSI/ESDA/JEDEC JS-001	All pins except the analog inputs	±3000	V
		Only analog input pins	±7000	V
VESD-CDM	Charging mode (CDM) complies with JEDEC JESD22-C101	All pins	±500	V

Thermal Information

Mnemonic	Parameter	Rating	Unit
RθJA	Junction-to-ambient thermal resistance	46.0	°C/W
RθJC(top)	Junction-to-case (top) thermal resistance	7.8	°C/W
RθJB	Junction-to-board thermal resistance	20.1	°C/W
Mnemonic	**Parameter**	**Rating**	**Unit**
Pb/SN Temperature, Soldering	Reflow (10 sec to 30 sec)	240 (+0)	℃
Pb/SN Temperature, Soldering	Pb-Free Temperature, Soldering Reflow	260 (+0)	℃

Electrical Characteristics

At TA = -40℃ to 85℃, Vs = 1.65V to 5.5V (unless otherwise noted)

Mnemonic		Parameter	Test Conditions /Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE		fIN= 1 kHz sine wave unless otherwise noted					
SNR	Signal-to-Noise Ratio （SNR）	Oversampling by 16; ±10 V range; fIN=130Hz		97.5	99		dB
		Oversampling by 16; ±5 V range; fIN=130Hz		95	97		dB
		No oversampling; ±10 V range		89	90.5		dB
		No oversampling; ±5 V range		88.5	90		dB
SINAD	Signal-to-(Noise + Distortion) (SINAD)	No oversampling; ±10 V range		89	90.5		dB
		No oversampling; ±5 V range		88.9	90		dB
Dynamic Range	Dynamic Range	No oversampling; ±10 V range			91.5		dB
		No oversampling; ±5 V range			90.5		dB
THD	Total Harmonic Distortion(THD)				-106	-95	dB
SFDR	Peak Harmonic or Spurious Noise				-109		dB
IMD	Intermodulation Distortion(IMD)	fa = 1 kHz, fb = 1.1 kHz					
	Second-Order Terms			-110			dB
	Third-Order Terms			-111			dB
	Channel-to-Channel Isolation	fIN on unselected channels up to 160 kHz		-105			dB
ANALOG INPUT FILTER							
BW(-3dB)	Full Power Bandwidth	−3 dB, ±10 V range			43		kHz
		−3 dB, ±5 V range			20		kHz
BW(-0.1dB)		−0.1 dB, ±10 V range			10		kHz
		−0.1 dB, ±5 V range			5		kHz
$t_{GROUP\ DELAY}$	$t_{GROUP\ DELAY}$	±10 V range			11		µs
		±5 V range			15		µs
Mnemonic	**Parameter**		**Test Conditions/ Comments**	**Min**	**Typ**	**Max**	**Unit**
DC ACCURACY							
	Resolution		No missing codes	18			Bits
DNL	Differential Nonlinearity				±0.75	±0.99	LSB
INL	Integral Nonlinearity				±2.5	±7.5	LSB
TUE	Total Unadjusted Error (TUE)		±10 V range		±15		LSB
			±5 V range		±40		LSB
EPFS	Positive Full-Scale Error		External reference		±15	±120	LSB
			Internal reference		±40		LSB
	Positive Full-Scale Error Drift		External reference		±2		ppm/°C
			Internal reference		±7		ppm/°C
	Positive Full-Scale Error Matching		±10 V range		12	95	LSB

		±5 V range		30	125	LSB
EZC	Bipolar Zero Code Error	±10 V range		±3.5	±24	LSB
		± 5 V range		±3.5	±48	LSB
	Bipolar Zero Code Error Drift	±10 V range		10		μV/°C
		± 5 V range		5		μV/°C
	Bipolar Zero Code Error Matching	±10 V range		3	30	LSB
		±5 V range		21	65	LSB
ENFS	Negative Full-Scale Error	External reference		±15	±128	LSB
		Internal reference		±40		LSB
	Negative Full-Scale Error Drift	External reference		±4		ppm/°C
		Internal reference		±8		ppm/°C
	Negative Full-Scale Error Matching	±10 V range		12	95	LSB
		±5 V range		30	128	LSB
ANALOG INPUT						
AIN	Input Voltage Ranges	RANGE = 1			±10	V
		RANGE = 0			±5	V
Iin	Analog Input Current	10V/5V	5.4/2.5			μA
CAIN	Input Capacitance			5		pF
Rin	Input Impedance	Refer to the analog input section		1		MΩ
REFERENCE INPUT/OUTPUT						
VREF-IN	Reference Input Voltage Range	Refer to the section on ADC transfer function	2.475	2.5	2.525	V
IRLK	DC Leakage Current				±1	μA
CREFIN	Input Capacitance	REF SELECT = 1		7.5		pF
VREF-OUT	Reference Output Voltage	REFIN/ REFOUT	2.49	2.5	2.505	V
	Reference Temperature Coefficient			±10		ppm/°C
LOGIC INPUTS						
VINH	Input High Voltage (VINH)		0.9 × VDRIVE			V
VINL	Input Low Voltage (VINL)				0.1× VDRIVE	V
IIN	Input Current (IIN)				±2	μA
CLIN	Input Capacitance (CIN)			5		pF

Mnemonic	**Parameter**	**Test Conditions /Comments**	**Min**	**Typ**	**Max**	**Unit**
LOGIC OUTPUTS						
VOH	Output High Voltage (VOH)	ISOURCE= 100 µA	VDRIVE -0.2			V
VOL	Output Low Voltage(VOL)	ISINK= 100 µA			0.2	V
ILLK	Floating-State Leakage Current			±1	±20	µA
CLOUT	Floating-State Output Capacitance			5		pF
	Output Coding	Twos complement				
POWER REQUIREMENTS						
AVCC	AVCC		4.75		5.25	V
VDRIVE	VDRIVE		2.3		5.25	V
ITOTAL	ITOTAL	Digital inputs = 0 V or VDRIVE				
IStatic	Normal Mode (Static)			16	22	mA
IAVCC	Normal Mode (Operational)	fSAMPLE= 200ksps		20	27	mA
ISTDBY	Standby Mode			5	8	mA
ISTDN	Shutdown Mode			2	11	uA
Power Dissipation						
	Normal Mode (Static)			80	115.5	mW
	Normal Mode (Operational)	fSAMPLE= 200ksps		100	142	mW
	Standby Mode			25	42	mW
	Shutdown Mode			10	58	µW

TIMING SPECIFICATIONS

AVcc = 4.75 V to 5.25 V, Vdrive = 2.3 V to 5.25 V, VREF = 2.5 V external reference/internal reference, Ta = Tmin to Tmax, unless otherwise noted.

Mnemonic	Parameter	Limit at TMIN, TMAX (0.1 × VDRIVE and 0.9 × VDRIVE Logic Input Levels)			Unit
		Min	Typ	Max	
tCYCLE	1/throughput rate				
	Serial mode, reading during or after conversion; VDRIVE =2.7 V		5		µs
	Serial mode, reading during or after conversion; VDRIVE =2.3 V, DOUTA and DOUTB lines			9.7	µs
tCONV	Conversion time				
	Oversampling off	3.45	4	4.2	µs
	Oversampling by 2	7.87		9.1	µs
	Oversampling by 4	16.05		18.8	µs
	Oversampling by 8	33		39	µs
	Oversampling by 16	66		78	µs
	Oversampling by 32	133		158	µs
tWAKE-UP STANDBY	STBY rising edge to CONVST x rising edge; power-up time from standby mode			100	µs
tWAKE-UP SHUTDOWN					
Internal Reference	STBY rising edge to CONVST x rising edge; power-up time from shutdown mode			30	ms
External Reference	STBY rising edge to CONVST x rising edge; power-up time from shutdown mode			13	ms
tRESET	RESET high pulse width	50			ns
tOS_SETUP	BUSY to OS x pin setup time	20			ns
tOS_HOLD	BUSY to OS x pin hold time	20			ns
t1	CONVST x high to BUSY high			40	ns
t2	Minimum CONVST x low pulse	25			ns
t3	Minimum CONVST x high pulse	25			ns
t4	BUSY falling edge to CS falling edge setup time	0			ns
t5	Maximum delay allowed between CONVST A, CONVST B rising edges			0.5	ms
t6	Maximum time between last CS rising edge and BUSY falling edge			25	ns
t7	Minimum delay between RESET low to CONVST x high	25			ns
t8	CS to RD setup time	0			ns
t9	CS to RD hold time	0			ns
t10	RD low pulse width				
	VDRIVE above 4.75 V	16			ns

	VDRIVE above 3.3 V	21			ns
	VDRIVE above 2.7 V	25			ns
	VDRIVE above 2.3 V	32			ns
t11	RD high pulse width	15			ns
t12	CS high pulse width; CS and RD linked	22			ns
t13	Delay from CS until DB[15:0] three-state disabled				
	VDRIVE above 4.75 V			16	ns
	VDRIVE above 3.3 V			20	ns
	VDRIVE above 2.7 V			25	ns
	VDRIVE higher than 2.3 V			30	ns
t14	Data access time after the RD falling edge				
	VDRIVE above 4.75 V			16	ns
	VDRIVE above 3.3 V			21	ns
	VDRIVE above 2.7 V			25	ns
	VDRIVE above 2.3 V			32	ns
t15	Data hold time after the RD falling edge	6			ns
t16	CS to DB [15:0] hold time	6			ns
t17	Delay from CS rising edge to DB[15:0] three-state enabled			22	ns
fSCLK	Frequency of serial read clock				
	VDRIVE above 4.75 V			23.5	MHz
	VDRIVE above 3.3 V			17	MHz
	VDRIVE above 2.7 V			14.5	MHz
	VDRIVE above 2.3 V			11.5	MHz
t18	Delay from CS until DOUTA/DOUTB three-state disabled/delay from CS until MSB valid				
	VDRIVE above 4.75 V			15	ns
	VDRIVE above 3.3 V			20	ns
	VDRIVE = 2.3 V to 2.7 V			30	ns
t19	Data access time after SCLK rising edge				
	VDRIVE above 4.75 V			17	ns
	VDRIVE above 3.3 V			23	ns
	VDRIVE above 2.7 V			27	ns
	VDRIVE above 2.3 V			34	ns
t20	SCLK low pulse width	0.4 tSCLK			ns
t21	SCLK high pulse width	0.4 tSCLK			ns
t22	SCLK rising edge to DOUTA/DOUTB valid hold time	7			
t23	CS rising edge to DOUTA/DOUTB three-state enabled			22	ns

t24	Delay from CS falling edge until FRSTDATA three-state disabled				
	VDRIVE above 4.75 V			15	ns
	VDRIVE above 3.3 V			20	ns
	VDRIVE above 2.7 V			25	ns
	VDRIVE above 2.3 V			30	ns
t25	Delay from CS falling edge until FRSTDATA high, serial mode				ns
	VDRIVE above 4.75 V			15	ns
	VDRIVE above 3.3 V			20	ns
	VDRIVE above 2.7 V			25	ns
	VDRIVE above 2.3 V			30	ns
t26	Delay from RD falling edge to FRSTDATA high				
	VDRIVE above 4.75 V			16	ns
	VDRIVE above 3.3 V			20	ns
	VDRIVE above 2.7 V			25	ns
	VDRIVE above 2.3 V			30	ns
t27	Delay from RD falling edge to FRSTDATA low				
	VDRIVE = 3.3 V to 5.25V			19	ns
	VDRIVE = 2.3 V to 2.7V			24	ns
t28	Delay from 16th SCLK falling edge to FRSTDATA low				
	VDRIVE = 3.3 V to 5.25V			17	ns
	VDRIVE = 2.3 V to 2.7V			22	ns
t29	Delay from CS rising edge until FRSTDATA three-state enabled			24	ns

Timing Diagrams

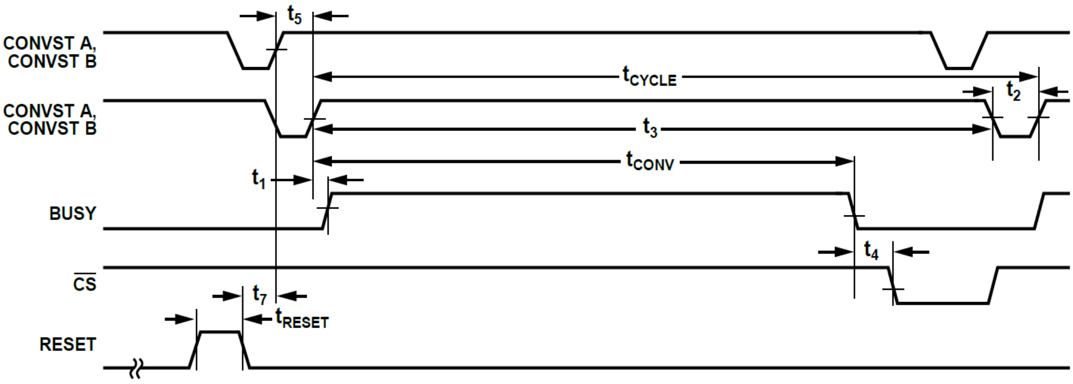


Figure 2: CONVST x Timing—Reading After a Conversion

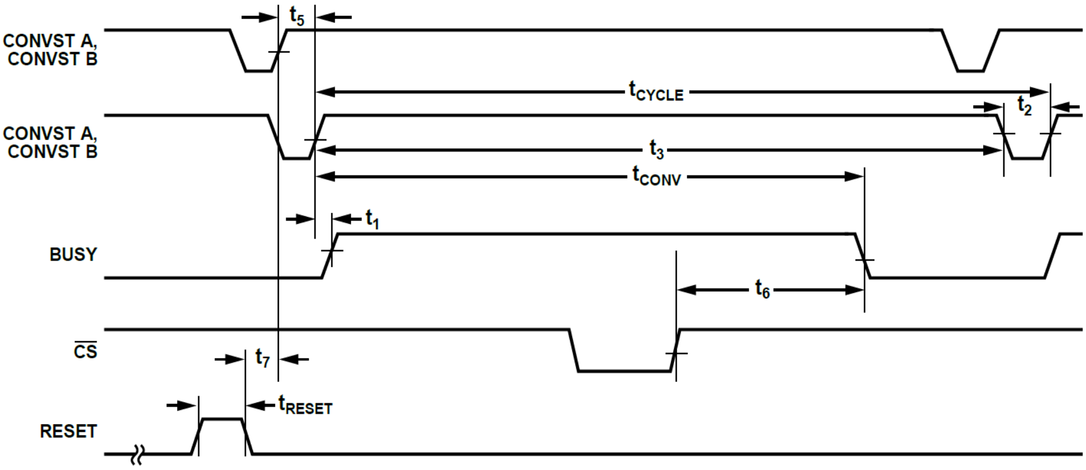


Figure 3. CONVST x Timing—Reading During a Conversion

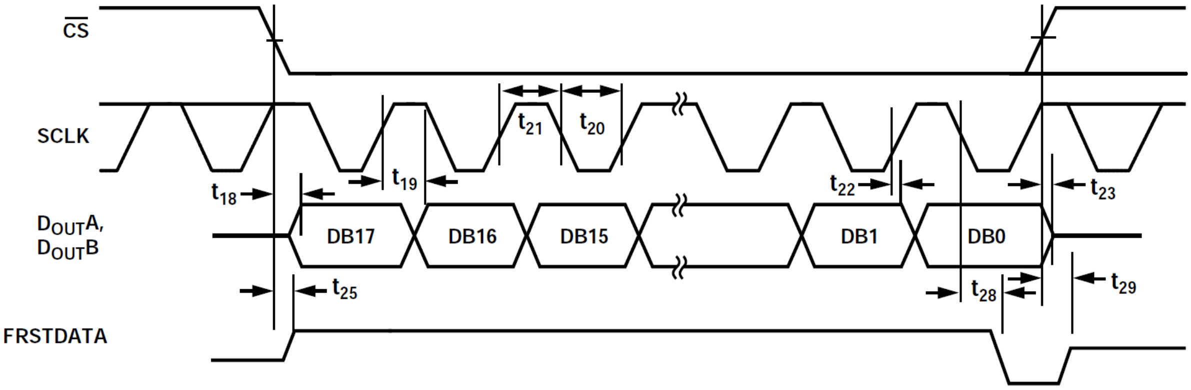
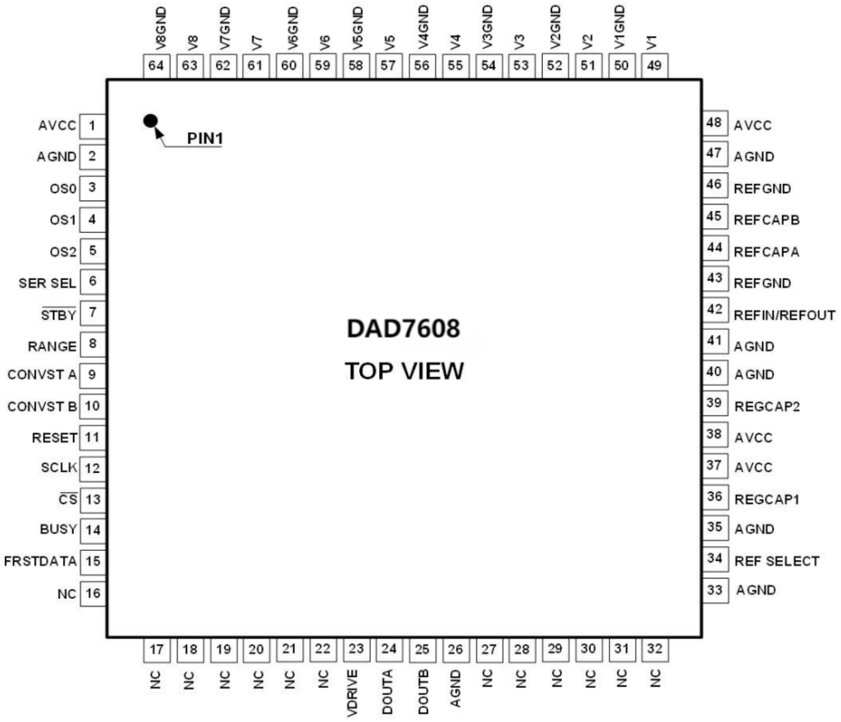


Figure 4. Serial Read Operation (channel 1)



PIN CONFIGURATION

Figure 5 Pin Configuration

Table 1. Pin Function Descriptions

Pin		Type	Description
Name	Pin No.		
AGND	2, 26, 35, 40, 41, 47	P	Analog Ground.
V1GND	50	AI	Analog Input Channel 1: Negative Input.
V1P	49	AI	Analog Input Channel 1: Positive Input.
V2GND	52	AI	Analog Input Channel 2: Negative Input.
V2P	51	AI	Analog Input Channel 2: Positive Input.
V3GND	54	AI	Analog Input Channel 3: Negative Input.
V3P	53	AI	Analog Input Channel 3: Positive Input.
V4GND	56	AI	Analog Input Channel 4: Negative Input.
V4P	55	AI	Analog Input Channel 4: Positive Input.
V5GND	58	AI	Analog Input Channel 5: Negative Input.
V5P	57	AI	Analog Input Channel 5: Positive Input.
V6GND	60	AI	Analog Input Channel 6: Negative Input.
V6P	59	AI	Analog Input Channel 6: Positive Input.
V7GND	62	AI	Analog Input Channel 7: Negative Input.
V7P	61	AI	Analog Input Channel 7: Positive Input.

V8GND	64	AI	Analog Input Channel 8: Negative Input.
V8P	63	AI	Analog Input Channel 8: Positive Input.
AVCC	1, 37, 38, 48	P	Analog Supply Voltage. These power pins should be decoupled to AGND.
BUSY	14	DO	Active-high digital output indicating that a conversion is in progress.
CONVSTA	9	DI	Active high logic input controls the start of counting conversion in the first half of the device input channel.
CONVSTB	10	DI	Initiate the conversion of the second half of the device input channel count by actively controlling the logic input.
$\overline{\text{CS}}$	13	DI	Chip select.
NC	16	NC	Disabled.
NC	17	NC	Disabled.
NC	18	NC	Disabled.
NC	19	NC	Disabled.
NC	20	NC	Disabled.
NC	21	NC	Disabled.
NC	22	NC	Disabled.
DOUTA	24	DO	Data output pin.
DOUTB	25	DO	Data output pin.
NC	27	NC	Disabled.
NC	28	NC	Disabled.
NC	29	NC	Disabled.
NC	30	NC	Disabled.
NC	31	NC	Disabled.
NC	32	NC	Disabled.
AGND	33	DI	Analog Ground.
VDRIVE	23	P	Logic Power Supply Input. The voltage (2.3 V to 5.25 V) supplied at this pin determines the operating voltage of the interface.
FRSTDATA	15	DO	Active high digital output, indicating data read from device channel 1.
OS0	3	DI	Oversampling mode pins.
OS1	4	DI	Oversampling mode pins.
OS2	5	DI	Oversampling mode pins.
SER SEL	6	DI	Serial interface select input, active-high logic input.
RANGE	8	DI	Multifunction logic input pin: When the STBY pin is at a high logic level, this pin selects the device′ s input range (±10 V or ±5 V); when the STBY pin is at a low logic level, this pin selects between standby and shutdown modes.
SCLK	12	DI	Clock input pin.
REFCAPA	44	AO	Reference Buffer Output Force/Sense Pins. These pins must be connected together and decoupled to AGND using a low ESR 10 μF ceramic capacitor.
REFCAPB	45	AO	
REFGND	43, 46	P	Reference Ground Pins. These pins should be connected to AGND.
REFIN/ REFOUT	42	AIO	When REFSEL is high, this pin serves as the internal reference output; when REFSEL is low, this pin serves as the external reference input. Use a 10 μF capacitor on pin 43 to decouple it to REFGND.
REFSEL	34	DI	Internal/External Reference Selection Input. Logic input.
REGCAP1	36	AO	Decoupling Capacitor Pin 1 for Voltage Output from Internal Regulator. These output pins should be decoupled separately to AGND using a 1 μF capacitor.
REGCAP2	39	AO	Decoupling Capacitor Pin 2 for Voltage Output from Internal Regulator. These output pins should be decoupled separately to AGND using a 1 μF capacitor.
RESET	11	DI	Active-high logic input, reset device digital logic.
$\overline{\text{STBY}}$	7	DI	Active-low logic input enables the device to enter one of two power-off modes: standby or shutdown.

ELABORATE

Converter Details

The DAD7608 is a data acquisition system featuring a high-speed, low-power, charge redistribution successive approximation analog-to-digital converter (ADC) with 8 simultaneous analog input channels. It supports true bipolar input signals and offers two input range options: ±10 V or ±5 V. Powered by a single 5V supply, the device incorporates built-in protection mechanisms including input clamping, signal scaling amplifiers, second-order anti-aliasing filters, track-and-hold amplifiers, an on-chip reference voltage source, reference voltage buffers, a high-speed ADC, digital filters, and a high-speed serial interface. Sampling operations are controlled by the CONVST signal.

ANALOG INPUT

Analog Input Range

The DAD7608 supports true bipolar, single-ended input voltages. The logic level at the RANGE pin determines the analog input range for all channels. When connected to a high logic level, all channels operate within ±10V. At a low logic level, the range is set to ±5V.

While the pin's logic state directly affects the input range, the device also requires approximately 80μs of setup time beyond standard acquisition time. For optimal performance, the RANGE pin should be hardwired according to the system's required input range specifications.

During normal operation, the applied analog input voltage must remain within the range selected by the RANGE pin. A RESET pulse must be applied upon power-on to ensure the analog input channel is configured to the selected range. When powering down, it is recommended to connect the analog input to GND. According to the analog input clamp protection section, overvoltage clamp protection is recommended for transient overvoltage conditions but should not remain effective for extended periods. It is emphasized that analog inputs operating outside these specified conditions may reduce the DAD7608′ s bipolar zero code error and THD performance.

Analog Input Impedance

The DAD7608 features a fixed analog input impedance of 1MΩ, which remains constant regardless of its sampling frequency. This high impedance eliminates the need for a driver amplifier preceding the DAD7608, enabling direct connection to signal sources or sensors. Furthermore, the absence of a driver amplifier allows the bipolar power supply (typically a noise source in the system) to be removed from the signal chain.

Analog Input Clamp Protection

Figure 8 illustrates the analog input architecture of the DAD7608. Each analog input features a clamping protection circuit. Although powered by a single 5V supply, this clamping protection enables input overvoltages up to ±16.5 V.

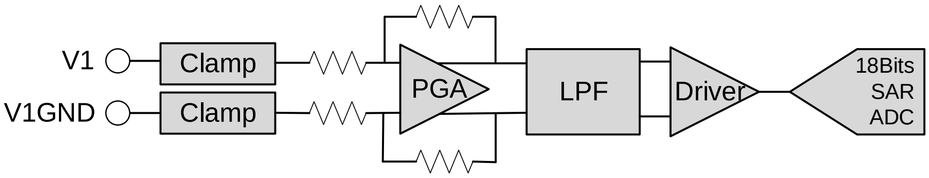


Figure 8: Analog input circuitry

Figure 9 shows the voltage and current characteristics of the clamping circuit. When the input voltage does not exceed ±16.5 V, no current flows through the clamping circuit. For input voltages above ±16.5 V, the DAD7608 clamping circuit is activated.

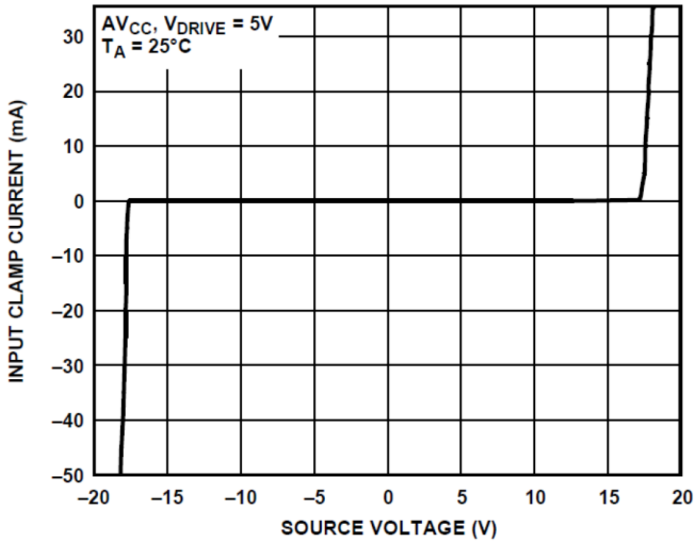


Figure 9 Input Protection Clamp Profile

A series resistor should be placed on the analog input channel to limit current to ±10 mA when the input voltage exceeds ±16.5V. When a series resistor is connected on the analog input channel Vx, a corresponding resistor must be placed on the analog input GND channel VxGND (see Figure 10). Failure to connect the resistor on VxGND will cause offset errors in this channel. It is recommended to implement an input overvoltage clamping protection circuit to shield the DAD7608 from transient overvoltage events. Leaving the DAD7608 in an active state during normal or prolonged power outages is not advisable, as this may degrade its bipolar zero-code error performance.

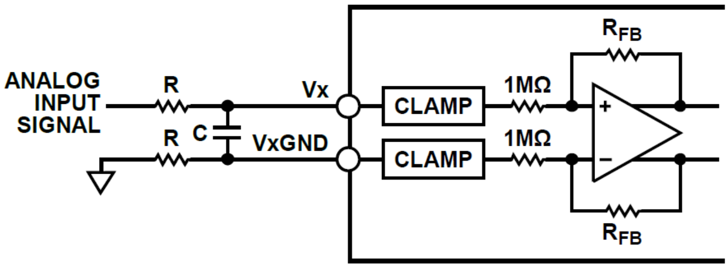


Figure 10 Input resistance matching on the analog input

Analog Input Antialiasing Filter

The DAD7608 also features an analog antialiasing filter. The −3 dB frequency is typically 15 kHz at ±5 V and 43 kHz at ±10 V.

ADC Transfer Function

The DAD7608 employs two's complement encoding for its output. The code conversion is designed to occur between consecutive integer Least Significant Bit (LSB) values, specifically between 1/2 LSB and 3/2 LSB. With an LSB width of FSR/262,144, the DAD7608′ s ideal transfer characteristics are illustrated in Figure 11. The LSB width is determined by the selected analog input range.

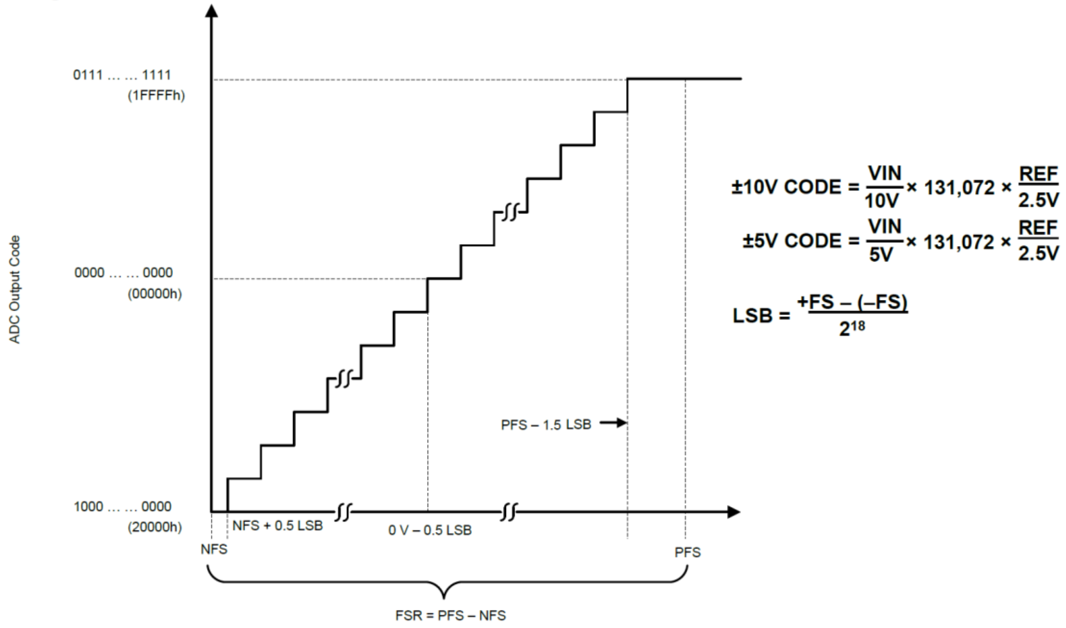


Figure 11 Transfer characteristics

	+FS	MIDSCALE	−FS	LSB
±10V RANGE	+10V	0V	−10V	76.29µV
±5V RANGE	+5V	0V	−5V	38.15µV

Internal/External Reference

The DAD7608 features an on-chip 2.5V band gap reference. The REFIN/REFOUT pins provide two options: either generate an internal 4.0V reference from the 2.5V band gap or connect an external 2.5V reference to the DAD7608. When using an external 2.5V reference, the internal buffer can boost the voltage to 4.0V. This 4.0V buffered reference serves as the operational reference for the SAR ADC.

The REF SELECT pin functions as a logic input pin that allows users to choose between internal and external references. When set to logic high, the internal reference is selected and enabled. If the pin is set to logic low, the internal reference is disabled, requiring an external reference voltage to be applied to the REFIN/REFOUT pins. The internal reference buffer remains active. After reset, the DAD7608 operates on the REF SELECT pin configured for reference mode. Both internal and external reference options require decoupling. A 10μF ceramic capacitor must be connected to the REFIN/REFOUT pins. The DAD7608 includes a reference buffer that boosts the REF voltage to approximately 4.0V (as shown in Figure 12). The REFCAPA and REFCAPB pins must be externally shorted together, with a 10μF ceramic capacitor connected to REFGND to ensure the reference buffer operates in closed-loop mode. The reference voltage for the REFIN/REFOUT pins is 2.5V.

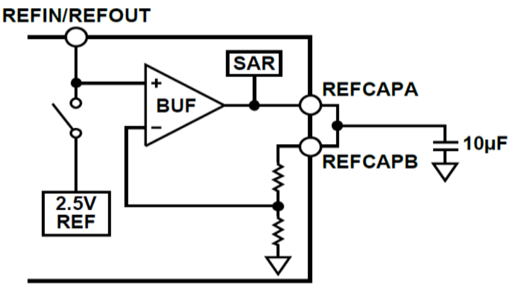


Figure 12 Reference circuitry

When configured in external reference mode, the REFIN/REFOUT pin has high input impedance. For applications with multiple DAD7608 devices, the following configuration is recommended based on specific requirements.

External Reference Mode

An external reference can drive one or more REFIN/REFOUT pins of the DAD7608 chip. In this configuration, each REFIN/REFOUT pin of the DAD7608 should be decoupled with at least 100nf decoupling capacitors.

Internal Reference Mode

A DAD7608 device configured in internal reference mode can drive other DAD7608 devices operating in external reference mode. For DAD7608 in internal reference mode, the REFIN/REFOUT pins should be decoupled using a 10μF ceramic capacitor. Other DAD7608 devices in external reference mode require at least a 100nf decoupling capacitor on their REFIN/REFOUT pins.

Typical Connection Diagram

Single-end connection mode:

Figure 13 illustrates the typical schematic of the DAD7608. The device features four AVCC power pins, each requiring decoupling with a 100 nF capacitor at the pin and a 10μF capacitor on the power supply. The DAD7608can operate with either an internal reference or external application reference. In this configuration, the device is set to work with the internal reference. When using a single DAD7608 on the board, the REFIN/REFOUT pins should be decoupled with a 10μF capacitor. For applications involving multiple DAD7608 devices, refer to the internal/external reference section. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10μF ceramic capacitor. The VDRIVE power is connected to the same supply as the processor, controlling the logic signal voltage. For layout, decoupling, and grounding guidelines, consult the Layout Guide section. After powering the DAD7608, apply a reset signal to ensure it operates in the correct configuration mode.

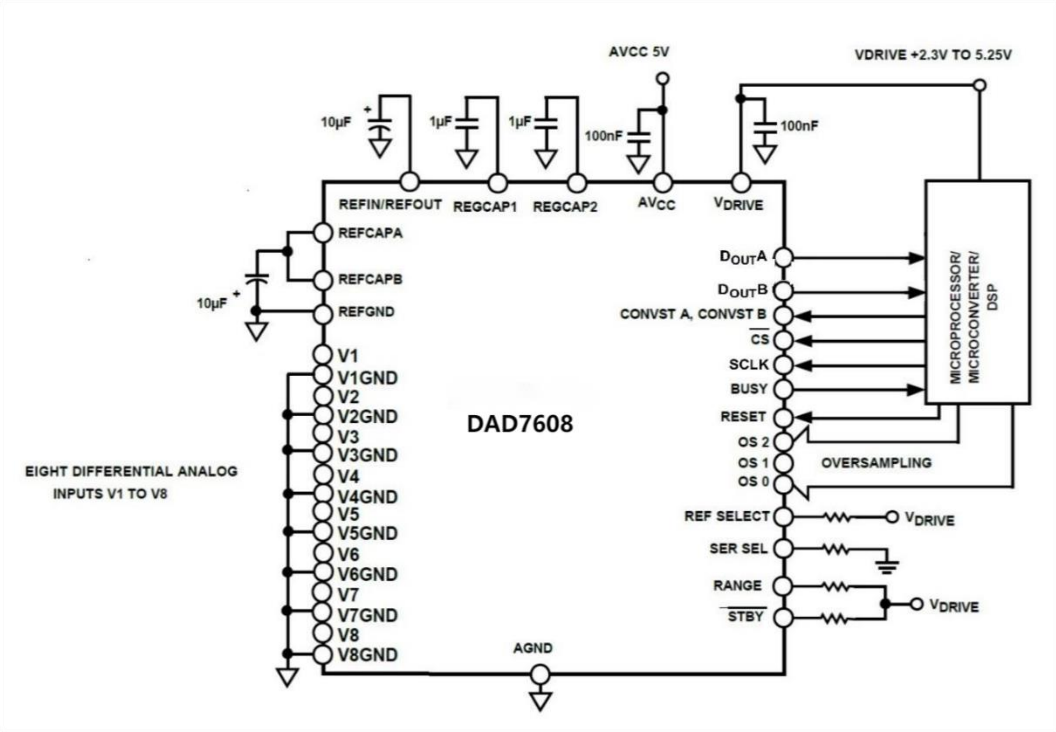


Figure 13 Typical single-ended input connection diagram

Differential connection mode

The DAD7608 also supports differential input mode, with the typical connection diagram shown below:

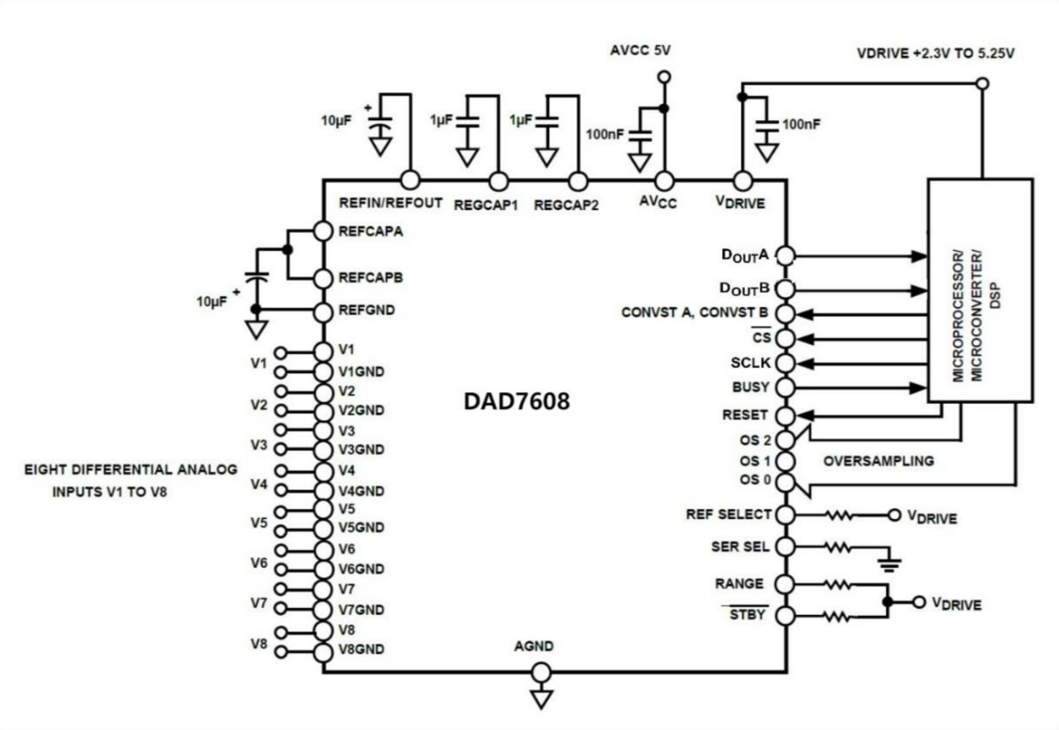


Figure 14 Typical differential input connection diagram

Figure 15 shows the differential input signal. Vx is the same-direction analog input terminal, and VxGND is the reverse analog input terminal. The differential input voltage ranges are 10Vpp and 20Vpp respectively. The common-mode voltage is 0-5V.

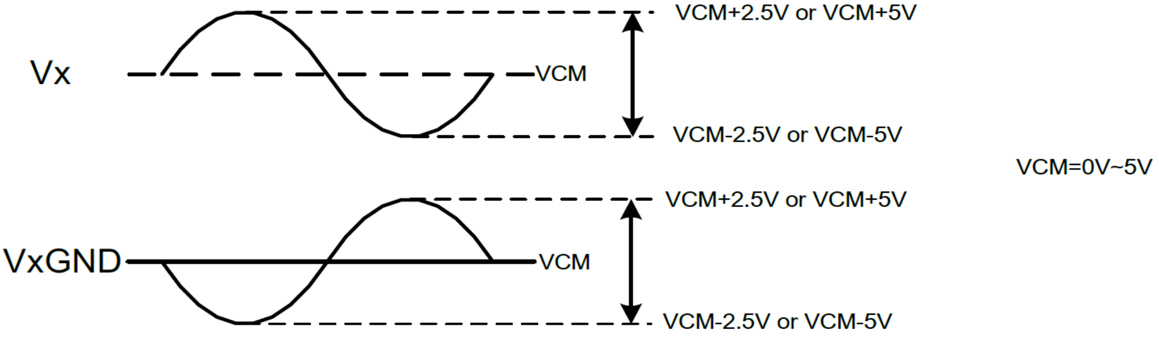


Figure 15 Differential signal input waveform

Power-Down Mode

The DAD7608 features two power-down modes: standby and shutdown. The STBY pin controls whether the device remains in normal operation or switches between these modes. When the STBY pin is low, the RANGE pin's status determines the power-down mode. Table 6 outlines the configuration settings required for each mode. During standby mode, the maximum current consumption is 7mA as the capacitors on REFCAPA and REFCAPB pins need to be charged, with a power-on duration of approximately 100µs. In this state, the on-chip reference and voltage regulator remain powered, while the amplifier and ADC core are powered down.

Table 6. Power-down mode selection

Power-down mode	STBY	RANGE
Standby	0	1
Shutdown	0	0

When the DAD7608 is in shutdown mode, its maximum current consumption is 6 mA, with a power-up time of approximately 13 ms (external reference mode). All circuits are deactivated during shutdown. Upon power-up from shutdown mode, the DAD7608 must receive a RESET signal after the specified power-up duration.

CONVERSION CONTROL

Simultaneous Sampling on All Analog Input Channels

The DAD7608 supports simultaneous sampling of all analog input channels. When the two CONVST pins (CONVST A and CONVST B) are connected, all channels are sampled concurrently. A single CONVST signal controls both CONVST x inputs. The rising edge of this standard CONVST signal initiates synchronized sampling across all analog input channels (V1 to V8 of the DAD7608). The device incorporates an on-chip oscillator for conversion execution, with all ADC channels sharing a common conversion time (tCONV). During conversion, the BUSY signal alerts users: when the CONVST rising edge is applied, the BUSY logic level rises while the conversion value drops upon completion. The BUSY falling edge also signals readiness for new data reading from the DOUTA and DOUTB serial data lines.

Simultaneously Sampling Two Sets of Channels

The DAD7608 also enables simultaneous sampling of two sets of analog input channels. This feature is utilized in power line protection and measurement systems to compensate for phase differences introduced by PT and CT transformers. In 50Hz systems, it allows up to 9° phase compensation; in 60Hz systems, it enables up to 10° phase compensation. This is achieved through separate pulses to two CONVST pins, which is only possible without oversampling. CONVST A initiates simultaneous sampling for the first group of channels (V1 to V4 of the DAD7608), while CONVST B triggers synchronous sampling for the second group of analog input channels (V5 to V8 of the DAD7608), as shown in Figure 16. The conversion process begins when the rising edges of both CONVST x signals occur, causing BUSY to rise on the subsequent CONVST x edge. In Table 3, Time t5 represents the maximum allowable time between CONVST x sampling points. The data read process remains unchanged when using two separate CONVST x signals. Connecting all unused analog input channels to AGND still results in data readings, as all channels are always converted.

DIGITAL INTERFACE

The DAD7608 provides a high-speed serial interface.

Serial Interface (SER SEL = 1)

To read data from the DAD7608 via the serial interface, the SER SEL pin must be set to a high level. Data transfer is performed using the CS and SCLK signals. The DAD7608 features two serial data output pins, DOUTA and DOUTB, allowing data reading through either or both DOUT lines. For the DAD7608, conversion results from channel V1 to V4 are first output on DOUTA, while those from channel V5 to V8 appear first on DOUTB.

The falling edge of CS pulls the data output lines DOUTA and DOUTB out of their three-state configuration, recording the MSB of the conversion result. During the rising edge of SCLK, all subsequent data bits are serially output through DOUTA and DOUTB. The CS input can remain low throughout the serial read operation or be read by each channel in 18 SCLK cycles per pulse frame. Figure 18 illustrates the reading of 8 synchronous conversion results using two DOUT lines on the DAD7608.

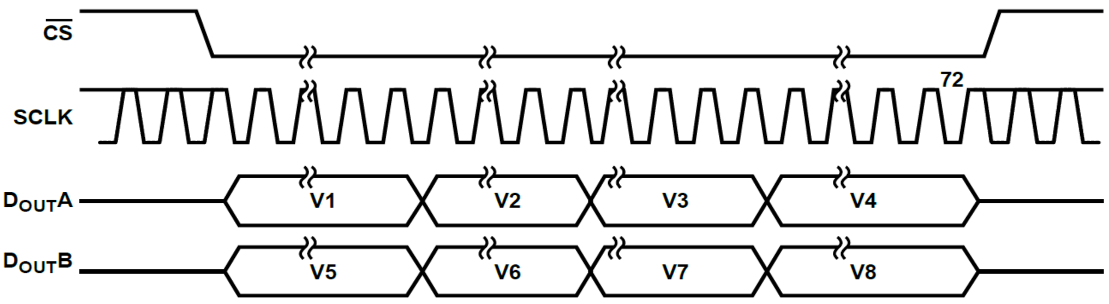


Figure 18 DAD7608 serial interface with dual DOUT lines

In this scenario, a 72 SCLK transfer is employed to access DAD7608 data, with CS maintained at low level to enable all 72 SCLK cycle frames. Alternatively, a single DOUT line may be used for data locking. In this case, it is recommended to utilize DOUTA to access all conversion data, as channel data is output in ascending order: V1, V2, V3, V4, V5, V6, V7, V8. To enable DAD7608 to access all eight conversion results via a single DOUT line, a total of 144 SCLK cycles are required. These 144 SCLK cycles can be framed by a single CS signal, or grouped in 18 SCLK cycles per frame by CS signal. The drawback of using only one DOUT line is reduced throughput when reading data post-conversion. Unused DOUT lines should not be connected in series. For DAD7608, when DOUTB serves as a single-line DOUT, the channel result output sequence is: V5, V6, V7, V8, V1, V2, V3, V4. However, after reading V5 on DOUTB, the FRSTDATA indicator returns to low level.

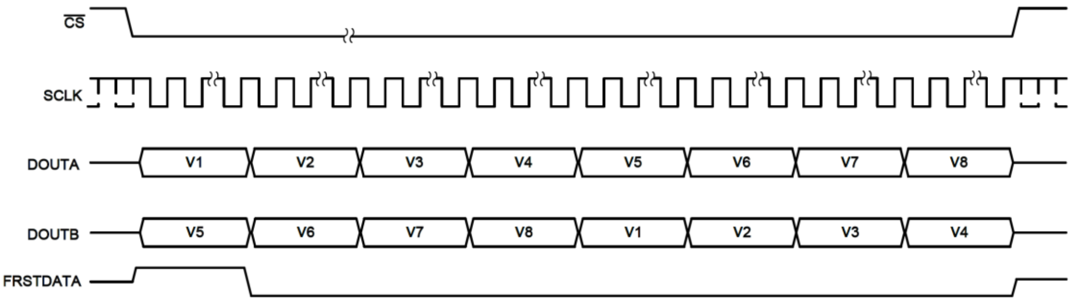


Figure 19 timing diagram of serial data reading from the DAD7608 channel (composed of CS signals)

The SCLK input signal provides the clock source for serial read operations. CS low-level access the DAD7608 data. The CS falling edge deactivates the bus three-state and outputs the MSB of the 18-bit conversion result. This MSB becomes valid on the first falling edge after SCLK's falling edge. The subsequent 17-bit data bits are clocked out by SCLK on the rising edge. Data remains valid during SCLK's falling edge. To access each conversion result, 18 clock cycles must be provided to the DAD7608. The FRSTDATA output signal indicates when the first channel V1 is read back. When CS input is high, the FRSTDATA output pin remains in three-state. In serial mode, the CS falling edge pulls FRSTDATA out of three-state and sets the FRSTDATA pin high, indicating the result from V1 is available on the DOUTA data line. FRSTDATA outputs a logic low level after the 18th SCLK falling edge. If all channels are read on DOUTB, FRSTDATA will not go high when V1 is output on this serial data output pin. It only becomes high when V1 on DOUTA becomes available (which corresponds to V5 on DAD7608′ s DOUTB).

Read During Conversion

When BUSY is high, data can be read from DAD7608 while conversion is in progress. This minimally impacts converter performance and enables faster throughput rates. Serial reads can be performed during conversion or when oversampling is active. Figure 3 illustrates the timing diagram for reading data with BUSY at high level in serial mode. When using VDRIVE serial interfaces above 4.75V, conversion-time reads allow full throughput rates. Data can be read from DAD7608 at any time except during the BUSY deactivation edge, as this is when the output data register is updated with new conversion data. In such cases, the t6 timing requirement specified in Table 3 must be met.

Digital Filter

The DAD7608 features an optional digital first-order sinc filter, ideal for applications requiring lower data rates, higher SNR, or expanded dynamic range. The oversampling ratio is controlled by the OS pins (OS[2:0] in Table 1), where OS2 is the MSB control bit and OS0 is the LSB control bit. Table 8 decodes the oversampling bits to select different rates. The OS pin latch is triggered by the falling edge of the BUSY signal, setting the oversampling rate for the next conversion (see Figure 46). Beyond oversampling, the output is sampled at 18-bit resolution.

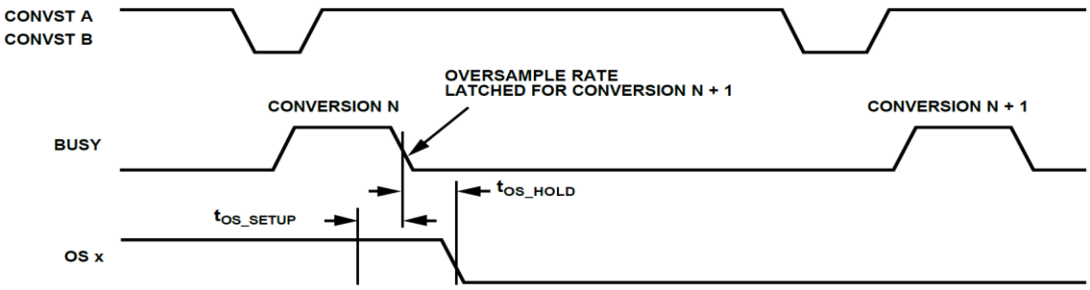


Figure 20 OS x Pin Timing

Table 8 Oversample Bit Decoding

OS[2:0]	OS Ratio	SNR 5 V Range（dB）	SNR 10 V Range（dB）	3 dB BW 5 V Range (kHz)	3 dB BW 10 V Range (kHz)	Maximum Throughput CONVST Frequency (kHz)
000	No OS	88.5	89	15	22	200
001	2	90.3	91	15	22	100
010	4	91.7	92.5	13.7	18.5	50
011	8	93.2	93.4	10.3	11.9	25
100	16	94.8	95	6	6	12.5
101	32	95.1	95.6	3	3	6.25
110	64	95.8	96.1	1.5	1.5	3.125
111	Invalid					

When the OS pin is set to an OS ratio of 8, the next rising edge of the CONVST x signal captures the first sample for each channel, while the remaining seven samples from all channels are sampled using internally generated signals. These samples are then averaged to enhance the signal-to-noise ratio (SNR). Table 8 demonstrates typical SNR performance across ±10 V and ±5 V ranges. As shown in Table 8, the SNR improves with increasing OS ratio. However, higher OS ratios reduce the 3 dB frequency and consequently lower the permissible sampling frequency. In applications requiring 10 kSPS sampling rates, OS ratios up to 16 can be utilized. While this configuration improves SNR, the input 3 dB bandwidth is limited to approximately 6 kHz.

When oversampling is enabled, the pins of CONVST A and CONVST B must be connected or driven together. The conversion process will be extended during the BUSY high-level period. The actual BUSY high-level duration depends on the selected oversampling rate: higher oversampling rates result in longer BUSY high periods or total conversion time.

As shown in Figure 21, the conversion time increases with higher oversampling rates, and the BUSY signal duration also extends under different oversampling conditions. For example, a 10 kSPS sampling frequency generates a 100μs cycle. Figure 47 illustrates

OS × 2 and OS × 4 scenarios. For the 10 kSPS example, sufficient cycle time exists to further increase the oversampling rate, resulting in greater improvements in signal-to-noise ratio performance. In applications with initial sampling or throughput rates of 200 kSPS, enabling oversampling requires reducing the throughput rate to accommodate longer conversion times and allow read operations. To achieve the fastest possible throughput with oversampling enabled, read operations can be performed during the BUSY high-level period. The falling edge of BUSY is used to update the output data register with new conversion data; therefore, reading conversion data should not occur during this edge.

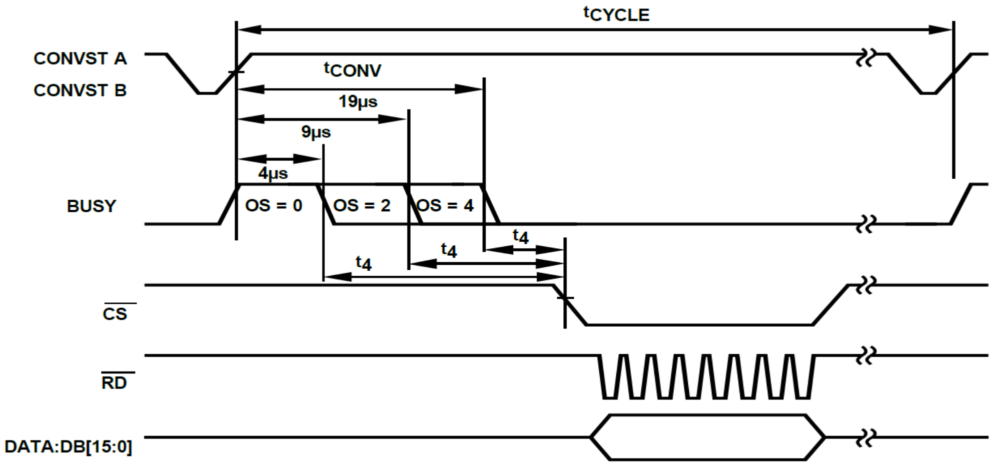


Figure 21 results of no oversampling, 2x oversampling, and 4x oversampling after conversion and reading

Figures 22 to 28 demonstrate how oversampling affects code distribution in the DC histogram. As the oversampling rate increases, code spread decreases. When the DAD7608 selects oversampling mode, it achieves the effect of adding a digital filter after the ADC. Different oversampling rates and CONVST sampling frequencies result in distinct frequency distributions of the digital filter.

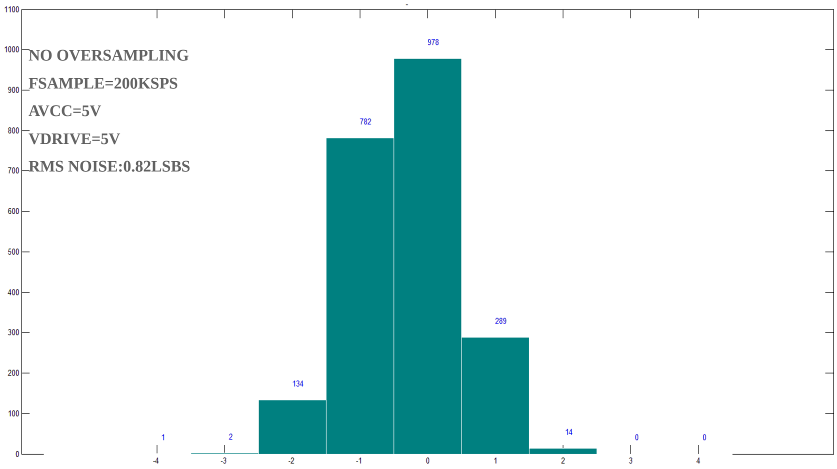


Figure 22. Histogram data-No OS

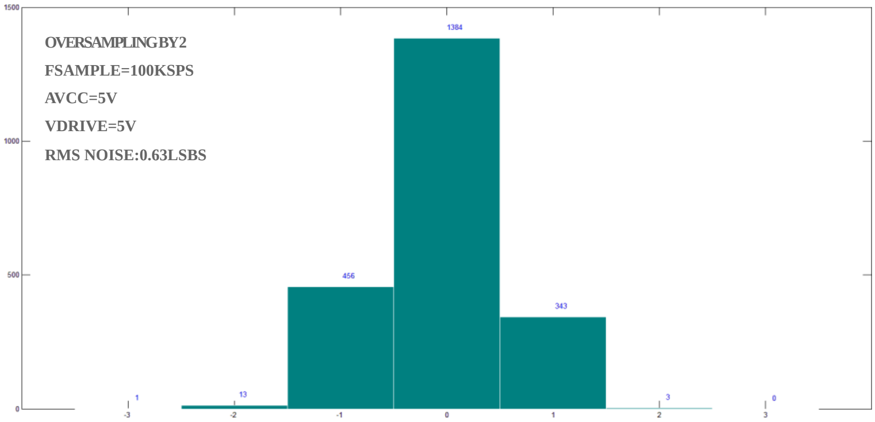


Figure 23. Histogram data—OS × 2

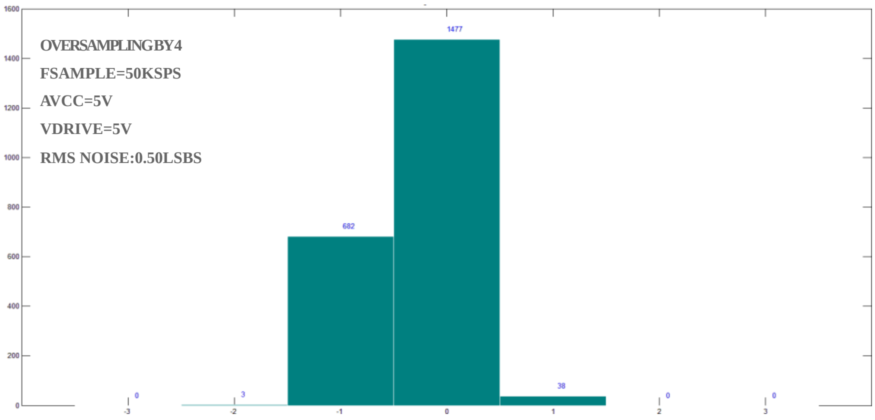


Figure 24. Histogram Data—OS × 4

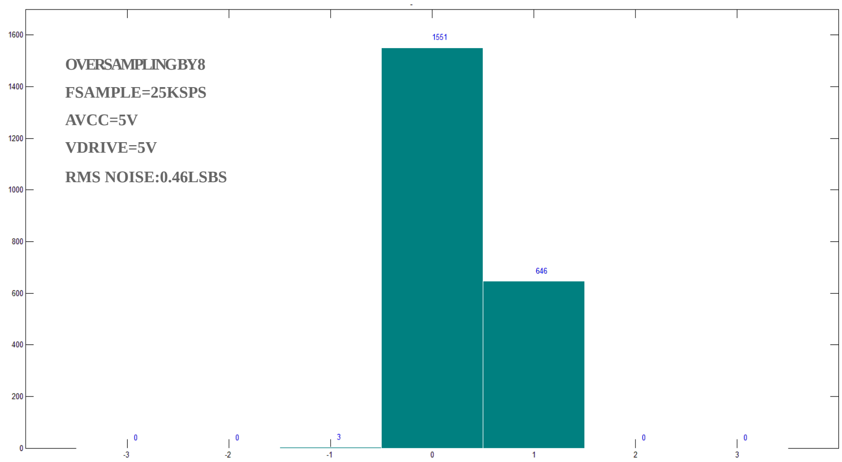


Figure 25. Histogram data—OS × 8

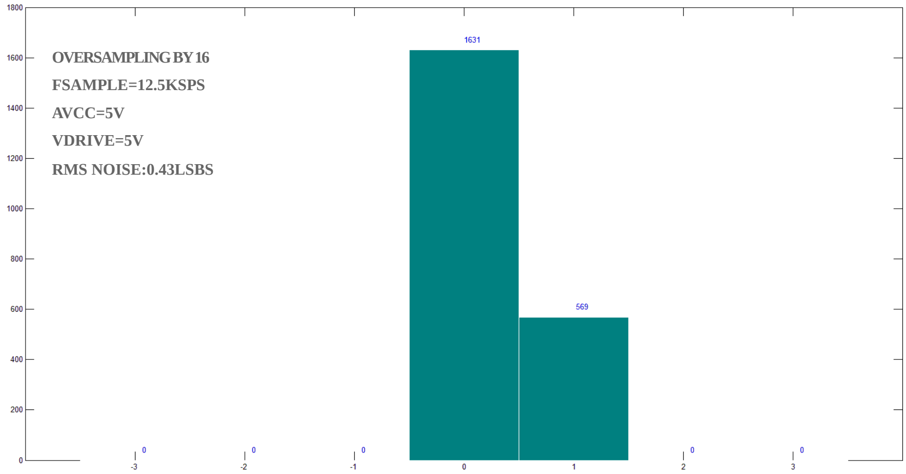


Figure 26. Histogram data—OS × 16

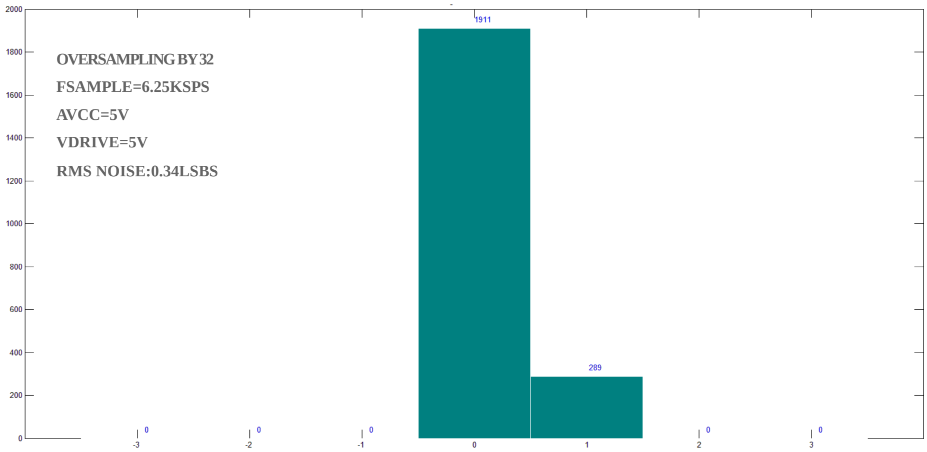


Figure 27. Histogram data—OS × 32

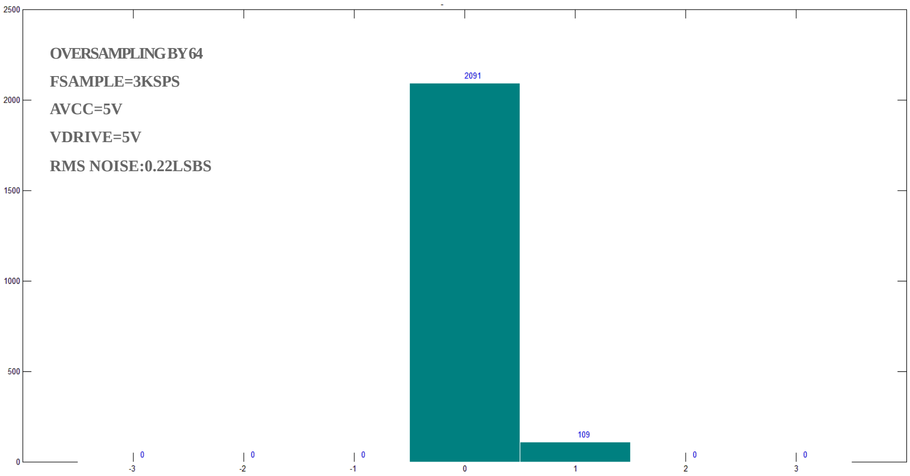


Figure 28 Histogram Data—OS × 64

LAYOUT GUIDELINES

When designing printed circuit boards for DAD7608 applications, analog and digital sections should be physically separated and housed in distinct areas of the board. At least one ground plane must be implemented, which can be either a common ground plane or a dedicated partition between analog and digital zones.

In the case of separate ground planes, both analog and digital ground planes should be connected at a single point—ideally as close as possible to the DAD7608.

Even when the DAD7608 is part of a system requiring analog-digital grounding for multiple devices, a single connection point must still be established: the star ground should be positioned as near the DAD7608 as feasible. Ensure proper connectivity with the ground plane. Avoid sharing a single ground pin across multiple devices. For each ground pin, use dedicated or multiple channels on the ground plane.

Avoid running digital traces beneath analog traces to prevent noise coupling. Analog ground planes should be routed under the DAD7608 to prevent noise coupling. Fast-switching signals like CONVST A, CONVST B, or clock signals should be shielded with digital ground to prevent radiation noise from affecting other board components, and should not run near analog signal paths. Avoid crossing digital and analog signals. Traces on adjacent layers of the board should be routed at right angles to minimize feed-through effects.

The power traces for the AVCC and VDRIVE pins on the DAD7608 should utilize the widest possible paths to ensure low-impedance routing and minimize the impact of minor faults. Where feasible, employ power planes and establish reliable connections between the DAD7608′ s power pins and the board's power traces. Each power pin should be routed through one or more dedicated channels.

Effective decoupling is essential for reducing the DAD7608′ s power supply impedance and minimizing power supply spike amplitudes. Decoupling capacitors should be positioned adjacent to (ideally directly facing) these pins and their corresponding ground pins. Place the decoupling capacitors for the REFIN/REFOUT pins and the REFCAPA and REFCAPB pins as close as possible to their respective DAD7608 pins, and if feasible, integrate them on the same PCB as the DAD7608 device.

Figure 29 illustrates the recommended decoupling configuration for the top layer of the DAD7608 board. Figure 30 demonstrates the bottom-layer decoupling for the four AVCC pins and the VDRIVE pin. The ceramic 100nF caps for the AVCC pins are positioned near their respective device pins, with a 100nF capacitor shared between pins 37 and 38.

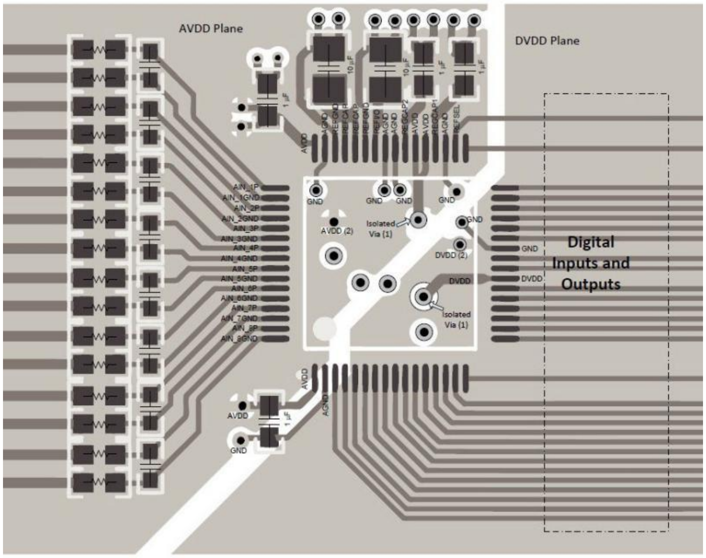


Figure 29 Top-level layout of all pins

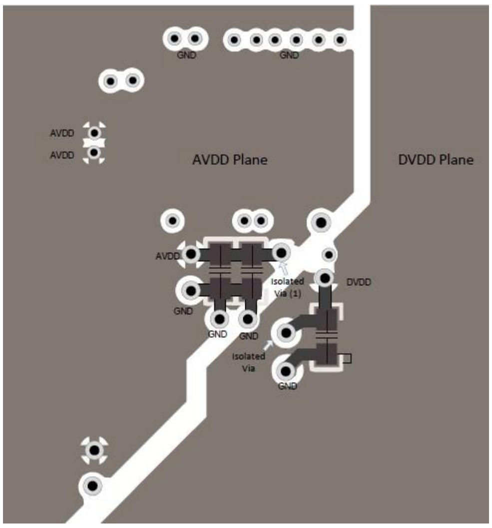


Figure 30: Bottom layer layout

In systems containing multiple DAD7608 devices, maintaining performance consistency between components requires a symmetrical layout. Figure 31 illustrates a configuration with two DAD7608 devices: the AVCC power plane runs along the right side of both devices, while the VDRIVE power rail extends along the left side. The reference chip is positioned between the devices, with its reference voltage rail connecting to pin 42 of U1 (north) and pin 42 of U2 (south), utilizing a solid ground plane. These symmetrical layout principles apply equally to systems with multiple DAD7608 devices. Devices can be arranged in a north-south configuration, with the reference voltage rail positioned between the devices and the respective reference rails running in the north-south direction, as shown in Figure 31.

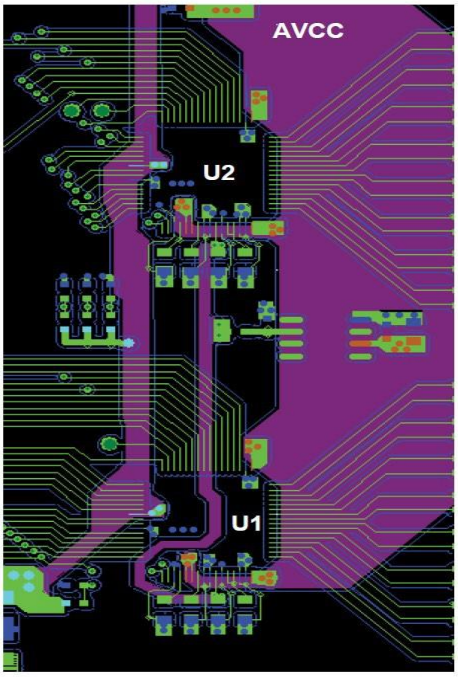
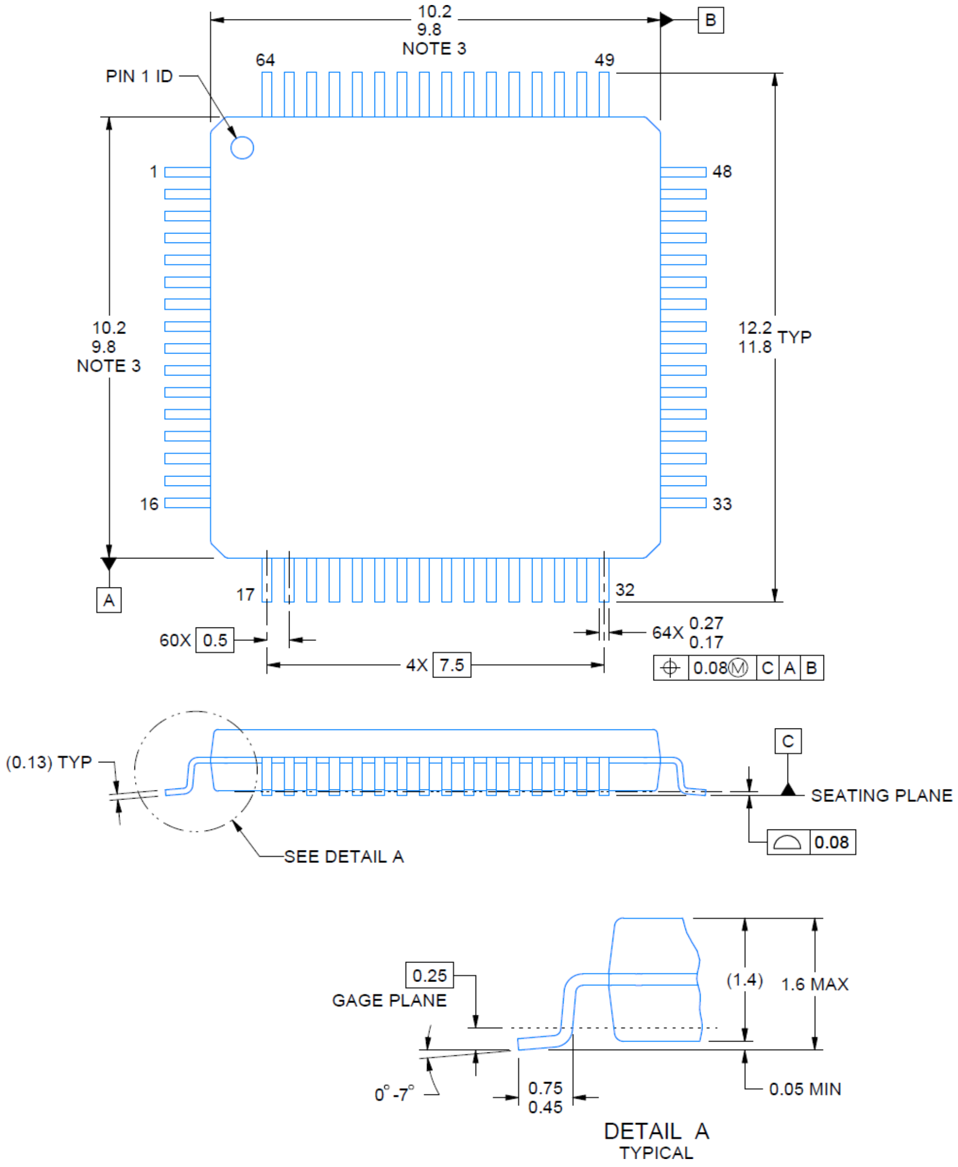
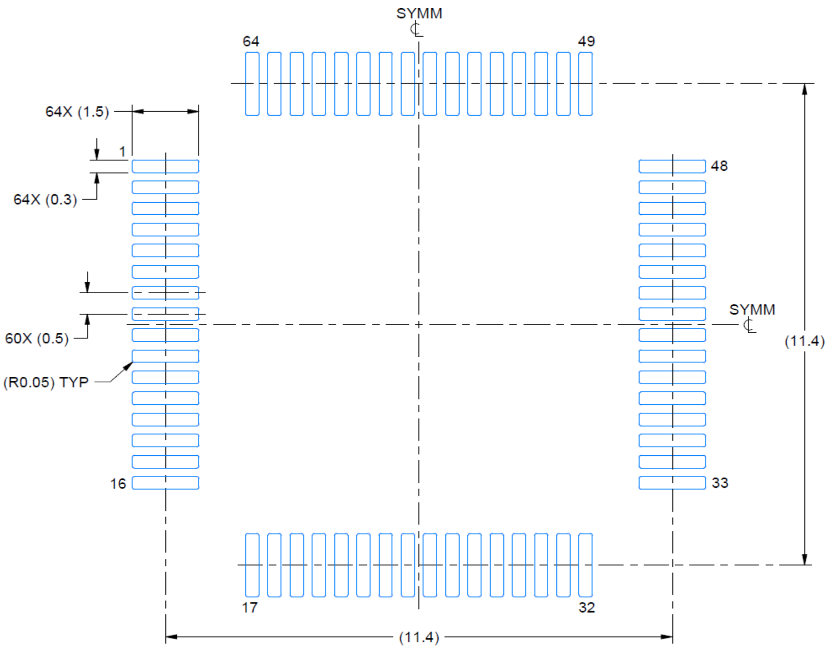


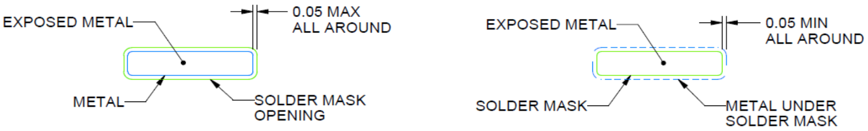
Figure 31 DAD7608 Multi-device Layout: Top layer and supply plane layer

OUTLINE DIMENSION





LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

ORDERING GUIDE

Device Order List

Model	Temperature Range	Package Type	Packing	ROHS
DAD7608-C	A	64-LQFP	960/tray	Y
DAD7608-E	B	64-LQFP	960/tray	Y

Note 1:

Temperature coding information: A for-40℃ to 85℃; B for-40℃ to 125℃; C for-40℃ to 150℃

Package information: REEL, tray, and tray packaging.