

DAC5541TS-5542TS Single-Channel, 16-Bit, Serial-Input Voltage-Output DAC

1. Features

- Full 16-bit performance
- 2.7V to 5.5V single power supply operation
- Low power consumption ($I=250\mu A@12MHz$ SCLK)
- 1 μs stabilization time
- Unbuffered voltage output, output impedance 6.16k Ω
- SPI-/QSPI-/MICROWIRE compatible interface standards
- Power-on reset clears the DAC output to 0V (unipolar mode).
- Low failure rate: 1.5nV-sec

2. Applications

- Digital gain and offset adjustment
- Automated testing equipment
- Data acquisition system
- Industrial process control

3. Overview

The DAC5541TS-5542TS is a single 16-bit serial input voltage-output digital-to-analog converter (DAC) operating from 2.7V

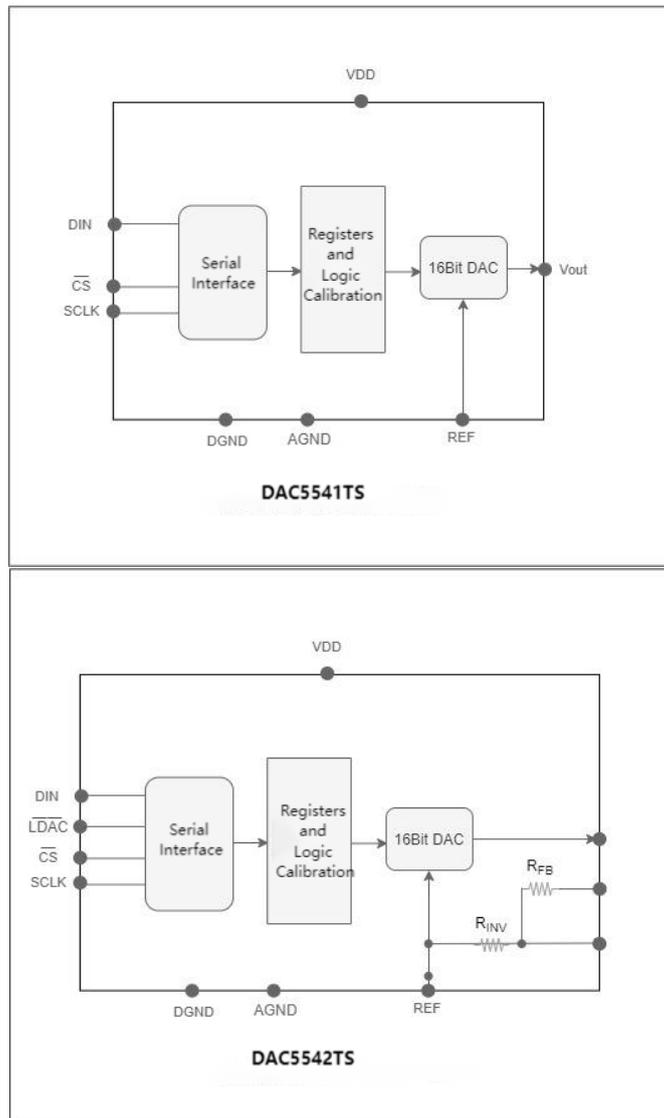
to 5.5V. The DAC output range extends from 0V to VREF. The DAC provides 16-bit 1LSB INL accuracy without the need for adjustment over the entire specified temperature range of -40°C to +85°C/105°C. Providing unbuffered output, the DAC5541TS-5542TS achieves a 1 μs settling time with low power consumption and low offset error. The DAC5541TS-5542TS features low noise performance and low failure rate, making it suitable for deployment across multiple end systems.

The DAC5542TS can operate in bipolar mode, producing $\pm VREF$ output oscillation. The DAC5541TS-5542TS features a versatile 3-wire interface, compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards. The DAC5541TS-5542TS is available in 8-lead SOP8L and 14-lead SOP14L packages.

4. Equipment Information

Device Model	Packaging	Package Size (nominal value)
DAC5541TS	SOP8L	5.0 mm × 4.0 mm
DAC5542TS	SOP14L	8.5 mm × 4.0 mm

5. Functional Block Diagram



6. Pin Configuration and Functions

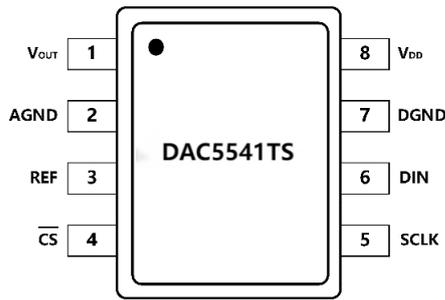


Figure 2. Pin diagram of SOP8L (DAC5541TS)

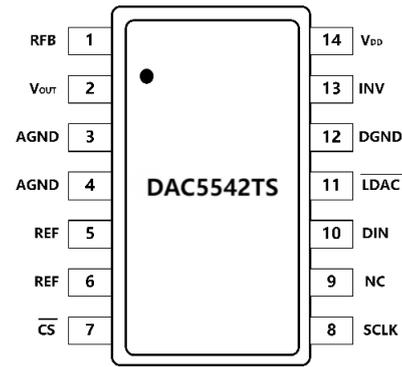


Figure 3. Pin diagram of SOP14L (DAC5542TS)

SOP8L (DAC5541TS) Pin Functions

Name	No.	Function	Description
V _{OUT}	1	Output	Analog output voltage of DAC
AGND	2	Ground	Ground reference point of analog circuit
REF	3	Input	The DAC's voltage reference input. The reference voltage range is 2.5V to V _{DD} .
\overline{CS}	4	Input	Logic input signals and chip select signals are used to frame serial data input.
SCLK	5	Input	Clock input: Data is recorded by the clock into the input register at the rising edge of SCLK. The duty cycle must be between 40% and 60%.
DIN	6	Input	Serial data input : This device accepts 16-bit words , and the data is recorded into the input register on the rising edge of SCLK by the clock.
DGND	7	Ground	Digital circuit ground reference point
V _{DD}	8	Power supply	Analog power supply voltage

SOP14L (DAC5542TS) Pin Functions

Name	No.	Function	Description
RFB	1	Input/Output	In bipolar mode, connect the feedback resistor pin to the output of an external operational amplifier.
V _{OUT}	2	Output	Analog output voltage of DAC
AGND	3	Ground	Ground reference point of analog circuit
AGND	4	Ground	Ground reference point of analog circuit
REF	5	Input	The DAC's voltage reference input has a reference voltage range of 2.5V to V _{DD} .
REF	6	Input	The DAC's voltage reference input has a reference voltage range of 2.5V to V _{DD} .
\overline{CS}	7	Input	Logic input signals and chip select signals are used to frame serial data input.
SCLK	8	Input	Clock input : Data is recorded by the clock into the input register at the rising edge of SCLK . The duty cycle must be between 40% and 60%.
NC	9	null	No connection
DIN	10	Input	For serial data input , the device accepts 16-bit words , and the data is clocked into the input register on the rising edge of SCLK.
\overline{LDAC}	11	Input	The \overline{LDAC} input , when this input is low, simultaneously updates the DAC register with the contents of the input register.
DGND	12	Ground	Digital circuit ground reference point
INV	13	Input/Output	Connect the internal scaling resistor to the DAC . In bipolar mode, connect the INV pin to the inverting input of the external operational amplifier.
V _{DD}	14	Power supply	Analog power supply voltage

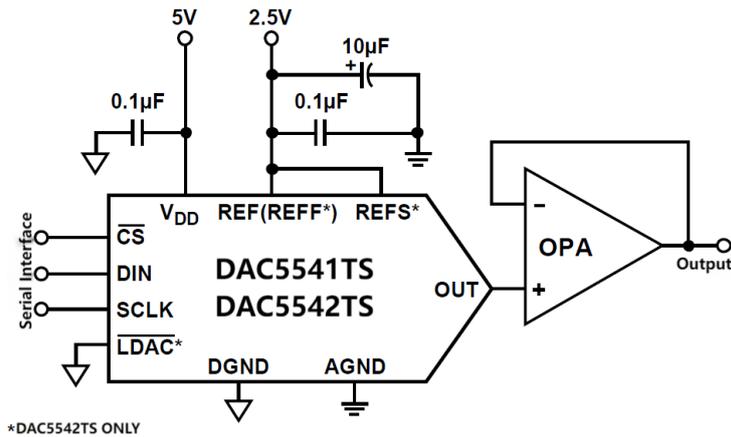
7. Typical Application Circuits


Figure 4. Single-stage output connection

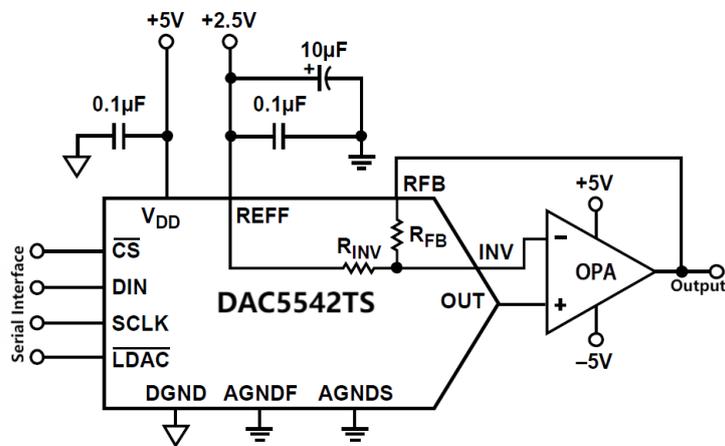


Figure 5. Two-stage output connection

8. Absolute maximum rating

(TA = 25°C, unless otherwise specified.)

Parameter	Symbol	Range	Unit
Power supply voltage relative to ground	V _{DDabs}	-0.3 to +6	V
Digital input voltage relative to ground	V _{Digabs}	-0.3 to V _{DD} + 0.3	V
Analog output voltage relative to ground	V _{outabs}	-0.3 to V _{DD} + 0.3	V
Analog relative to digital		-0.3 to +0.3	V
Input current of any pin other than the power supply		±10	mA
Temperature range			
DAC5541TSC, DAC5542TSC	T _P	-40°C to +85°C	
DAC5541TSH, DAC5542TSH		-40°C to +105°C	
Storage temperature range	T _S	-65°C to +150°C	°C
Junction temperature	T _{Jmax}	150°C	°C
ESD characteristics			
Peak temperature		260°C	V
ESD: HBM		4000V	V
ESD: CDM		1000V	V
SOP8L package			
θJA thermal resistance		121°C/W to 202°C/W	°C/W

The stresses listed below, exceeding the absolute maximum ratings, may cause permanent damage to the equipment. This is only a pressure rating; it does not imply functional operation of the equipment under any other conditions above these or those shown in the Operating section of this specification. Prolonged exposure to absolute maximum ratings may affect the reliability of the equipment.

DAC5541TS-5542TS Single-Channel, 16-Bit, Serial-Input Voltage-Output DAC

9. Specifications

$V_{DD} = 2.7V$ to $5.5V$, $2.5V \leq V_{REF} \leq V_{DD}$, $AGND = DGND = 0V$. Unless otherwise specified, all specifications $T_A = T_{MIN}$ to T_{MAX} .

Parameter ¹	Symbol	Test conditions	Min	Typ	Max	Unit
Static Performance						
Resolution			16			Bits
Relative accuracy	INL	C and H grades		±0.5	±1.0	LSB
Differential nonlinearity	DNL	C and H grades		±0.5	±1.0	LSB
Gain error		$T_A = 25^\circ C$		0.5	±2	LSB
Gain error temperature coefficient				±0.13		LSB
Unipolar zero code error		$T_A = 25^\circ C$		±0.3	±0.7	LSB
DAC5542TS						
Bipolar resistor matching		R_{FB}/R_{INV} , typical $R_{FB} = R_{INV} = 28k\Omega$		1		Ω/Ω
		Ratio difference		±0.02		%
Bipolar zero code error		$T_A = 25^\circ C$		±1	±5	LSB
Bipolar gain error		$T_A = 25^\circ C$		1	±5	LSB
Output Characteristics						
Output voltage range		Unipolar operation	0		$V_{REF} - 1LSB$	V
		DAC5542TS Bipolar Operation	$-V_{REF}$		$V_{REF} - 1LSB$	V
Output voltage settling time		To 1/2 LSB of FS, $C_L = 10pF$		1		μs
Slope		$C_L = 10pF$, from 0% to 63%		20		V/ μs
Digital-to-analog conversion fault pulse		Changes around the 1LSB primary vehicle		1.5		nV-sec
Digital feedthrough		All 1s loaded to DAC, $V_{REF} = 2.5V$		0.2		nV-sec
DAC output impedance		The tolerance is usually 20%.		6.16		k Ω
Output noise spectral density ³		Code = 0x8400, Frequency = 1kHz		11.8		nV/ \sqrt{Hz}
Output noise ³		0.1Hz to 10Hz		0.134		$\mu VP-P$
Power supply rejection ratio		$\Delta V_{DD} \pm 10\%$			±1.0	LSB
DAC Reference Input						
Reference input range			2.5		V_{DD}	V
Reference input resistor ²		Unipolar operation	7			k Ω
		DAC5542TS Bipolar Operation	6.5			k Ω
Logical Input						
Input current					±1	μA
Low input voltage	V_{INL}				0.8	V
Input high voltage	V_{INH}	$V_{DD} = 2.7V$	$70\% * V_{DD}$			V
		$V_{DD} = 5V$	3			V
Input capacity ³					10	pF
Lag voltage ³				0.15		V
Reference³						
Reference -3dB bandwidth		All loaded in 1 second		2.23		MHz
Reference feedthrough		All 0s loaded, $V_{REF} = 1V_{PP}$ at 100kHz		1		mV _{PP}
Signal-to-noise ratio				92		dB
Reference input capacitor		Code 0x0000		35.2		pF
		Code 0xFFFF		26.6		pF
Power Requirements						
V_{DD}		The V_{DD} ramp-up conversion rate must be less than 5V/1 μs .	2.7		5.5	V
I_{DD}		SCLK=12MHz		250	3 00	μA
Power consumption		$V_{DD} = 5V$		1.25	1.5	mW

- The temperature range is $-40^\circ C$ to $+85^\circ C$ (DAC5541TSC, DAC5542TSC) or $-40^\circ C$ to $+105^\circ C$ (DAC5541TSH, DAC5542TSH).
- The reference input resistor depends on the code, with a minimum value of 0x8555.
- Design-guaranteed, no production testing is required.

10. Timing characteristics

DAC5541TS-5542TS Single-Channel, 16-Bit, Serial-Input Voltage-Output DAC

$V_{DD} = 2.7V$ to $5.5V \pm 10\%$, $V_{REF} = 2.5V$, $V_{INH} = 3V$ and 90% of V_{DD} , $V_{INL} = 0V$ and 10% of V_{DD} , $AGND = DGND = 0V$; $-40^{\circ}C < T_A < +85^{\circ}C$, unless otherwise specified.

Parameters ^{1 and 2}	Limit	Unit	Description
f _{SCLK}	25	MHz max	SCLK cycle frequency
t ₁	40	ns min	SCLK cycle time
t ₂	20	ns min	SCLK high time
t ₃	20	ns min	SCLK low time
t ₄	10	ns min	\overline{CS} low to SCLK high setup
t ₅	15	ns min	\overline{CS} high to SCLK high setup
t ₆	30	ns min	SCLK high to \overline{CS} low hold time
t ₇	20	ns min	SCLK high to \overline{CS} high hold time
t ₈	15	ns min	Data setup time
t ₉	10	ns min	Data hold time
t ₁₀	30	ns min	\overline{LDAC} pulse width
t ₁₁	30	ns min	\overline{CS} high to \overline{LDAC} low setup
t ₁₂	30	ns min	\overline{CS} high time between active periods

1. Guaranteed by design and features. No production testing conducted.
2. All input signals are specified as $t_R = t_F = 1ns/V$, and timing begins from the voltage level of $(V_{INL} + V_{INH})/2$.

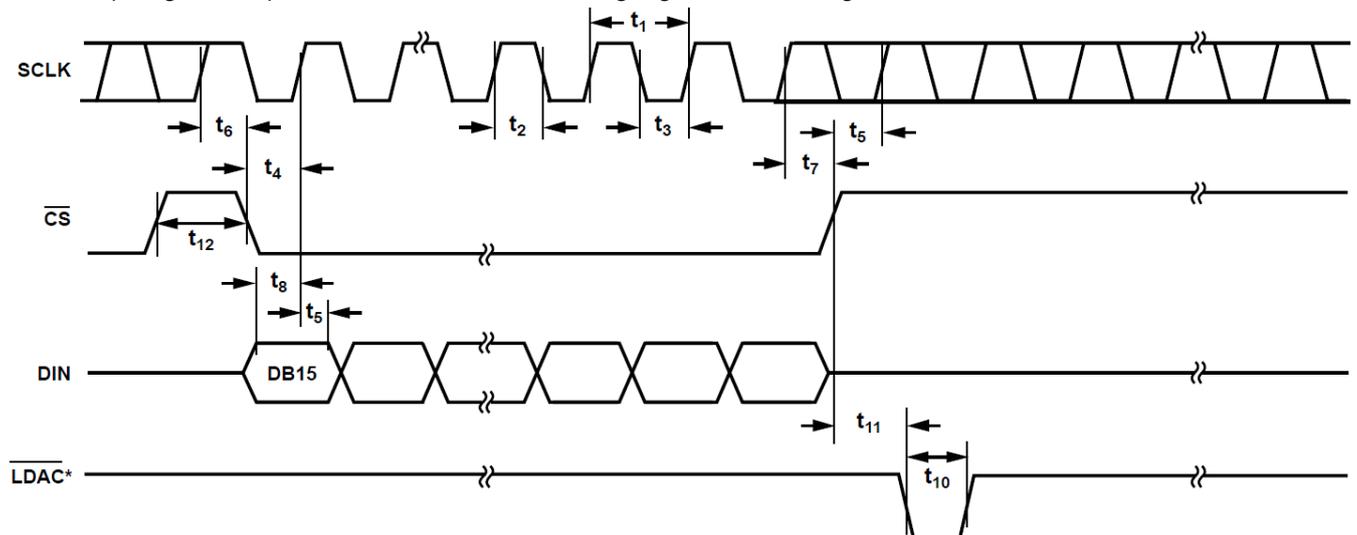


Figure 6. Timing Diagram

*DAC5542TS only. It can be permanently bound low if needed.

11. Theory of operation

- **Function Description**

The DAC5541TS-5542TS are single 16-bit serial input voltage-output DACs. They are powered by a single supply from 2.7V to 5.5V. Data is written to these devices in 16-bit word format via a 3-wire or 4-wire serial interface. To ensure known power-on conditions, these components are designed with a power-on reset function. In unipolar mode, the output is reset to 0V; in bipolar mode, the DAC5542TS output is set to $-V_{REF}$.

- **Digital-to-analog conversion section**

The DAC output impedance is independent of the code, while the input impedance seen by the reference is heavily dependent on the code. The output voltage depends on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N} \dots\dots\dots \text{Formula 1}$$

Note :

D is the decimal data word loaded into the DAC register.

N is the resolution of the DAC.

For a 2.5V reference, the equations simplify to the following:

$$V_{OUT} = \frac{2.5 \times D}{65536} \dots\dots\dots \text{Formula 2}$$

V_{OUT} of 1.25V for the DAC under medium-scale load and 2.5V under full-scale load. The LSB size is $V_{REF}/65536$.

- **Serial interface**

The DAC5541TS-5542TS is controlled by a versatile 3- or 4-wire serial interface that operates at clock rates up to 25MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. The timing diagram is shown in Figure 6. Input data is generated by the chip select input CS. After a high-to-low transition on CS, the data is synchronously shifted and latched into the input register on the rising edge of the serial clock SCLK. The data is first loaded as a 16-bit word (MSB). After loading the 16 data bits into the serial input register, a low-to-high transition on CS transfers the contents of the shift register to the DAC. Data can only be loaded into the device when CS is low.

The DAC5542TS features an LDAC function, which allows the DAC latch to be asynchronously updated by bringing LDAC low after CS goes high. LDAC should be held high while data is written to the shift register. Alternatively, LDAC can be held low for synchronous DAC updates. Because LDAC is always low, the rising edge of CS loads data into the DAC.

- **Power-on reset**

The DAC5541TS-5542TS features a power-on reset function to ensure the output is in a known state upon power-up. For 150 milliseconds after power-on, the DAC output will remain at 0V regardless of the SPI input data. Thereafter, if the input is 0, the DAC output can only be updated when a precise 16-bit input is loaded. The DAC output remains unchanged when the number of loaded bits is greater than or less than 16.

12. Application Information

- **Unipolar output operation**

These DACs are capable of driving unbuffered loads up to 60kΩ. Unbuffered operation results in low supply current (typically 300μA) and low offset error. The DAC5541TS provides a unipolar output swing from 0V to V_{REF}. The DAC5542TS can be configured to output both unipolar and bipolar voltages. The code table for unipolar output operation modes is shown in Table 1.

DAC latch				Analog output
MSB	LSB			
1111	1111	1111	1111	V _{REF} × (65535/65536)
1000	0000	0000	0000	V _{REF} × (32768/65536) = 1/2V _{REF}
0000	0000	0000	0001	V _{REF} × (1/65536)
0000	0000	0000	0000	0V

Table 1. Unipolar Code Table

Assuming a perfect reference, the worst-case output voltage of a single pole can be calculated using the following equation:

$$V_{OUT-UNI} = \frac{D}{2^{16}} \times (V_{REF} + V_{GE}) + V_{ZSE} + INL \dots \dots \dots \text{Equation 3}$$

Note:

- V_{OUT-UNI} is the worst-case output in unipolar mode.
- D is the code loaded into the DAC.
- V_{REF} is the reference voltage applied to the component.
- V_{GE} is the gain error in volts.
- V_{ZSE} is the zero-scale error measured in volts.
- INL is an integral nonlinearity measured in volts.

- **Bipolar output operation**

With the aid of an external operational amplifier, the DAC5542TS can be configured to provide a bipolar voltage output. Matched bipolar offset resistors R_{FB} and R_{INV} are connected to the external operational amplifier to achieve this bipolar output swing; typically, R_{FB} = R_{INV} = 28kΩ. Table 2 shows the transfer function for this output operating mode.

DAC latch				Analog output
MSB	LSB			
1111	1111	1111	1111	+V _{REF} × (32767/32768)
1000	0000	0000	0001	+V _{REF} × (1/32768)
1000	0000	0000	0000	0V
0111	1111	1111	1111	-V _{REF} × (1/32768)
0000	0000	0000	0000	-V _{REF} × (32768/32768) = -V _{REF}

Table 2, Bipolar Code Table

Assuming a perfect reference, the worst-case bipolar output voltage can be calculated using the following equation:

$$V_{OUT-BIP} = \frac{[(V_{OUT-UNI} + V_{OS})(2 + RD) - V_{REF}(1 + RD)]}{1 + (2 + RD) / A} \dots \dots \dots \text{Equation 4}$$

Note:

- V_{OUT-BIP} is the worst-case output in bipolar mode.
- V_{OUT-UNI} is the worst-case output in unipolar mode.
- V_{OS} is the input offset voltage of the external operational amplifier.
- RD is the matching error of resistors R_{FB} and R_{INV}.
- A is the open-loop gain of the operational amplifier.

- **Decodes multiple channels DAC5541TS-5542TS**

The CS pin of the DAC5541TS-5542TS can be used to select one of multiple DACs. All devices receive the same serial clock and serial data, but only one device receives the CS signal at any given time. The DAC being addressed is determined by the decoder. There are some digital feedthroughs on the digital input lines. Using a burst clock minimizes the impact of digital feedthroughs on the analog signal path.

- **References and basis**

Because the input impedance is code-dependent, the reference pin should be driven by a low-impedance source. The DAC5541TS-5542TS operates from a reference voltage of 2.5V to VDD. Reference voltages below 2.5V will result in reduced accuracy. The DAC's full-scale output voltage is determined by the reference value. Tables 1 and 2 summarize the analog output voltages or specific digital codes. Bundle the wiring close to the package to minimize voltage drop between the package leads and the internal die.

