DAC5304/14/24, Low-Power, 4-Channel, 8/10/12 Bit DAC

1. Functional Description

- The DAC5304/14/24 series are 4-channel 8/10/12-bit DAC.
- Internal output voltage driver
- Internally integrated low-power, high-speed 3-wire SPI interface

2. Chip Features

- 2.5V-5.5V power supply
- The entire product line guarantees full code monotonicity.
- The DAC5304 integral nonlinearity is ±0.625 LSB.
- The DAC5314 integral nonlinearity is ±2.5 LSB.
- The DAC5324 integral nonlinearity is ±10 LSB.
- Power consumption as low as 120uA/channel with 3V power supply
- Power consumption as low as 150uA/channel under 5V supply
- Power consumption as low as 200nA in chip shutdown mode
- Reference voltage supports 0 to VDD
- The initial value for power-on reset is 0
- On-chip integrated rail-to-rail output driver (1nF load stable)
- Operating temperature range: -40℃ to +105℃

3. Applications

- Industrial control signal generation
- Digital control gain application
- Digital control DC deviation application
- Digital potentiometer applications
- Programmable voltage control applications
- Programmable current control applications

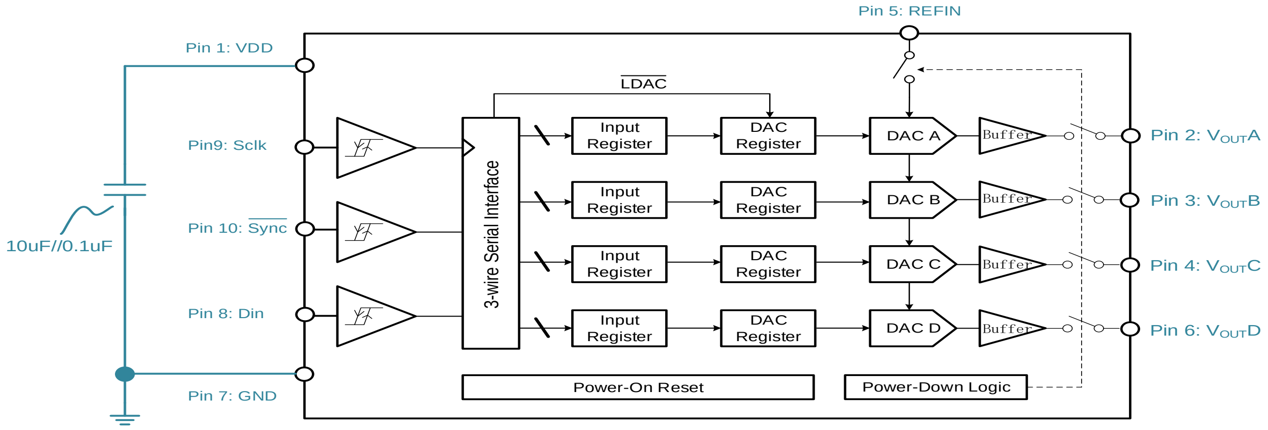
4. Component Selection Guide

Product Model	Function Definition
DAC5304ADF DAC5304AMS	4- channel, 8- bit digital-to-analog converter
DAC5304BDF DAC5304BMS	4- channel, 8- bit digital-to-analog converter
DAC5314ADF DAC5314AMS	4- channel, 10- bit digital-to-analog converter
DAC5314BDF DAC5314BMS	4- channel, 10- bit digital-to-analog converter
DAC5324ADF DAC5324AMS	4- channel, 12- bit digital-to-analog converter
DAC5324BDF DAC5324BMS	4- channel, 12- bit digital-to-analog converter

5. Device Packaging Information

Product Model	Packaging	Package Size
DAC5304	MSOP -10L	3mm×3mm
DAC5304	DFN -10L	3mm×3mm
DAC5314	MSOP -10L	3mm×3mm
DAC5314	DFN -10L	3mm×3mm
DAC5324	MSOP -10L	3mm×3mm
DAC5324	DFN -10L	3mm×3mm

6. Functional Block Diagram



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7. Pin Configuration and Functions

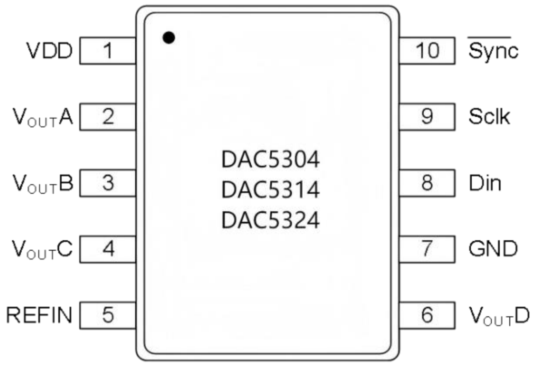

Figure 1. Pin diagram of MSOP10

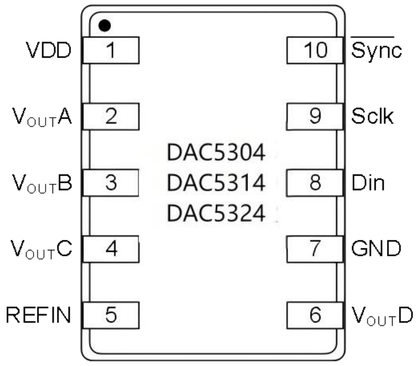

Figure 2. Pin diagram of DFN10

Pin Functions

Name	No.	Functions	Detailed description
VDD	1	Power supply	Power input. These components can operate within a voltage range of 2.5V to 5.5V, and the power supply can be disconnected from GND.
V_{OUT} A	2	Output	The buffered analog output voltage of channel A. The output amplifier has rail-to-rail operation.
V_{OUT} B	3	Output	The buffered analog output voltage of channel B. The output amplifier has rail-to-rail operation.
V_{OUT} C	4	Output	The buffered analog output voltage of channel C. The output amplifier has rail-to-rail operation.
REFIN	5	Input	The reference input pins for all four-channel digital-to-analog converters (DACs) have an input voltage range of 0.25V to VDD .
V_{OUT} D	6	Output	The buffered analog output voltage of channel D. The output amplifier has rail-to-rail operation.
GND	7	Ground	The ground reference point for all circuits on the component.
DIN	8	Input	Serial data input. The device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The Din input buffer is de-energized after each write cycle.
SCLK	9	Input	Serial clock input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock speeds up to 30MHz. The SCLK input buffer is de-energized after each write cycle.
SYNC	10	Input	Active Low Control Input (SYNC). This is the frame synchronization signal for input data. When SYNC goes low, it enables the input shift register, and data is transmitted on the next 16 falling edges of the clock cycle. If SYNC goes high before the 16th falling edge of SCLK, the rising edge of SYNC will act as an interrupt, and the device will ignore the write sequence.

8. Absolute operational conditions

(T_A = 25℃, unless otherwise specified.)

Parameter	Electrical symbols	Value
Power supply voltage relative to ground	V_{DDabs}	-0.3V to +7V
Digital input voltage relative to ground	V_{Digabs}	-0.3V to V_{DD} + 0.3V
Reference input voltage relative to ground	V_{refabs}	-0.3V to V_{DD} + 0.3V
A to D relatively	V_{outabs}	-0.3V to V_{DD} + 0.3V
Operating temperature range		
Industrial application temperature range	TP	-40℃ to +105℃
Storage temperature range	T_S	-65℃ to +150℃
Maximum junction temperature	T_J	150℃
Reflow soldering		
Peak temperature (Pb-free)		260℃
Peak temperature (non-Pb-free)		220℃
Peak temperature time		10 to 40 seconds

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9. Recommended operational conditions

Electrical parameters	Electrical symbols	Value		Unit
		Min	Max	
Power supply voltage	V_{DD}	2.5	5.5	V
Supply current	I_{DD}	400	600	μA
Ambient temperature	T_a	-40	105	° C

10. Device Static Characteristic Parameters

V_{DD} = 2.5V to 5.5V; V_{REF} = 2V; R_L = 2KΩ to ground (GND); C_L = 200pF to ground (GND); TA = 25℃; unless otherwise specified.

Parameter	Symbol	Test conditions	Version A			Version B			Unit
			Min	Typ	Max	Min	Typ	Max	
DC performance [1,2]									
DAC5304									
Resolution	Res_N	Ensure monotony		8			8		Bits
Integral nonlinearity	INL			±0.15	±1.15		±0.15	±0.625	LSB
Differential nonlinearity	DNL			±0.02	±0.25		±0.02	±0.25	LSB
DAC5314									
Resolution	Res_N	Ensure monotony		1 0			1 0		Bits
Integral nonlinearity	INL			±0.5	±4.05		±0.5	±2.5	LSB
Differential nonlinearity	DNL			±0.05	±0.5		±0.05	±0.5	LSB
DAC5324									
Resolution	Res_N	Ensure monotony		1 2			1 2		Bits
Integral nonlinearity	INL			±2	±16.05		±2	±10	LSB
Differential nonlinearity	DNL			±0.2	±1		±0.2	±1	LSB
Offset error				±0.4	±3		±0.4	±3	% of FSR
Gain error				±0.15	±1		±0.15	±1	% of FSR
Low-level dead zone		The low dead zone exists only when the offset error is negative.					20		mV
DC power supply common mode rejection ratio [3]	P SRR	VDD = ±10%		-60			-60		dB
DC interference [3]		RL = 2KΩ to ground (GND) or V_{DD}		200			200		uV
Reference Input [3]									
Reference input voltage range			0.25		V_{DD}	0.25		V_{DD}	V
Reference input impedance			37	45		37	45		KΩ
Reference feed		Frequency = 10kHz		-90			-90		dB
Output characteristic [3]									
Minimum output voltage[4]				0.001			0.001		V
Maximum output voltage[4]				V_{DD}-0.001			V_{DD}-0.001		V
DC output impedance				0.5			0.5		Ω
Short circuit current		V_{DD} = 5V		25			25		mA
		V_{DD} = 3V		16			16		mA
Startup time		Exit power-off mode V_{DD} = 5V		5			5		μs
		Exit power-off mode V_{DD} = 3V		2.5			2.5		μs

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Logical input [3]									
Low voltage input	V_{IL}	V_{DD}=5V ± 10%			0.8			0.8	V
		V_{DD} = 3V ± 10%			0.6			0.6	V
		V_{DD} = 2.5V ± 10%			0.5			0.5	V
High voltage input	V_{IH}	V_{DD}=5V ± 10%	24			24			V
		V_{DD} = 3V ± 10%	21			21			V
		V_{DD} = 2.5V ± 10%	2.0			2.0			V
Capacitance									pF

Parameter	Symbol	Test conditions	Version A			Version B			Unit
			Min	Typ	Max	Min	Typ	Max	
Power requirements									
Power supply voltage	V_{DD}					2.5		5.5	V
I_{DD} (Standard Mode) [4]									
V_{DD} = 4.5V to 5.5V		V_{IH} = V_{DD} and V_{IL} = GND		6 00	9 00		6 00	9 00	uA
V_{DD} = 2.5V to 3.6V		V_{IH} = V_{DD} and V_{IL} = GND		500	7 00		500	7 00	uA
I_{DD} (Sleep Mode)									
V_{DD} = 4.5V to 5.5V		V_{IH} = V_{DD} and V_{IL} = GND		0.2	1		0.2	1	uA
V_{DD} = 2.5V to 3.6V		V_{IH} = V_{DD} and V_{IL} = GND		0.08	1		0.08	1	uA

1. DC specification test without load output.
2. During the linearity test , the input code range is: DAC5304 (Code 8 to Code 248), DAC5314 (Code 28 to Code 995), DAC5324 (Code 115 to Code 3981).
3. The design value is not the actual test value.
4. If the amplifier output reaches its minimum voltage value, the offset error must be negative. If the amplifier output reaches its maximum voltage value, V_{REF} = V_{DD} and the offset and gain errors must be positive.
5. In standard mode (IDD), the specifications are valid for all digital-to-analog converters (DACs) and all digital-to-analog converters (DACs) input codes, excluding load current, but invalid for interfaces.

11. Device dynamic characteristic parameters

V_{DD} = 2.5V to 5.5V; V_{REF} = 2V; R_L = 2KΩ to ground (GND); C_L = 200pF to ground (GND); T_A = 25℃; unless otherwise specified.

Parameter	Test conditions	Min	Typ	Max	Unit
DAC5304	1/4 to 3/4 (0x40 to 0xC0)		7		uS
DAC5314	1/4 to 3/4 (0x100 to 0x300)		8		uS
DAC5324	1/4 to 3/4 (0x400 to 0xC00)		9		uS
Slewing rate			0.7		V/uS
Main code converts glitch energy	1 LSB changes carry		40		nV-sec
Digital feedthrough			1		nV-sec
Digital crosstalk			1		nV-sec
DAC-to-DAC crosstalk			3		nV-sec
Maximum bandwidth	V_{REF} = 2V ± 0.1V_{PP}		200		kHz
Total Harmonic Distortion	V_{REF} = 2.5V ± 0.1V_{P-P}; Frequency = 10KHz		-70		dB

12 . Device Operational Principle

12.1 Principle Description

The DAC5304/14/24 are four-channel resistor-divided analog-to-digital converters (DACs) manufactured using CMOS technology. The DAC5304/14/24 offers 8-bit , 10-bit, and 12-bit resolutions, respectively. Each product includes four output buffer amplifiers, and data is written via a 3-wire serial interface. They operate from a single supply ranging from 2.5V to 5.5V, with the output buffer amplifiers providing rail-to-rail output swing at a slew rate of 0.7V/μs. The four DACs share an independent reference input pin. The devices feature a programmable sleep mode, in which all digital-to-analog conversions are completely shut down in a high-impedance output mode. A single DAC channel architecture includes one series-divided DAC and one output buffer amplifier in series. The reference voltage on the reference pin provides the reference voltage for the DAC. The input encoding for the DAC is standard binary encoding. The four DACs share an independent reference input pin. The reference input voltage is unbuffered. Because there are no limitations on the voltage required for the upper and lower margins of any reference amplifier, users can obtain reference voltages as low as 0.25V or as high as V_{DD}. It is recommended to use an external buffered reference voltage. The typical input impedance is 45kΩ. The output buffer amplifier generates rail-to-rail voltage on the output circuit, with an output voltage range of 0V to V_{DD} when the reference voltage is V_{DD}. The amplifier can drive a 2kΩ load to ground (GND) or V_{DD}, with a 500pF capacitor in parallel with a resistor to ground (GND) or V_{DD}, a slew rate of 0.7V/μs, a half-amplitude settling time of 8μs, and an error of ±0.5LSB (on a 12-bit device).

The DAC5304/14/24 features a power-on restart function, therefore a power-on state is defined. In the power-on state, normal operation is used, with the output voltage set to 0V. The input and DAC registers are set to 0 and remain so until a valid write sequence is loaded onto the device.

The DAC5304/14/24 is controlled by a versatile, 3-wire serial interface with an operating clock rate of up to 30MHz, and is compatible with PI, QSPI, MICROWIRE, and DSP interface standards.

12.2 Programming Interface

BIT15 (MSB) … BIT0 (LSB)

A1	A0	$\overline{\text{PD}}$	$\overline{\text{LDAC}}$	D7	D6	D5	D4	D3	D2	D1	D0	0	0	X	X

DATA BITS (D7–D0)

Figure 3. Contents of the DAC5304 input shift register

BIT15 (MSB) … BIT0 (LSB)

A1	A0	$\overline{\text{PD}}$	$\overline{\text{LDAC}}$	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

DATA BITS (D9–D0)

Figure 4. Contents of the DAC5314 input shift register

BIT15 (MSB) … BIT0 (LSB)

A1	A0	$\overline{\text{PD}}$	$\overline{\text{LDAC}}$	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

DATA BITS (D11–D0)

Figure 5. Contents of the DAC5324 input shift register

The input shift register is 16 bits wide. Under serial clock input control (S_{clk}), data is loaded onto the device in 16-bit form. The 16-bit word contains four control bits, adjacent to either 10 or 12 bits of DAC data, the number of bits depending on the device type. Data is loaded to the most significant bit (MSB, bit 15). The first two bits determine whether data is provided to DAC A, DAC B, DAC C, or DAC D. Bits 13 and 12 control the DAC operating mode. Bit 13 is a pin pull-down (active low), determining whether the device operates in normal or sleep mode. Bit 12 indicates asynchronous DAC load input (active low), controlling the input when the DAC register and output are updated.

Address

A1	A0	DAC Addressed
0	0	DAC A

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0	1	DAC B
1	0	DAC C
1	1	DAC D

Address and control bits

PD 0: All four digital-to-analog converters (DACs) enter sleep mode, consuming only 200nA @ 5V, and the DAC outputs enter a high impedance state.

1: Normal working mode.

LDAC 0: All 4-channel digital-to-analog converter (DAC) registers and outputs are updated as the write sequence completes.

1: Only the address input register is updated; the contents of the digital-to-analog converter (DAC) register remain unchanged.

- DAC5324 uses all 12 bits of DAC data; DAC5314 uses 10 bits and ignores 2 LSB bits; DAC5304 uses 8 bits and ignores the last 4 bits ; the data format is pure binary, all 0s correspond to 0 V output, and all 1s correspond to full-scale output (V_{REF} −1 LSB).
- The $\overline{SYNC}$ input is a level-triggered input used as a frame synchronization signal and chip enable. Data can only be transmitted to the device when $\overline{SYNC}$ is low. To begin serial data transmission, set $\overline{SYNC}$ low and observe the minimum setup time t4 from $\overline{SYNC}$ to the falling edge of SCLK. After $\overline{SYNC}$ goes low, serial data is shifted into the device's input shift register on the falling edge of SCLK, lasting for 16 clock pulses. Since SCLK and the DIN input buffer are de-energized, any data and clock pulses after the 16th falling edge of SCLK are ignored. No further serial data transmission occurs until $\overline{SYNC}$ goes high and low again.
- $\overline{SYNC}$ can be set to high after the falling edge of the 16th SCLK pulse, and the time t7 from the minimum falling edge of SCLK to the rising edge of $\overline{SYNC}$ can be observed.
- After the serial data transmission is completed, the data is automatically transferred from the input shift register to the input register of the selected DAC. If $\overline{SYNC}$ goes high before the 16th falling edge of SCLK, the data transmission is aborted, and the DAC input register is not updated.
- When data is transferred to the three DAC input registers, all DAC registers and all DAC outputs are updated simultaneously by setting $\overline{LDAC}$ low when writing to the remaining DAC input registers.

13. Timing characteristics

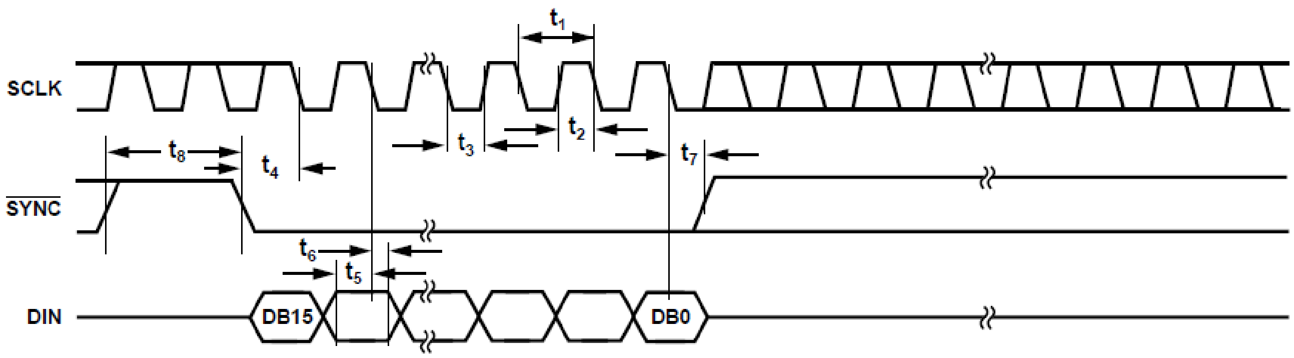

Figure 6. Timing diagram of the serial interface

VDD = 2.5V to 5.5V; TMIN to TMAX for all converters , unless otherwise specified .

Parameter [1 2 3]	T_{MIN}, T_{MAX} extreme values		Unit	Test conditions
	V_{DD} = 2.5V to 3.6V	V_{DD} = 3.6V to 5.5V	ns min	
t1	40	33	ns min	SCLK cycle time
t2	16	13	ns min	SCLK high level time
t3	16	13	ns min	SCLK low level time
t4	16	13	ns min	SYNC to SCLK falling edge setting time
t5	5	5	ns min	Data setting time
t6	4.5	4.5	ns min	Data retention time
t7	0	0	ns min	SCLK falling edge to SYNC rising edge time
t8	80	33	ns min	Minimum SYNC high level time

1. The design value is not the actual test value.
2. All input signals are specified as tr=tf=5ns (10% to 90% of V_{DD}), and the signal time starts from (V_{IL} + V_{IH}) / 2.
3. As shown in Figure 6.

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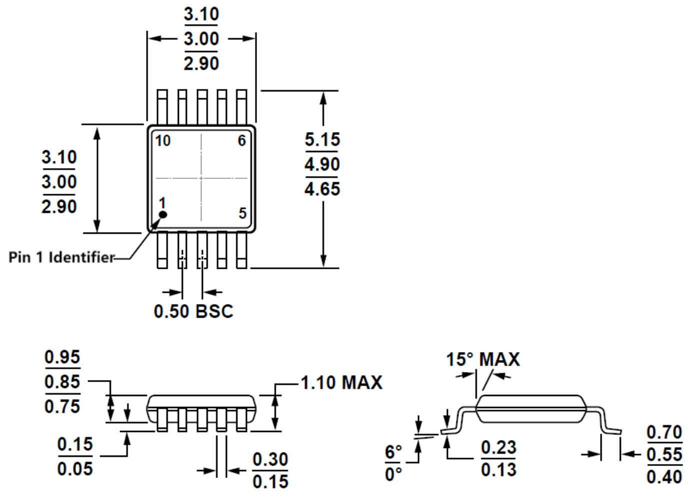
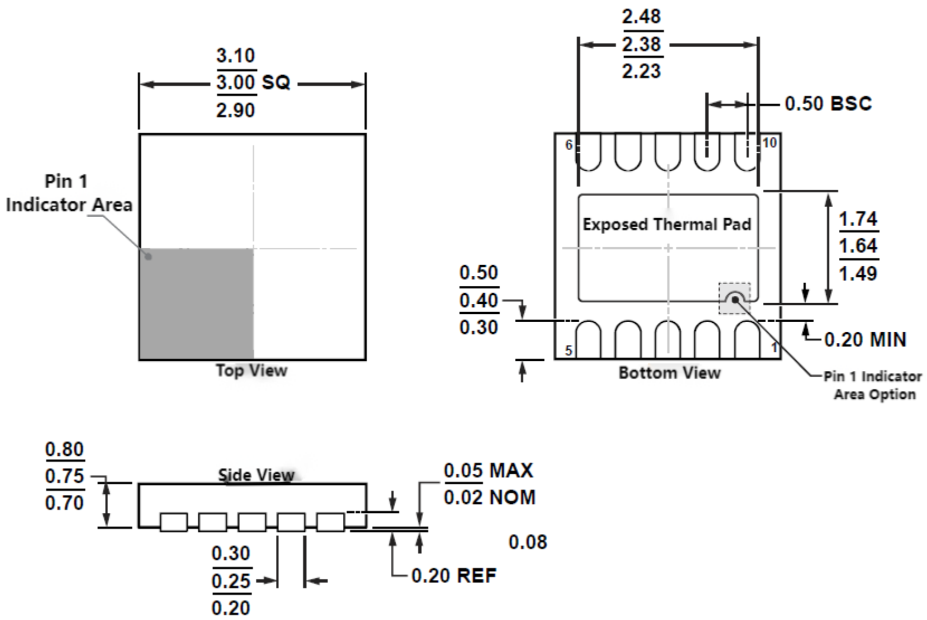
14. Packaging Dimensions and Structure

MSOP10 package



QFN10 package



15. Package Dimensions and Structure

Model		Temperature range	Packaging	Package
DAC5304	DAC5304ADF	-40 ℃ ~105 ℃	QFN10	4,000/reel
	DAC5304BDF	-40 ℃ ~105 ℃	QFN10	4,000/reel
	DAC5304AMS	-40 ℃ ~105 ℃	MSOP10	4,000/reel
	DAC5304BMS	-40 ℃ ~105 ℃	MSOP10	4,000/reel
DAC5314	DAC5314ADF	-40 ℃ ~105 ℃	QFN10	4,000/reel
	DAC5314BDF	-40 ℃ ~105 ℃	QFN10	4,000/reel
	DAC5314AMS	-40 ℃ ~105 ℃	MSOP10	4,000/reel
	DAC5314BMS	-40 ℃ ~105 ℃	MSOP10	4,000/reel
DAC5324	DAC5324ADF	-40 ℃ ~105 ℃	QFN10	4,000/reel
	DAC5324BDF	-40 ℃ ~105 ℃	QFN10	4,000/reel
	DAC5324AMS	-40 ℃ ~105 ℃	MSOP10	4,000/reel
	DAC5324BMS	-40 ℃ ~105 ℃	MSOP10	4,000/reel

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