

1. Characteristics

- Dual-channel, 14 bit A/D converter
- 1300MSPS conversion rate
- Integrated DDC
- SPI control interface
- JESD204B data output interface

2. Applications

- Multimode digital receiver
- Phased array radar
- Software radio
- Satellite receiver
- Instrument and apparatus

3. Overview

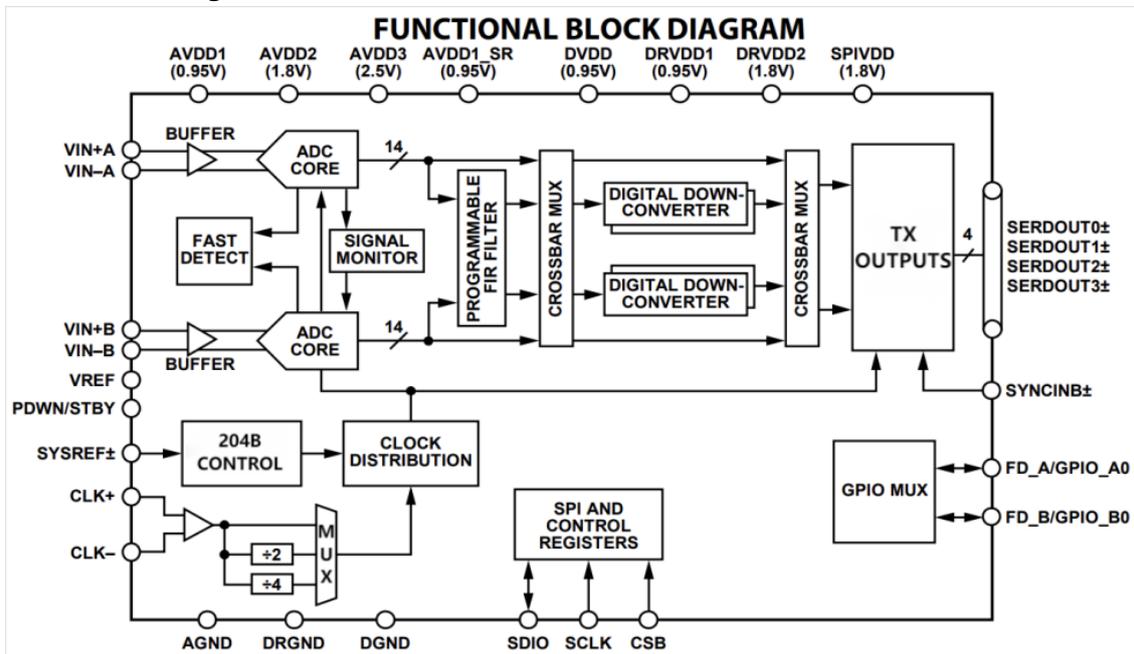
The functional block diagram of the ADCP9695-23 dual-channel 14-bit 1300MSPS A/D converter is shown in Figure 1. This device incorporates on-chip buffers and sample-and-hold circuitry, specifically designed for low power consumption, small size, and ease of use. It is designed for wideband analog signal sampling up to 2GHz. The device is optimized for wide input bandwidth, high sampling rate, and excellent linearity. This dual-channel ADC core employs a multi-stage, differential pipelined architecture and

integrates output error correction logic. Each ADC has a wide-bandwidth input, supporting a variety of user-selectable input ranges. An integrated reference voltage source simplifies the design. Both the analog input and clock signals are differential input signals. A programmable threshold detector monitors the input signal power using the ADC's fast detection output bit. If the input signal level exceeds the programmable threshold, the fast detection indicator goes high. Because of the extremely short delay of this threshold indicator, users can quickly reduce the system gain, thereby avoiding over-range phenomena at the ADC input. Users can configure the Class 1 JESD204B high-speed serial output as 1, 2, or 4 channels, depending on the DDC configuration and the acceptable channel rate of the receiving logic device. Multi-device synchronization is available via the SYSREF± and SYNCINB± input pins, with the operating timing shown in Figure 2. The rated operating temperature range is $-40^{\circ}\text{C} \leq \text{TA} \leq 85^{\circ}\text{C}$. The device uses the QFN64 pinout, which is pin-compatible with Analog Devices' AD9695 and serves as a functional replacement.

4. Device packaging information

Product Model	Packaging Type	Package Size
ADCP9695-23	QFN-64	9mm×9mm

5. Functional Block Diagram



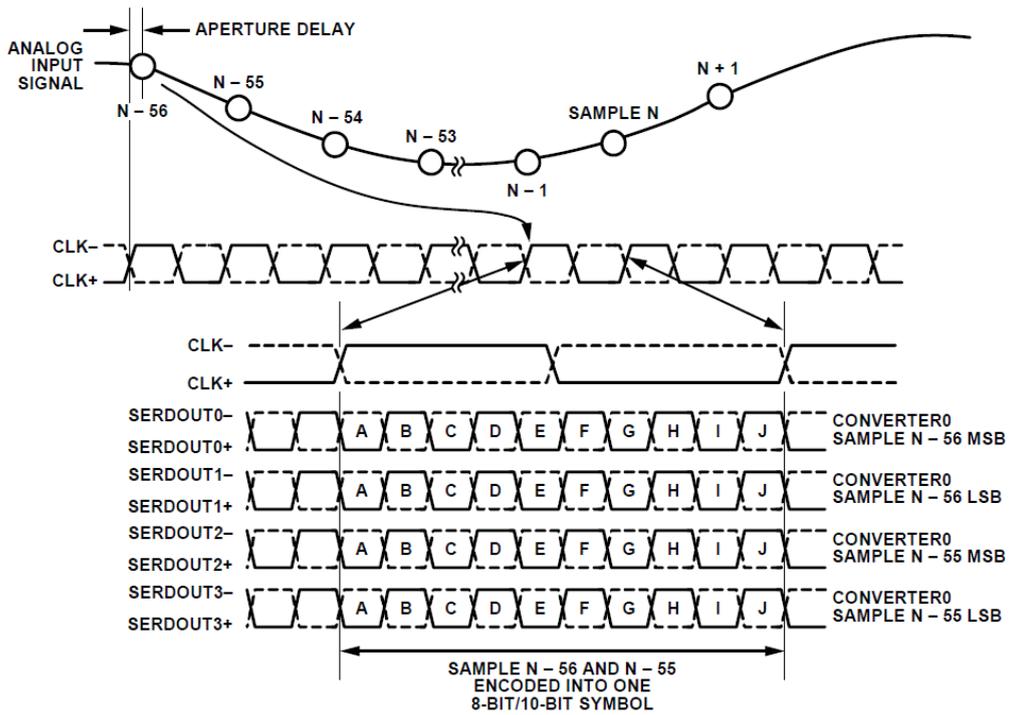
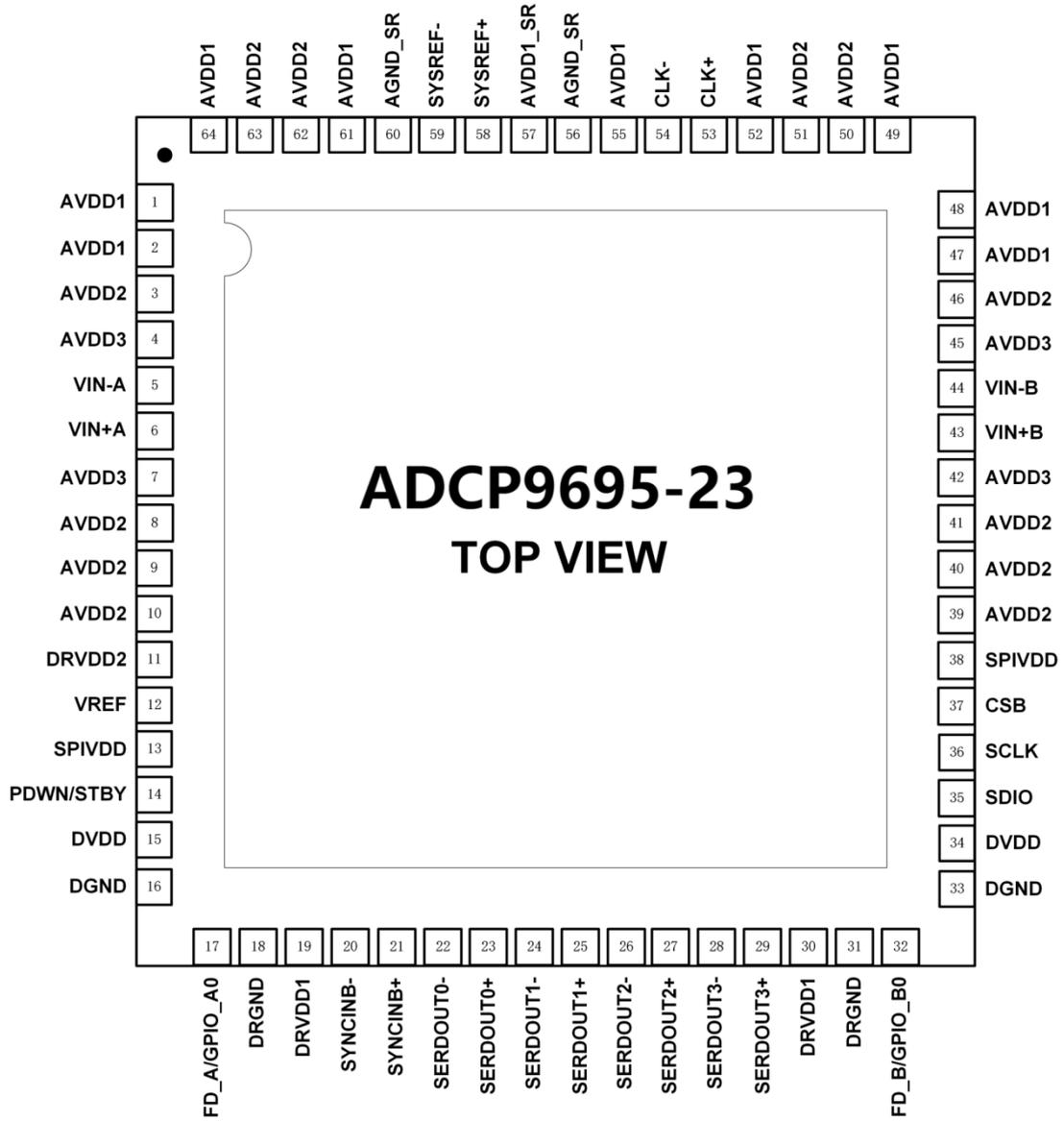
6. Timing diagram


Figure 2. Data output timing diagram

7. Pin Configuration and Functions


Pin configuration diagram

Pin Functions

No.	Symbol	Function	No.	Symbol	Function
1	AVDD1	0.95V analog power supply	33	DGND	Digital
2	AVDD1	0.95V analog power supply	34	DVDD	Digital power supply 0.95V
3	AVDD2	1.8V analog power supply	35	SDIO	SPI Input / Output
4	AVDD3	2.5V analog power supply	36	SCLK	SPI clock
5	VIN - A	Channel A analog input, negative terminal	37	CSB	SPI chip select
6	VIN+A	Channel A analog input,, positive terminal	38	SPIVDD	SPI power supply (1.8V)
7	AVDD3	2.5V analog power supply	39	AVDD2	1.8V analog power supply
8	AVDD2	1.8V analog power supply	40	AVDD2	1.8V analog power supply
9	AVDD2	1.8V analog power supply	41	AVDD2	1.8V analog power supply
10	AVDD2	1.8V analog power supply	42	AVDD3	2.5V analog power supply
11	DRVDD2	TX power supply 1.8V	43	VIN+B	Channel B analog input, positive terminal
12	VREF	0.5V reference voltage input	44	VIN-B	Channel B analog input, negative terminal
13	SPIVDD	SPI power supply (1.8V)	45	AVDD3	2.5V analog power supply
14	PDWN/STBY	Power-off input	46	AVDD2	1.8V analog power supply
15	DVDD	Digital power supply 0.95V	47	AVDD1	0.95V analog power supply
16	DGND	Digital	48	AVDD1	0.95V analog power supply
17	FD_A/GPIO_A0	Channel A rapid detection output / General input/output port A0	49	AVDD1	0.95V analog power supply
18	DRGND	TX drive	50	AVDD2	1.8V analog power supply
19	DRVDD1	TX power supply 0.95V	51	AVDD2	1.8V analog power supply
20	SYNCINB-	JESD204B LVDS synchronous input, negative terminal	52	AVDD1	0.95V analog power supply
21	SYNCINB+	JESD204B LVDS synchronous input, positive terminal	53	CLK+	Clock, positive end
22	SERDOUT0-	Lane 0 data output, negative end	54	CLK-	Clock, negative end
23	SERDOUT0+	Lane 0 data output, positive terminal	55	AVDD1	0.95V analog power supply
24	SERDOUT1-	Lane 1 data output, negative end	56	AGND_SR	SYSREF
25	SERDOUT1+	Lane 1 data output, positive end	57	AVDD1_SR	SYSREF power supply 0.95V
26	SERDOUT2-	Lane 2 data output, negative end	58	SYSREF+	SYSREF, positive terminal
27	SERDOUT2+	Lane 2 data output, positive end	59	SYSREF-	SYSREF, negative terminal
28	SERDOUT3-	Lane 3 data output, negative end	60	AGND_SR	SYSREF
29	SERDOUT3+	Lane 3 data output, positive end	61	AVDD1	0.95V analog power supply
30	DRVDD1	TX power supply 0.95V	62	AVDD2	1.8V analog power supply
31	DRGND	TX drive	63	AVDD2	1.8V analog power supply
32	FD_B/GPIO_B0	Channel B rapid detection output / general input/output port B0	64	AVDD1	0.95V analog power supply
0	AGND	Analog ground			

8. Recommended working conditions

- Supply voltage (V_{AVDD1}) to analog ground (AGND): 0.93V~0.98V
- Supply voltage (V_{AVDD1_SR}) to analog ground (AGND): 0.93V~0.98V
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- Supply voltage (V_{AVDD2}) to analog ground (AGND): 1.71V~1.89V
- Supply voltage (V_{AVDD3}) to analog ground (AGND): 2.44V~2.56V
- Supply voltage (V_{DVDD}) to analog ground (DGND): 0.93V~0.98V
- Supply voltage (V_{DRVDD1}) to analog ground (DRGND): 0.93V~0.98V
- Supply voltage (V_{DRVDD2}) to analog ground (DRGND): 1.71V~1.89V
- Supply voltage (V_{SPIVDD}) to analog ground (DGND): 1.71V~1.89V
- Operating temperature (T_A): -40 °C~85°C

9. Absolute maximum ratings

- Supply voltage (V_{AVDD1}) to AGND: 1.05V
- Power supply voltage (V_{AVDD1_SR}) to AGND: 1.05V
- Supply voltage (V_{AVDD2}) to AGND: 2.0V
- Supply voltage (V_{AVDD3}) to AGND: 2.7V
- Power supply voltage (V_{DVDD}) to DGND: 1.05V
- Power supply voltage (V_{DRVDD1}) to DRGND: 1.05V
- Power supply voltage (V_{DRVDD2}) to DRGND: 2V
- Power supply voltage (V_{SPIVDD}) to DGND: 2V
- AGND to DRGND: -0.3V to 0.3V
- AGND to DGND: -0.3V to 0.3V
- DGND to DRGND: -0.3V to 0.3V
- VIN to AGND: .AGND-0.3V to $V_{AVDD3} + 0.3V$
- CLK to AGND: AGND-0.3V to $V_{AVDD1} + 0.3V$
- SCLK,SDIO,CSB to AGND: DGND-0.3V to $V_{SPIVDD} + 0.3V$
- PDWN/STBY to AGND: DGND-0.3V to $V_{SPIVDD} + 0.3V$
- SYSREF to AGND: 2.5V
- SYNCINB to AGND: 2.5V
- Storage temperature (T_{stg}): -65°C~150°C
- Junction temperature (T_j): 125°C

10. Specifications

Unless otherwise specified, $V_{AVDD1} = 0.95V$, $V_{AVDD1_SR} = 0.95V$, $V_{AVDD2} = 1.8V$, $V_{AVDD3} = 2.5V$, $V_{DVDD} = 0.95V$, $V_{DRVDD1} = 0.95V$, $V_{DRVDD2} = 1.8V$, $V_{SPIVDD} =$

1.8V, AGND=DGND=DRGND=AGND_SR=0V, FS = 1300MSPS, -40°C ≤ T_A ≤ 85°C, input amplitude range is 1.70Vp-p

Parameter	Symbol	Condition	Grouping	Limit value		Unit
				Min	Max	
Resolution	RES	—	A1, A2, A3	14		Bits
Offset error	O _e	—		-1	1	%FSR
Offset error matching	O _{em}	—		-1	1	%FSR
Imbalanced temperature drift ^a	O _{td}	T _A = -40°C ~ 85°C		-18	18	ppm/°C
Integral nonlinearity error	INL	f _{IN} = 10MHz		-10.0	10.0	LSB
Differential nonlinear error	DNL	f _{IN} = 10MHz		-0.9	0.9	LSB
Input equivalent noise	G _{in}	—	A4, A5, A6	—	8	LSB rms
noise spectral density	NSD	f _{IN} = 10MHz	A4, A5, A6	—	-146	dBFS/Hz
Input common-mode voltage ^a	V _{cm}	T _A = 25°C	A1	1.30	1.50	V
Power consumption	P _W	Dual Channel	A1, A2, A3	—	2.3	W
Power loss	P _D	—		—	580	mW
standby power consumption	P _{SB}	—		—	1.3	W
Internal reference voltage	V _{REF}	—		490	510	mV
Clock input frequency ^a	f _{clk}	L=4, T _A = 25°C	A4	—	1300	MHz
Sampling frequency ^a	F _S	T _A = 25°C		—	1300	MSPS
AVDD1 current	I _{AVDD1}	—	A1, A2, A3	—	450	mA
AVDD1_SR current	I _{AVDD1_SR}	—		—	45	mA
AVDD2 current	I _{AVDD2}	—		—	550	mA
AVDD3 current	I _{AVDD3}	—		—	105	mA
DVDD current	I _{DVDD}	—		—	400	mA
DRVDD1 current	I _{DRVDD1}	—		—	270	mA
DRVDD2 current	I _{DRVDD2}	—		—	45	mA
SPIVDD current	I _{SPIVDD}	—		—	7	mA
Offset error	O _e	—		-1	1	%FSR
Offset error matching	O _{em}	—		-1	1	%FSR
Signal-to-noise ratio	SNR	f _{IN} = 10MHz, -1.0dBFS	A4, A5, A6	60	—	dBFS
		f _{IN} = 170MHz, -1.0dBFS	A4, A5, A6	60	—	dBFS
		f _{IN} = 765MHz, -1.0dBFS	A4, A5, A6	58	—	dBFS
		f _{IN} = 1480MHz, -1.0dBFS	A4, A5, A6	56	—	dBFS
Signal-to-noise ratio	SINAD	f _{IN} = 10MHz, -1.0dBFS	A4, A5, A6	59	—	dBFS
		f _{IN} = 170MHz, -1.0dBFS	A4, A5, A6	59	—	dBFS
		f _{IN} = 765MHz, -1.0dBFS	A4, A5, A6	57	—	dBFS
		f _{IN} = 1480MHz, -1.0dBFS	A4, A5, A6	55	—	dBFS
Stray dynamic range	SFDR	f _{IN} = 10MHz, -1.0dBFS	A4, A5, A6	68	—	dBFS
		f _{IN} = 170MHz, -1.0dBFS	A4, A5, A6	68	—	dBFS
		f _{IN} = 765MHz, -1.0dBFS	A4, A5, A6	63	—	dBFS
		f _{IN} = 1480MHz, -1.0dBFS	A4, A5, A6	58	—	dBFS
Worst harmonic distortion (Except for second and third order)	HD _{2nd, 3rd}	f _{IN} = 10MHz, -1.0dBFS	A4, A5, A6	—	-68	dBFS
		f _{IN} = 170MHz, -1.0dBFS	A4, A5, A6	—	-68	dBFS
		f _{IN} = 765MHz, -1.0dBFS	A4, A5, A6	—	-63	dBFS
		f _{IN} = 1480MHz, -1.0dBFS	A4, A5, A6	—	-58	dBFS
Significant digits	ENOB	f _{IN} = 170MHz, -1.0dBFS	A4, A5, A6	9.5	—	Bits
		f _{IN} = 765MHz, -1.0dBFS	A4, A5, A6	9.1	—	Bits
		f _{IN} = 1480MHz, -1.0dBFS	A4, A5, A6	8.8	—	Bits
Crosstalk ^a	CT	f _{IN} = 10MHz, -1.0dBFS, T _A = 25°C	A4	80	—	dB
Parameter	Symbol	Condition	Grouping	Limit value		Unit

				Min	Max	
Double-tone intermodulation distortion ^a	IMD	$f_{IN1} = 170.8 \text{ MHz, } -7 \text{ dBFS}$ $f_{IN2} = 173.8 \text{ MHz, } -7 \text{ dBFS}$ $T_A = 25^\circ\text{C}$	A4	—	-70	dBFS
Clock input common-mode voltage ^a	V_{clk_cm}	$T_A = 25^\circ\text{C}$	A9	0.6	0.8	V
Clock differential input resistor ^a	R_{clk}	$T_A = 25^\circ\text{C}$	A9	—	50	k Ω
JESD204B Lane Rate ^a	f_{SDATA}	$T_A = 25^\circ\text{C}$	A9	—	13	Gbps
JESD204B Lane Number of Passages	L	—	A9, A10, A11	—	4	Lane
Logic 1 input voltages (SCLK, CSB, SDIO, PDWN/STBY, FD_A, FD_B)	V_{IH}	—	A9, A10, A11	$0.7 V_{SPIVDD}$	V_{SPIVDD}	V
Logic 0 input voltage (SCLK, CSB, SDIO, PDWN/STBY, FD_A, FD_B)	V_{IL}	—	A9, A10, A11	0	$0.35 V_{SPIVDD}$	V
Logic 1 output voltage (SDIO, FD_A, FD_B)	V_{OH_SDIO}	$I_{OH} = 4 \text{ mA}$	A9, A10, A11	$V_{SPIVDD} - 0.5$	V_{SPIVDD}	V
Logic 0 output voltage (SDIO, FD_A, FD_B)	V_{OL_SDIO}	$I_{OL} = 4 \text{ mA}$	A9, A10, A11	0	0.45	V
Setup time between data and the rising edge of SCLK	t_{DS}	—	A9, A10, A11	4	—	ns
Hold time between data and the rising edge of SCLK	t_{DH}	—		2	—	ns
SCLK cycle	t_{CLK}	—		40	—	ns
Establishment time between CSB and SCLK	t_S	—		2	—	ns
The holding time between CSB and SCLK	t_H	—		2	—	ns
SCLK should be in a logic high state for the shortest possible time.	t_{HIGH}	—		10	—	ns
SCLK should be in a low-level state for the shortest possible time.	t_{LOW}	—		10	—	ns
Maximum delay from the falling edge of SCLK to data output	t_{ACCESS}	—		—	—	14
^a . Initial identification and testing of the influencing parameters during design and process changes. Group A: 3 samples were randomly tested at room temperature (0 samples) . Groups B , C and D: This parameter was not tested.						

11. Typical Applications

● **Differential input port**

The equivalent circuit of the analog input port is shown in Figure 3, designed to provide a 200Ω terminating impedance for the analog input signal. An input buffer provides high input impedance and reduces kickback noise from the ADC. The common-mode voltage of the ADCP9695-23 analog input port is approximately 1.4V. The clock signal alternates between sample-and-hold modes of the input circuitry. A differential capacitor or two single-ended capacitors can be placed at the input to provide a matched passive network; this configuration ultimately creates a low-pass filter at the input, limiting unwanted broadband noise. For optimal dynamic performance, the impedances driving VIN + x and VIN-x must be matched to ensure symmetrical common-mode stability error.

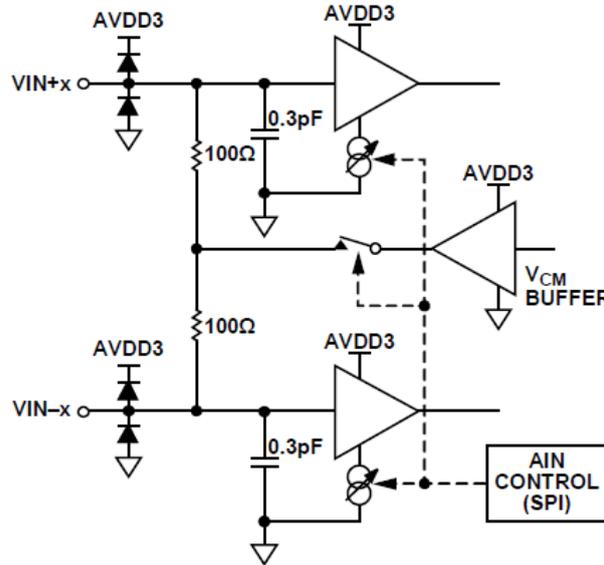


Figure 3. Equivalent circuit diagram of analog input terminal

Optimal performance can be achieved by driving analog inputs differentially.

- 1) For applications where SNR and SFDR are critical parameters, differential transformer coupling is recommended.
 - 2) For low-IF frequencies, a dual balun or dual transformer network is recommended for optimal performance.
 - 3) For higher frequencies in the second or third Nyquist region, remove some front-end passive components to ensure signal bandwidth.
- Recommended low-frequency and high-frequency input signal configurations are shown in Table 1 of Figure 4.

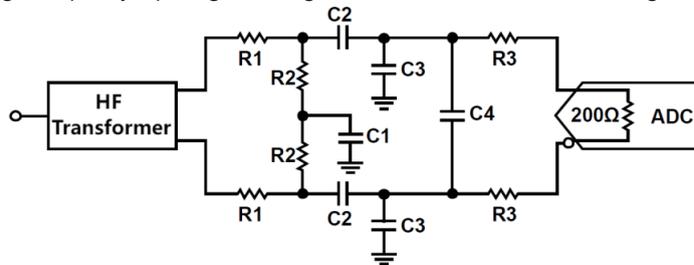


Figure 4. Low-frequency input signal configuration

Table 1. Input Signal Configuration Component Parameter Table

Product Model	Frequency range	Transformer	R1	R2	R3	C1	C2	C3	C4
ADCP9695-23	<2 GHz	BAL-0006/BAL0006SMG	25 Ω	25 Ω	10 Ω	0.1 μF	0.1 μF	DNI ¹	DNI ¹

¹. DNI indicates do not insert.

● **Reference voltage source**

The ADCP9695-23 features a built-in stable and accurate 0.5V reference voltage source. Users can choose to use this internal 0.5V reference voltage source or provide an external 0.5V reference voltage source via SPI register 0x18A6. When using an external reference voltage source, a 0.5V reference voltage source must be provided.

- 1) The required SPI write sequence for using an external voltage reference is as follows:
 1. register 0x18E3 to 0x00 to disable VCM output.
 2. register 0x18E6 to 0x00 to turn off the temperature diode output.
 3. register 0x18A6 to 0x01 to enable the external reference voltage.

- 2) The internal reference voltage can be output through the VREF port, which can help determine whether the circuit is working properly. The SPI writing sequence required for the internal reference voltage output is as follows:
1. Configure register 0x18E3 to 0x00 to disable VCM output.
 2. Configure register 0x18E6 to 0x00 to turn off the temperature diode output.
 3. Configure register 0x18A6 as the internal reference output of 0x10.

● **Clock port**

To achieve good dynamic performance, this product requires differential input at the clock input terminal. Figures 5 to 7 show several recommended clock input methods.

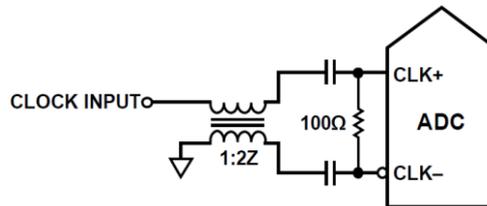


Figure 5. Transformer-coupled differential clock input

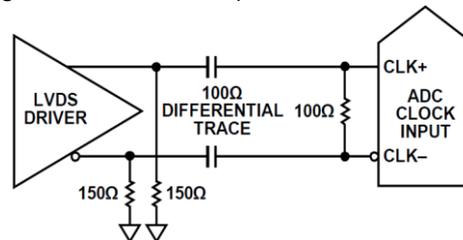


Figure 6. LVPECL Differential Clock Input

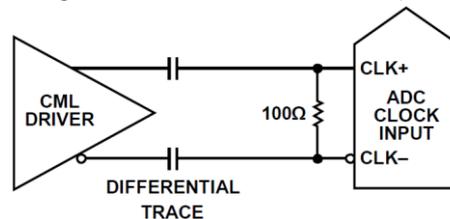


Figure 7. CML Differential Clock Input

● **Power off/standby mode**

The ADCP9695-23 has a PDWN/STBY pin that can be used to configure the device into power-down or standby mode. The default configuration is PDWN. The PDWN/STBY pin is a logic high-level pin. In power-down mode, the JESD204B link is interrupted. The power-down option can also be set via registers 0x003F and 0x0040. In standby mode, the JESD204B link is not interrupted, and 0 is transmitted for all converter samples. This can be changed using bit 7 of register 0x0571 to select the /K/ character.

● **Temperature diode**

The ADCP9695-23 incorporates a diode-based temperature sensor for measuring chip temperature. The diode output voltage is correlated with the chip temperature. Multiple diodes are present on the chip, and the temperature reading from the diode at the chip's center is representative of the entire chip's temperature. However, in applications using only one channel (with the other channel powered down), it is recommended to read the temperature from the diode corresponding to the active channel. Figure 8 shows the diode locations on the chip, with a pair of diodes at each location, one being 20 times the size of the other. It is recommended to use two diodes simultaneously at one location to obtain an accurate estimate of the die temperature.

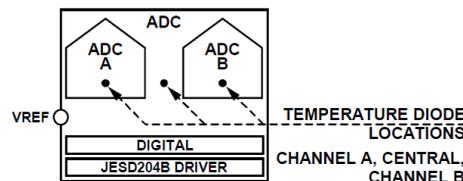


Figure 8. Location of the temperature diode in the chip

The temperature diode voltage can be output to the VREF pin using SPI. The diode is enabled or disabled using local register 0x18E6. The SPI write required to output the center temperature diode voltage is as follows:

- 1) Configure register 0x18E3 to 0x00 to disable VCM output.

- 2) Configure register 0x18A6 to 0x00 to disable the reference voltage output.
- 3) Configure register 0x18E6 to 0x01 to enable the voltage output of the 1× temperature diode. A typical voltage response of the temperature diode is shown in Figure 9. Although this voltage represents the chip temperature, it is recommended to measure it using a pair of diodes for improved accuracy.
- 4) Configure register 0x18E6 to 0x02 to enable the second center temperature diode, which is 20 times the size of the first. The measured incremental voltage (ΔV) versus unit junction temperature is shown in Figure 10.

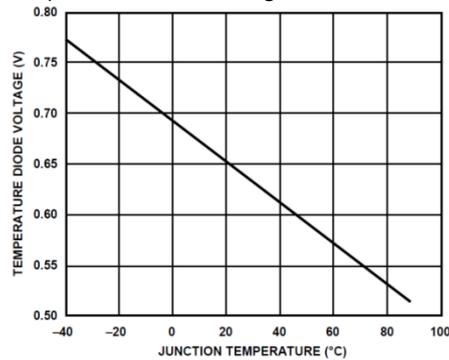


Figure 9. Typical voltage response of a 1× temperature diode

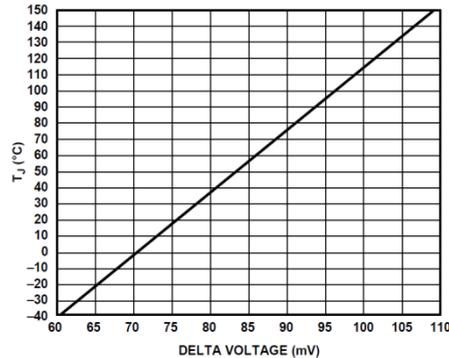


Figure 10. Relationship between ΔV and unit junction temperature

- **ADC offset calibration**

The ADCP9695-23 includes a digital filter to eliminate DC offset at the ADC output. For AC-coupled applications, this filter can be enabled by configuring register 0x0701 to 0x86 and 0x73B to 0x37. The filter calculates the average DC signal and subtracts it digitally from the ADC output. Because the filter does not distinguish the DC signal source, this function can be used when the DC signal content is not of interest. The filter can correct up to ± 512 LSB of DC; beyond this value, it saturates. Offset calibration is off by default.

- **Fast threshold detection (FD_A and FD_B)**

When the absolute value of the input signal exceeds the programmable upper threshold, the FD_A or FD_B pin is immediately set. The FD bit is cleared only when the absolute value of the input signal falls below the lower threshold and the duration exceeds the programmable dwell time. This feature provides hysteresis to prevent the FD bit from switching too frequently. The operation of the upper and lower threshold registers and the dwell time register are shown in Figure 11.

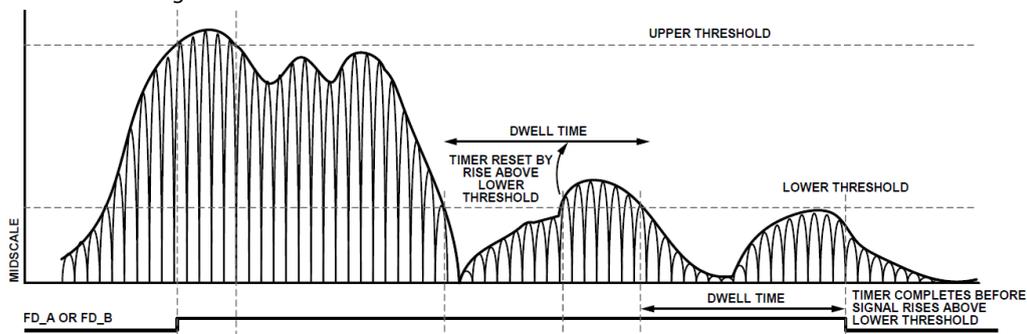


Figure 11. Threshold setting for FD signal

- 1) The FD indicator is set when the input signal amplitude exceeds the setting value of the fast detection threshold upper limit register (registers 0x0247 and 0x0248). The value of the selected threshold register is compared with the signal amplitude of the ADC output. Fast threshold

upper limit detection has a maximum delay of 28 clock cycles. The approximate threshold upper limit amplitude is defined by the following formula: **Threshold upper limit amplitude (dBFS) = 20log(threshold amplitude / 2¹³)**

- 2) The FD indicator will not be cleared until the signal drops below the lower threshold and remains there for a set dwell time. The lower threshold is set in the Fast Detection Lower Threshold Register (registers 0x0249 and 0x024A). The value of the 13-bit Fast Detection Lower Threshold Register is compared with the amplitude of the signal output by the ADC. This comparison is controlled by the ADC pipeline delay, and the comparison accuracy depends on the converter resolution. The lower threshold is defined by the following formula: **Lower Threshold Amplitude (dBFS) = 20log(Threshold Amplitude / 2¹³)**

For example, to set the upper threshold of -6dBFS, write 0xFFF to registers 0x0247 and 0x0248; to set the lower threshold of -10dBFS, write 0xA1D to registers 0x0249 and 0x024A. The dwell time can be set from 1 to 65535 sampling clock cycles by writing the desired value to the fast detection dwell time registers (registers 0x024B and 0x024C).

● ADC Application Modes and JESD204B Tx Conversion Mapping

The ADCP9695-23 includes a configurable signal path, allowing different functions to be enabled for different applications. These functions are controlled via the chip application mode register 0x0200, where the chip operating mode is controlled by bits [3:0], and bit 5 controls whether chip Q is ignored. The ADCP9695-23 includes the following modes:

- 1) Full bandwidth mode: Two 14-bit ADC cores operate at full sampling rate.
- 2) DDC mode: Up to four digital downconverter (DDC) channels.

After selecting the chip application mode, the chip decimation ratio is set using bits [3:0] of register 0x0201. The output sampling rate = ADC sampling rate / chip decimation ratio. To support different application layer modes, the ADCP9695-23 treats each sample stream (real, I, or Q) as an independent virtual converter. Table 2 shows the number of virtual converters and transport layer mapping required when channel switching is disabled. Figure 12 shows the virtual converters and their relationship to the DDC output when using complex outputs. Each DDC channel output is used for two sample streams (I/Q) for complex data (real + imaginary), or one sample stream for real (I) data. The ADCP9695-23 can be configured to use up to eight virtual converters, depending on the DDC configuration. I/Q samples are always mapped in pairs to I samples mapped to the first virtual converter and Q samples mapped to the second virtual converter. With this transport layer mapping, the number of virtual converters is the same whether a single real converter produces I/Q outputs through a digital downconverter or I/Q outputs are produced through two real converters after analog downconversion. Figure 13 is a block diagram describing two scenarios of I/Q transport layer mapping.

Table 2 , Virtual Converter Mapping

Number of supported virtual converters	Chip operating mode (register 0x0200, bit [3:0])	ChipQ ignores (0x0200, bit 5)	Virtual converter mapping							
			0	1	2	3	4	5	6	7
1-2	Full bandwidth mode (0x0)	Real or complex number (0x0)	ADC A sample	ADC B sample	Unused	Unused	Unused	Unused	Unused	Unused
1	A DDC pattern (0x1)	Real number (I only) (0x1)	DDC0I sample	Unused	Unused	Unused	Unused	Unused	Unused	Unused
2	A DDC pattern (0x1)	Complex number (I/Q) (0x0)	DDC0I sample	DDC0 Q sample	Unused	Unused	Unused	Unused	Unused	Unused
2	Two DDC modes (0x2)	Real numbers (I only) (0x1)	DDC0I sample	DDC1I sample	Unused	Unused	Unused	Unused	Unused	Unused
4	Two DDC modes (0x2)	Complex numbers (I/Q) (0x0)	DDC0I sample	DDC0 Q sample	DDC1I sample	DDC1 Q sample	Unused	Unused	Unused	Unused
4	Four DDC modes (0x3)	Real numbers (I only) (0x1)	DDC0I sample	DDC1I sample	DDC2I sample	DDC3I sample	Unused	Unused	Unused	Unused
8	Four DDC modes (0x3)	Complex numbers (I/Q) (0x0)	DDC0I sample	DDC0 Q sample	DDC1I sample	DDC1 Q sample	DDC2I sample	DDC2 Q sample	DDC3I sample	DDC3 Q sample

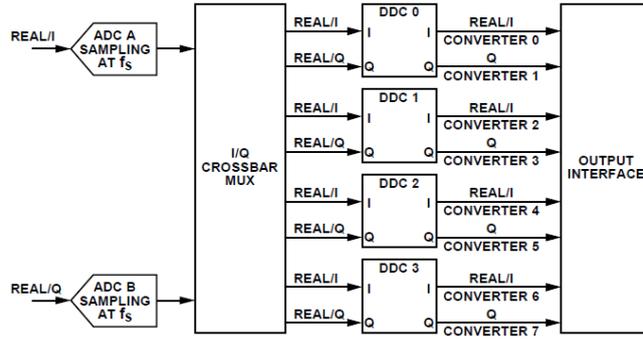


Figure 12. DDC and Virtual Converter Mapping

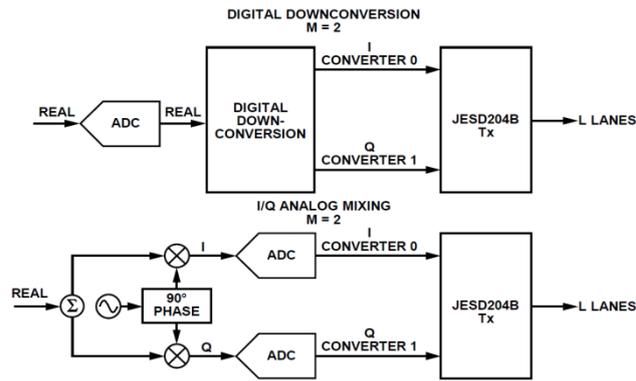


Figure 13. I/Q transport layer mapping

12. Digital Down - Inverter (DDC)

The ADCP9695-23 incorporates four digital down-converters (DDC0~DDC3) for filtering and reducing the output data rate. This digital processing section includes an NCO, multiple decimation FIR filters, a gain stage, and a complex-to-real conversion stage. Each processing module has control lines that can be individually enabled or disabled to provide the required processing functionality. The digital down-converters can be configured to output real or complex data.

The DDC outputs a 16-bit data stream. To enable this operation, the converter's bit width N is set to the default value of 16, even if the analog core only outputs 14 bits. In full-bandwidth operation, the ADC output is 14 bits followed by two zeros unless the end bit is enabled.

● DDC I/Q Input Selection

The ADCP9695-23 features two ADC channels and four DDC channels. Each DDC channel has two input ports, which can be paired to support real or complex inputs via an I/Q crossbar multiplexer. For real signals, both DDC input ports must select the same ADC channel; for example, DDC input port I = ADC channel A, and input port Q = ADC channel A. For complex signals, each DDC input port must select a different ADC channel; for example, DDC input port I = ADC channel A and DDC input port Q = ADC channel B. The inputs of each DDC are controlled by DDC input selection registers (Register 0x0311, Register 0x0331, Register 0x0351, and Register 0x0371).

● DDC I/Q output selection

Each DDC channel has two output ports, which can be paired to support real or complex outputs. For real output signals, only DDC output port I is used (DDC output port Q is invalid). For complex I/Q output signals, both DDC output ports I and Q are used. The I/Q outputs of each DDC channel are controlled by the DDC Complex to Real Enable bit (bit 3) in the DDC Control Registers (Registers 0x0310, 0x0330, 0x0350, and 0x0370). The Chip Q Ignore bit (bit 5) in the Chip Application Mode Register (Register 0x0200) controls the chip outputs of all DDC channels. When all DDC channels use real outputs, this bit is set high to ignore all DDC Q output ports. When setting any DDC channel to use complex I/Q outputs, the user must clear this bit to use both DDC output ports I and Q simultaneously.

● DDC Overview

Four DDC modules are used to extract a portion of the full digital spectrum captured by the ADC. Each DDC module contains four signal processing stages:

- 1) Frequency conversion stage (optional)
 - 2) Filtering stage
 - 3) Gain stage (optional)
 - 4) Complex to real number conversion level (optional)
1. Frequency conversion stage (optional)

The frequency conversion stage, consisting of a phase-coherent NCO and a quadrature mixer, can be used for frequency conversion of real or complex input signals. The phase-coherent NCO allows for an unlimited number of frequency hoppings, all referenced to a single synchronization event. It also includes 16 shadow registers for fast switching applications. This stage shifts a portion of the available digital spectrum down to baseband.

2. Filtering stage

After shifting down to baseband, the filtering stage uses multiple low-pass finite impulse response (FIR) filters to decimate the spectrum for rate conversion. The decimation process reduces the output data rate, which in turn reduces the output interface rate.

3. Gain stage (optional)

There will be losses when the real input signal is downmixed to the baseband. The gain stage compensates for this by increasing the gain by 0dB or 6dB.

4. Complex to Real Conversion Level (Optional)

When a real number output is required, the complex-to-real number conversion stage performs an $f_s/4$ mixing operation and filters out the complex components of the signal, thereby converting the complex output back to a real number output. [错误!未找到引用源。](#) shows a detailed block diagram of the DDC implemented in the ADCP9695-23.

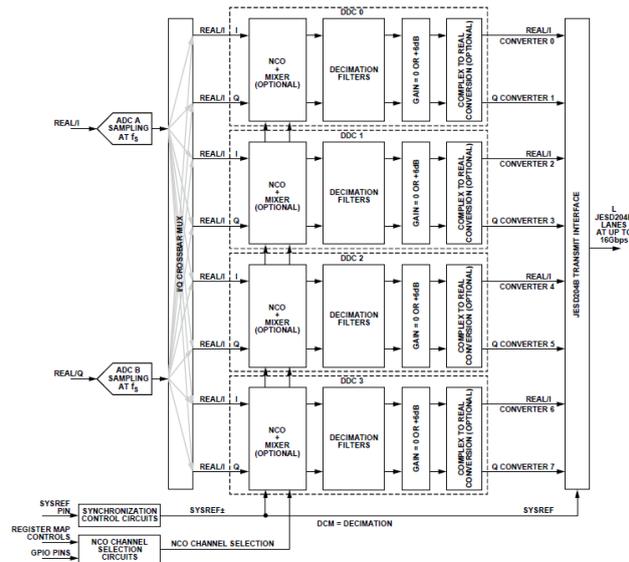


Figure 14. Detailed block diagram of DDC

13. DDC Frequency Conversion

• DDC Frequency Conversion Overview

Frequency conversion is implemented using a 48-bit complex NCO and a digital quadrature mixer. The frequency converter transforms a real or complex input signal from the intermediate frequency (IF) to a baseband complex digital output (carrier = 0Hz). Each DDC frequency conversion stage can be controlled independently, supporting four different IF modes, which can be selected using bits [5:4] of the DDC control registers (registers 0x0310, 0x0330, 0x0350, and 0x0370). These IF modes are as follows:

- 1) Variable IF pattern
- 2) Zero IF (ZIF) mode
- 3) $f_s/4$ Hz IF mode
- 4) Test mode

1. Variable IF pattern

NCO and mixer enable. The NCO output frequency can be used to digitally tune the IF frequency.

2. 0Hz IF (ZIF) mode

Mixer bypass, NCO disabled.

3. $f_s/4$ Hz IF mode

The mixer and NCO are enabled in a special $f_s/4$ mixing mode to save power.

4. Test mode

When the input sample reaches 0.999 to full scale, the NCO is enabled. This test mode allows the NCO to directly drive the decimation filter.

• DDC NCO Explanation

Each DDC contains an NCO, and each NCO performs the frequency conversion process by creating a complex exponential frequency ($e^{-j\omega t}$), which can be mixed with the input spectrum to convert the frequency band of interest to DC, and then filtered by a subsequent low-pass filter to prevent aliasing. When in variable IF mode, the NCO supports the following two modes.

• DDC NCO Programmable Modular Digital Mode

This mode supports >48-bit frequency tuning accuracy and is suitable for applications requiring precise rational number (M/N) frequency synthesis at a single carrier frequency. In this mode, the NCO is set by providing the following:

- 1) 48-bit frequency tuning word (FTW)
- 2) 48-bit Modular A-Word (MAW)
- 3) 48-bit Modular B-Word (MBW)
- 4) 48-bit phase offset word (POW)

• DDC NCO coherent mode

This mode allows for an unlimited number of frequency hopping events, with a single synchronization event at phase reference 0. This mode is useful when switching between different frequency bands while maintaining phase coherence. In this mode, the user can switch to any tuning frequency without resetting the NCO. Although only one FTW is required, the NCO contains 16 shadow registers for fast switching applications. The selection of the shadow registers is controlled by CMOS GPIO pins or SPI register mapping. In this mode, the NCO can be set by providing the following:

- 1) Up to 16 48-bit FTWs
- 2) A maximum of 16 48-bit Proof-of-Work (PoW) instances
- 3) In coherent mode, the 48-bit MAW must be set to 0.
- 4) Figure 15 shows a block diagram of an NCO and mixer. The coherent phase accumulator contains logic that allows for an unlimited number of frequency hoppings. The gray lines in the figure represent SPI control lines.

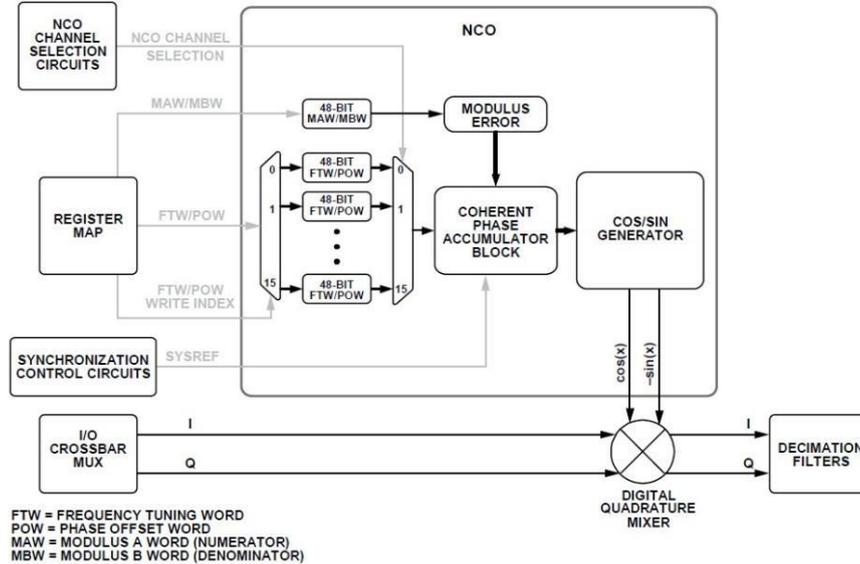


Figure 15. NCO and mixer block diagram

● NCO FTW/POW/MAW/MAB Description

The NCO frequency value is determined by the following settings:

- 1) 48-bit binary two's complement number input in FTW
- 2) 48-bit unsigned number entered in MAW
- 3) 48-bit unsigned number entered in MBW

The frequency between $-f_s/2$ and $+f_s/2$ (excluding $f_s/2$) is represented by the following values:

- 1) FTW=0x8000_0000_0000 and MAW=0x0000_0000_0000 represent the frequency of $-f_s/2$.
- 2) FTW=0x0000_0000_0000 and MAW=0x0000_0000_0000 represent DC (frequency 0Hz).
- 3) FTW=0x7FFF_FFFF_FFFF and MAW=0x0000_0000_0000 represent the frequency of $+f_s/2$.

● NCO FTW/POW/MAW/MAB Programmable Modular Digital Mode

For Programmable Modular Digital (MPD) mode, MAW must be set to a non-zero value (not equal to 0x0000_0000_0000). This mode is only required when frequency precision >48 bits is needed. An example of a frequency synthesis requirement requiring >48 -bit precision is a carrier frequency at $1/3$ sampling rate. When frequency precision ≤ 48 bits is needed, coherent mode must be used (see the NCO FTW/POW/MAW/MAB coherent mode section). In MPD mode, FTW, MAW, and MBW must satisfy the following four equations:

$$\frac{\text{mod}(f_c, f_s)}{f_s} = \frac{M}{N} = \frac{FTW + \frac{MAW}{MBW}}{2^{48}} \quad (1)$$

$$FTW = \text{floor}\left(2^{48} \frac{\text{mod}(f_c, f_s)}{f_s}\right) \quad (2)$$

$$MAW = \text{mod}(2^{48} \times M, N) \quad (3)$$

$$MBW = N \quad (4)$$

Where: f_c is the desired carrier frequency. f_s is the ADC sampling frequency. M is the integer representing the rational numerator of the frequency ratio. N is the integer representing the rational denominator of the frequency ratio. FTW is the 48-bit two's complement representation of NCO FTW. MAW is the 48-bit unsigned representation of NCO MAW (must be $< 2^{47}$). MBW is the 48-bit unsigned representation of NCO MBW. $\text{mod}(x)$ is the remainder function. For example, $\text{mod}(110,100) = 10$, and for negative numbers, $\text{mod}(-32,10) = -2$. $\text{floor}(x)$ is defined as the largest integer less than or equal to x . For example, $\text{floor}(3.6) = 3$.

Please note that the above formula applies to signal aliasing in the digital domain. M and N are coprime, and MAW and MBW are coprime. When

MAW is set to zero, the programmable analog-to-digital mode is automatically disabled. For example, if the ADC sampling frequency (f_s) is 1300 MSPS and the carrier frequency (f_c) is 417.8 MHz, then

$$\frac{\text{mod}(417.8, 1300)}{1300} = \frac{M}{N} = \frac{2089}{6250}$$

$$FTW = \text{floor}2^{48} \left(\frac{\text{mod}(2417.8, 1300)}{1300} \right) = 0x5590_C0AD_03D9$$

$$MAW = \text{mod}(2^{48} \times 2089, 6250) = 0x0000_0000_1117$$

$$MBW = 0x0000_0000_186A$$

The actual carrier frequency can be calculated using the following equation:

$$f_{C_ACTUAL} = \frac{FTW + \frac{MAW}{MBW} \times f_s}{2^{48}}$$

For the previous example, the actual carrier frequency (f_{C_ACTUAL}) is:

$$f_{C_ACTUAL} = \frac{0x5590_C0AD_03D9 \times \frac{0x0000_0000_1117}{0x0000_0000_186A} + \frac{MAW}{MBW} \times f_s}{2^{48}} = 417.8MHz$$

Each NCO has a 48-bit POW (Power over Wrap) to create a known phase relationship between multiple chips or individual DDC channels within a chip. In programmable analog-to-digital mode, the FTW (Fixed-Time Wrap) and POW registers can be updated at any time while still maintaining the deterministic phase results in the NCO. However, the following steps must be followed to update the MAW (Modal-Wave) and/or MBW (Modal-Time Wrap) registers to ensure proper NCO operation:

- 1) Write to the MAW and MBW registers of all DDCs.
- 2) The DDC can be soft-reset via the SPI register or the NCO can be synchronized via the SYSREF± pin.

- **NCO FTW/POW/MAW/MAB coherent modes**

For coherent mode, NCO MAW must be set to zero (0x0000_0000_0000). In this mode, NCO FTW can be calculated using the following equation:

$$FTW = \text{round} \left(2^{48} \frac{\text{mod}(f_c, f_s)}{f_s} \right)$$

Where: FTW is the 48-bit two's complement representation of NCO FTW. f_s is the ADC sampling frequency. f_c is the desired carrier frequency. $\text{mod}(x)$ is the remainder function. For example, $\text{mod}(110, 100) = 10$, and for negative numbers, $\text{mod}(-32, 10) = -2$. $\text{round}(x)$ is a rounding function. For example, $\text{round}(3.6) = 4$, and for negative numbers, $\text{round}(-3.4) = -3$.

Please note that the above formula applies to aliasing of signals in the digital domain. MAW must be set to zero to use coherent mode. When MAW is zero, the programmable analog-to-digital converter is automatically disabled. For example, if the ADC sampling frequency (f_s) is 1300 MSPS and the carrier frequency (f_c) is 417.3333 MHz, then:

$$FTW = \text{round} \left(2^{48} \frac{\text{mod}(417.333, 1300)}{1300} \right) = 0x5578_49CE_E73F$$

The actual carrier frequency can be calculated using the following equation:

$$f_{C_ACTUAL} = \frac{FTW \times f_s}{2^{48}}$$

For the previous example, the actual carrier frequency (f_{C_ACTUAL}) is:

$$f_{C_ACTUAL} = \frac{0x5578_49CE_E73F \times 1300}{2^{48}} = 417.333MHz$$

Each NCO has a 48-bit POW register to create a known phase relationship between multiple chips or individual DDC channels within a chip. In coherent mode, the FTW and POW registers can be updated at any time while still maintaining the deterministic phase results in the NCO.

- **NCO Channel Selection**

When configured in coherent mode, only one FTW is needed in the NCO. In this mode, the user can switch to any tuning frequency by directly writing to the FTW. For fast switching applications, all FTWs are known in advance and can be queued in a set; the NCO contains 16 additional shadow registers. These shadow registers are referred to as NCO channels below. Figure 16 shows a simplified block diagram of the NCO channel

selection module, with gray lines representing SPI control lines.

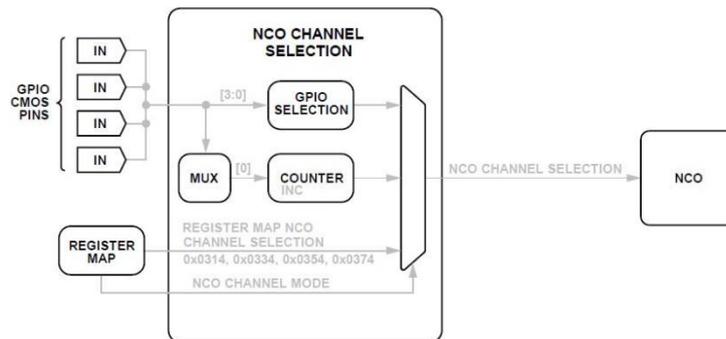


Figure 16. NCO channel selection module

Only one NCO channel is active at a time. NCO channel selection is controlled by a GPIO pin or via register mapping. Each NCO channel selector supports three different modes, described below:

- 1) GPIO level control mode. In this mode, the GPIO pin level determines the selected NCO channel.
 1. Configure one or more GPIO pins as NCO channel select inputs. GPIO pins not configured as NCO channel select inputs are internally connected to a low level.
 - a. To use GPIO_A0, write bits [2:0] in register 0x0040 to 0x6 and bits [3:0] in register 0x0041 to 0x6.
 - b. To use GPIO_B0, write bits [5:3] in register 0x0040 to 0x6, and write bits [7:4] in register 0x0041 to 0x6.
 2. By setting bits [7:4] in the NCO control registers (registers 0x0314, 0x0334, 0x0354, and 0x0374) to 0x1 to 0x6, the NCO channel selector is configured to GPIO level control mode, depending on the required GPIO pin command. The NCO channel is selected through the channel configuration gating registers (registers 0x0315, 0x0335, 0x0355, and 0x0375), and the corresponding FTW and POW are written.
 3. Select the desired NCO channel using the GPIO pin.
- 2) GPIO edge-triggered mode. A low-to-high transition on a single GPIO pin determines the selected NCO channel. The internal channel selection counter is reset by SYSREF± or DDC soft reset. To use GPIO edge-triggered mode for NCO channel selection, the following procedure must be followed:
 1. Configure one or more GPIO pins as NCO channel selection inputs.
 - a. To use GPIO_A0, write bits [2:0] in register 0x0040 to 0x6, and write bits [3:0] in register 0x0041 to 0x6.
 - b. To use GPIO_B0, write bits [5:3] in register 0x0040 to 0x6, and write bits [7:4] in register 0x0041 to 0x6.
 2. By setting bits [7:4] in the NCO control registers (registers 0x0314, 0x0334, 0x0354, and 0x0374) to 0x8 to 0xB, the NCO channel selector is configured to GPIO edge control mode, depending on the required GPIO pin. The NCO channel is selected through the channel configuration gating registers (registers 0x0315, 0x0335, 0x0355, and 0x0375), and the corresponding FTW and POW are written.
 3. The NCO channel is configured with a wraparound point by setting bits [3:0] in the NCO control registers (registers 0x0314, 0x0334, 0x0354, and 0x0374). For example, a value of 4 will cause the channel to wrap around back to channel 4 (e.g., 0, 1, 2, 3, 4, 0, 1, 2, 3, 4).
 4. The selected GPIO pin provides an edge-triggered NCO channel selection from low to high level.
- 3) Register control mode
 1. Select the NCO channel by configuring the channel strobe registers (registers 0x0315, 0x0335, 0x0355 and 0x0375) and write the corresponding FTW and POW.
 2. The register control mode is selected by setting bits [7:4] in the NCO control registers (register 0x0314, register 0x0334, register 0x0354 and register 0x0374) to 0x0, and bits [3:0] are set to 0x0 to 0xF to select the corresponding channel.

Figure 17 shows an example use case of coherent mode using three NCO channels. In this example, NCO channel 0 is downconverting to bandwidth 0 (B0), while NCO channels 1 and 2 are in standby mode and tuned to bandwidth 1 and bandwidth 2 (B1 and B2), respectively.

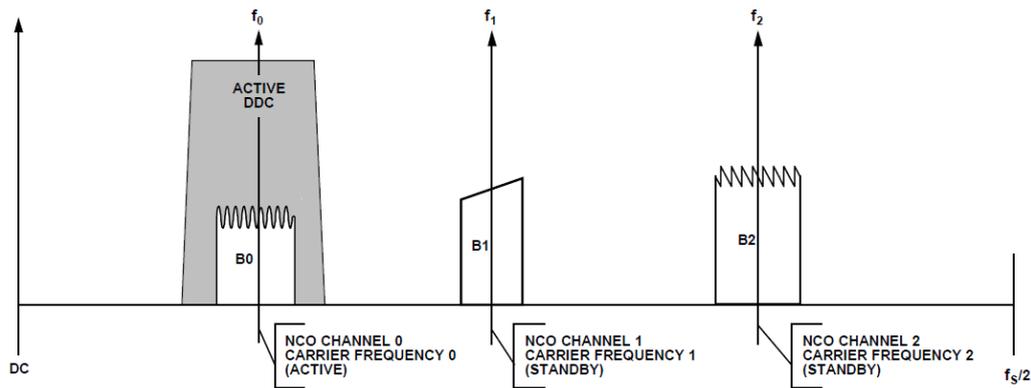


Figure 17. NCO coherent mode with three NCO channels (select B0)

The phase-coherent NCO switching function allows for an unlimited number of phase-coherent frequency hoppings. The initial phase of the NCO is synchronized with $SYSREF_{\pm}$. Switching the NCO FTW does not affect the phase; using this function, only one FTW is needed, and users can queue and hop frequencies using all 16 channels. If $SYSREF_{\pm}$ synchronization is completed during chip startup, all NCOs across multiple chips are essentially synchronized.

- **NCO synchronization**

Each NCO contains a separate Phase Accumulator Word (PAW), each PAW having an initial reset value of zero and incrementing every clock cycle. The instantaneous phase of the NCO is calculated using PAW, FTW, MAW, MBW, and POW. Due to this architecture, the FTW and POW registers can be updated at any time, while the NCO's PAW still maintains a deterministic phase result. There are two methods for PAW within the synchronization chip:

- 1) To enable SPI, all PAWs on the chip can be reset using the DDC NCO soft reset register (bit 4 of register 0x0300) in the DDC synchronization control register. This reset is accomplished by setting the DDC soft reset control bit high and then low. Note that this method can only be used to synchronize DDC channels within the same chip.
- 2) Use the $SYSREF_{\pm}$ pin. If the $SYSREF_{\pm}$ pin is enabled via the $SYSREF_{\pm}$ control registers (registers 0x0120 and 0x0121) and DDC synchronization is enabled via bits [1:0] of the DDC synchronization control register (register 0x0300), any subsequent $SYSREF_{\pm}$ event will reset all PAWs in the chip. Note that this method can be used to synchronize DDC channels within the same chip or DDC channels in different chips.

- **DDC Mixer Description**

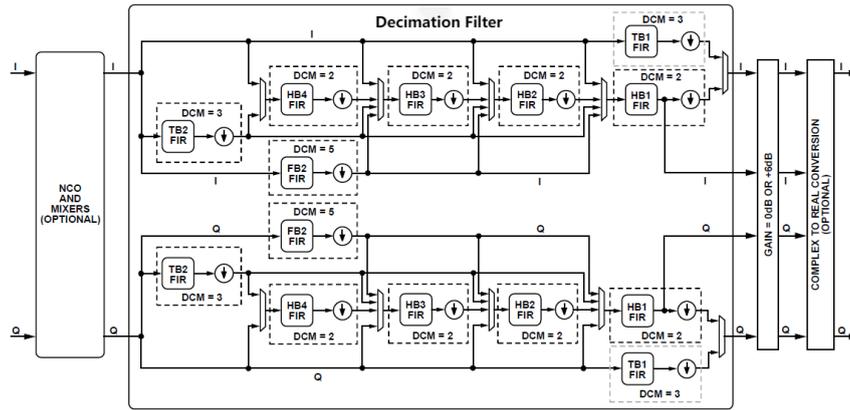
When not bypassed (register 0x0200 \neq 0x00), the digital quadrature mixer performs similar operations to the analog quadrature mixer, down-converting the input signal (real or complex) by using the NCO frequency as the local oscillator. For real input signals, a real-number mixer operation is performed (using two multipliers). For complex input signals, a complex-number mixer operation is performed (using four multipliers and two adders). The real or complex input can be selected for each DDC module using bit 7 of the DDC control registers (registers 0x0310, 0x0330, 0x0350, and 0x0370).

- **NCO+ mixer losses and SFDR**

When downmixing a real input signal to baseband, there is a 6dB signal loss due to filtering of the negative image. Additionally, the NCO causes a 0.05dB loss. The total loss for downmixing a real input signal to baseband is 6.05dB. Therefore, it is recommended that users enable the 6dB additional gain in the DDC gain stage to compensate for this loss. When downmixing a complex input signal (where the I and Q inputs of the DDC come from different ADCs) to baseband, the maximum value achievable by each I/Q sample after passing through the complex mixer is 1.414x full scale. For complex signals, to prevent I/Q samples from exceeding the range and to ensure the data bit width matches that of the real signal, the mixer causes a 3.06dB loss. Additionally, the NCO causes a 0.05dB loss. The total loss for downmixing a complex input signal to baseband is -3.11dB. For all output frequencies, the worst-case spurious signal SFDR of the NCO output is greater than 102dBc.

- **DDC Decimation Filter**

Following frequency conversion, multiple decimation filters reduce the output data rate. These filters effectively reduce the sampling rate while providing sufficient adjacent carrier aliasing suppression after down-converting the carrier frequency of interest to DC. Figure 18 shows a simplified block diagram of the decimation filter stage, and Table 3 [错误!未找到引用源。](#) describes the characteristics of different Finite Impulse Response (FIR) filter modules. Table 4 shows the different filter configurations that can be selected by including different filters. In all cases, the DDC filter stage provides 80% of the usable output bandwidth and 100 dB of stopband aliasing suppression.



FIR – Finite Impulse Response Filter DCM – Decimation After Sampling
TB1 is only supported in DDC0 and DDC1.

Figure 18. Block diagram of DDC decimation filter

Table 3. Characteristics of DDC Decimation Filter

Filter Name	Filter type	Extraction rate	Passband (radians/second)	Stopband (radians/second)	Passband ripple (dB)	Stopband attenuation (dB)
HB4	Low-pass FIR	2	$0.1 \times \pi/2$	$1.9 \times \pi/2$	$< \pm 0.001$	> 100
HB3	Low-pass FIR	2	$0.2 \times \pi/2$	$1.8 \times \pi/2$	$< \pm 0.001$	> 100
HB2	Low-pass FIR	2	$0.4 \times \pi/2$	$1.6 \times \pi/2$	$< \pm 0.001$	> 100
HB1	Low-pass FIR	2	$0.8 \times \pi/2$	$1.2 \times \pi/2$	$< \pm 0.001$	> 100
TB2	Low-pass FIR	3	$0.4 \times \pi/3$	$1.6 \times \pi/3$	$< \pm 0.002$	> 100
TB1 ¹	Low-pass FIR	3	$0.8 \times \pi/3$	$1.2 \times \pi/3$	$< \pm 0.005$	> 100
FB2	Low-pass FIR	5	$0.4 \times \pi/5$	$1.6 \times \pi/5$	$< \pm 0.001$	> 100

Table 4. DDC Filter Configuration

ADC Sampling Rate	DDC filter configuration	Real number (I) output		Complex (I/Q) output		Prevents overlapping bandwidth	Ideal signal-to-noise ratio Increase (dB) ²
		Extraction rate	Sampling rate	Extraction rate	Sampling rate		
fs	HB1	1	fs	2	fs/2(I) + fs/2(Q)	fs/2 x 80%	1
	TB1 ³	N/A	N/A	3	fs/3(I) + fs/3(Q)	fs/3 x 80%	2.7
	HB2+HB1	2	fs/2	4	fs/4(I) + fs/4(Q)	fs/4 x 80%	4
	TB2+HB1	3	fs/3	6	fs/6(I) + fs/6(Q)	fs/6 x 80%	5.7
	HB3+HB2+HB1	4	fs/4	8	fs/8(I) + fs/8(Q)	fs/8 x 80%	7
	FB2+HB1	5	fs/5	10	fs/10(I) + fs/10(Q)	fs/10 x 80%	8
	TB2+HB2+HB1	6	fs/6	12	fs/12(I) + fs/12(Q)	fs/12 x 80%	8.8
	FB2+TB1 ³	N/A	N/A	15	fs/15(I) + fs/15(Q)	fs/15 x 80%	9.7
	HB4+HB3+HB2+HB1	8	fs/8	16	fs/16(I) + fs/16(Q)	fs/16 x 80%	10
	FB2+HB2+HB1	10	fs/10	20	fs/20(I) + fs/20(Q)	fs/20 x 80%	11
	TB2+HB3+HB2+HB1	12	fs/12	24	fs/24(I) + fs/24(Q)	fs/24 x 80%	11.8
	HB2+FB2+TB1 ³	N/A	N/A	30	fs/30(I) + fs/30(Q)	fs/30 x 80%	12.7
	FB2+HB3+HB2+HB1	20	fs/20	40	fs/40(I) + fs/40(Q)	fs/40 x 80%	14
TB2+HB4+HB3+HB2+HB1	24	fs/24	48	fs/48(I) + fs/48(Q)	fs/48 x 80%	14.8	

¹ N/A indicates N/A.

² SNR improvement due to oversampling and filtering = $10 \log(\text{bandwidth}/f_s/2)$.

³ TB1 is only supported in DDC0 and DDC1.

● **HB4 filter**

The first 2x decimation, half-band, low-pass FIR filter (HB4) employs an 11-tap, symmetrical, fixed-coefficient filter scheme optimized for low power consumption. The HB4 filter is used only for complex output (16x decimation) or real output (8x decimation); otherwise, the filter is bypassed. Table 5 [错误!未找到引用源。](#) and Figure 19 show the coefficients and response of the HB4 filter.

Table 5. HB4 Filter Coefficients

HB4 coefficient value	Normalization coefficient	Decimal coefficient (15 digits)
C1, C11	0.006042	99
C2, C10	0	0
C3, C9	-0.049377	- 809
C4, C8	0	0
C5, C7	0.293304	4806
C6	0.5	8192

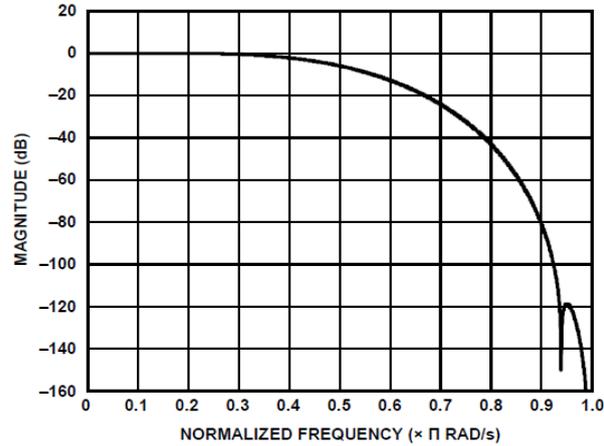


Figure 19 HB4 filter response

● **HB3 filter**

The second 2x decimation, half-band, low-pass FIR filter (HB3) employs an 11-tap, symmetrical, fixed-coefficient filter scheme optimized for low power consumption. The HB3 filter is only used when enabled for complex outputs (8x or 16x decimation) or real outputs (4x or 8x decimation); otherwise, the filter is bypassed. Table 6 and Figure 20 show the coefficients and response of the HB3 filter.

Table 6. HB3 Filter Coefficients

HB3 coefficient value	Normalization coefficient	Decimal coefficient (17 digits)
C1, C11	0.006637	435
C2, C10	0	0
C3, C9	-0.051055	-3346
C4, C8	0	0
C5, C7	0.294418	19295
C6	0.500000	65536

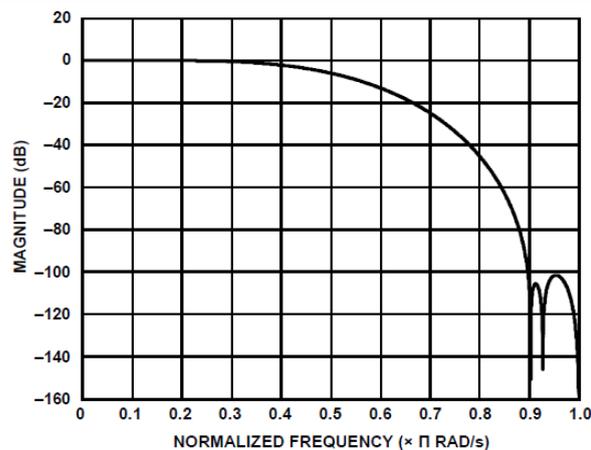


Figure 20. HB3 filter response

- **HB2 filter**

The third 2x decimation, half-band, low-pass FIR filter (HB2) employs a 19-tap, symmetrical, fixed-coefficient filter scheme optimized for low power consumption. The HB2 filter is only used for complex or real outputs (4x, 8x, or 16x decimation); otherwise, the filter is bypassed. Table 7 and Figure 21 show the coefficients and response of the HB2 filter.

Table 7. HB2 Filter Coefficients

HB2 coefficient value	Normalization coefficient	Decimal coefficient (18 digits)
C1,C19	0.000671	88
C2,C18	0	0
C3,C17	-0.005325	- 698
C4,C16	0	0
C5, C15	0.022743	2981
C6,C14	0	0
C7,C13	-0.074180	-9723
C8,C12	0	0
C9,C11	0.306091	40120
C10	0.5	65536

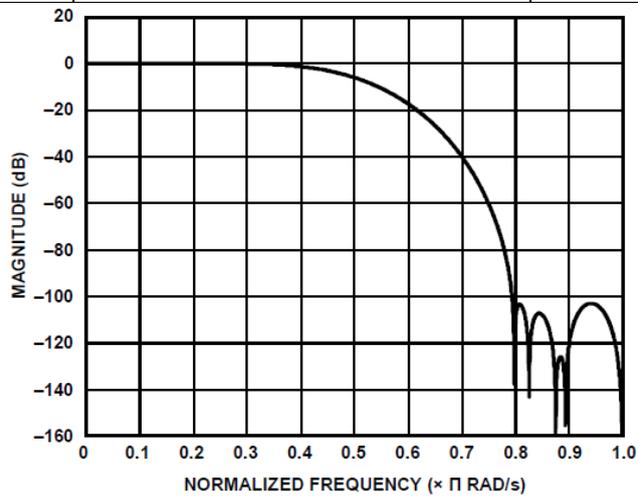


Figure 21. HB2 filter response

- **HB1 filter**

The fourth (and last) 2x decimation, half-band, low-pass FIR filter (HB1) employs a 63-tap, symmetrical, fixed-coefficient filter scheme optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 8 and Figure 22 show the coefficients and response of the HB1 filter.

Table 8. HB1 Filter Coefficients

HB1 coefficient value	Normalization coefficient	Decimal coefficient (20 digits)
C1, C63	-0.000019	-10
C2, C62	0	0
C3, C61	0.000072	38
C4, C60	0	0
C5, C59	-0.000195	-102
C6, C58	0	0
C7, C57	0.000443	232
C8, C56	0	0
C9, C55	-0.000891	-467
C10, C54	0	0
C11, C53	0.001644	862
C12, C52	0	0
C13, C51	-0.00284	-1489
C14, C50	0	0
C15, C49	0.004654	2440
C16, C48	0	0
C17, C47	-0.007311	-3833
C18, C46	0	0
C19, C45	0.011122	5831
C20, C44	0	0
C21, C43	-0.016554	-8679
C22, C42	0	0
C23, C41	0.02442	12,803
C24, C40	0	0
C25, C39	-0.036404	-19,086
C26, C38	0	0
C27, C37	0.056866	29,814
C28, C36	0	0
C29, C35	-0.101892	-53,421
C30, C34	0	0
C31, C33	0.316883	166,138
C32	0.5	262,144

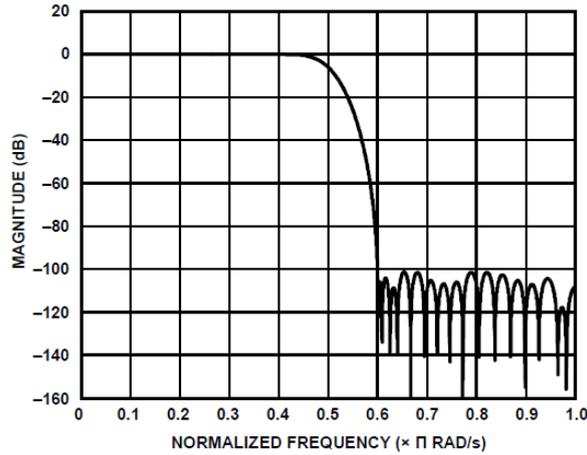


Figure 22. HB1 filter response

- TB2 filter**

The TB2 is implemented using a 26-tap, symmetric, fixed-coefficient filter optimized for low power consumption. The TB2 filter is only used when a decimation ratio of 6, 12, or 24 is required. Table 9 and Figure 23 show the coefficients and response of the TB2 filter.

Table 9. TB2 filter coefficients

TB2 coefficient value	Normalization coefficient	Decimal coefficient (19 digits)
C1,C26	-0.000190	-50
C2,C25	-0.000793	208
C3,C24	-0.00113	-298
C4,C23	0.000915	240
C5,C22	0.006290	1649
C6,C21	0.009822	2575
C7, C20	0.000915	240
C8,C19	- 0.023483	-6156
C9,C18	- 0.043151	-11312
C10, C17	- 0.019317	-5064
C11,C16	0.071327	18698
C12, C15	0.201171	52736
C13, C14	0.297756	78055

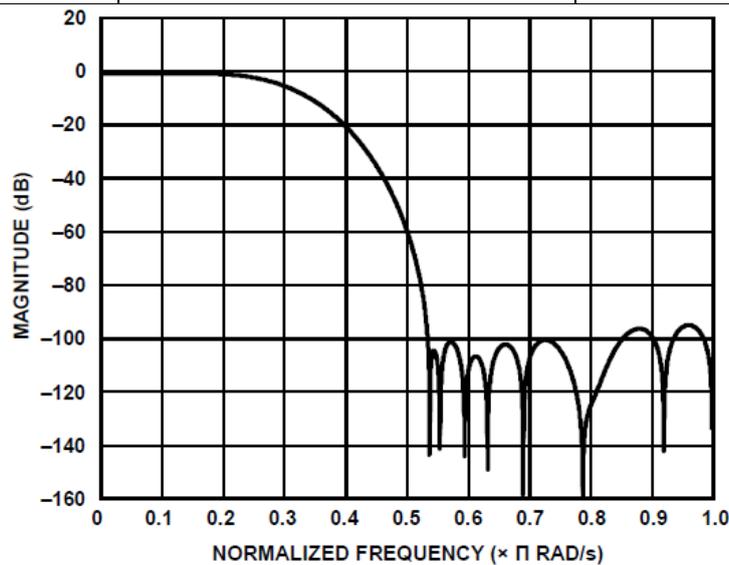


Figure 23. TB2 filter response

- **TB1 filter**

The TB1 decimation-3 low-pass FIR filter is implemented using a 76-tap, symmetric, fixed-coefficient filter. Table 10 shows the TB1 filter coefficients, and Figure 24 shows the TB1 filter response. TB1 is only available in DDC0 and DDC1.

Table 10. TB1 filter coefficients

TB1 coefficient value	Normalization coefficient	Decimal coefficient (22 bits)
C1, C96	-0.000023	-96
C2, C75	-0.000053	-224
C3, C74	-0.000037	-156
C4, C73	0.00009	379
C5, C72	0.000291	1220
C6, C71	0.000366	1534
C7, C70	0.000095	398
C8, C69	-0.000463	-1940
C9, C68	-0.000822	-3448
C10, C67	-0.000412	-1729
C11, C66	0.000739	3100
C12, C65	0.001665	6984
C13, C64	0.001132	4748
C14, C63	-0.000981	-4114
C15, C62	-0.002961	-12418
C16, C61	-0.002438	-10226
C17, C60	0.001087	4560
C18, C59	0.004833	20272
C19, C58	0.004614	19352
C20, C57	-0.000871	-3652
C21, C56	-0.007410	-31080
C22, C55	-0.008039	-33718
C23, C54	0.000053	222
C24, C53	0.010874	45608
C25, C52	0.013313	55840
C26, C51	0.001817	7620
C27, C50	-0.015579	-65344
C28, C49	-0.021590	-90556
C29, C48	-0.005603	-23502
C30, C47	0.022451	94167
C31, C46	0.035774	150046
C32, C45	0.013541	56796
C33, C44	-0.034655	-145352
C34, C43	-0.066549	-279128
C35, C42	-0.035213	-147694
C36, C41	0.07122	298720
C37, C40	0.210777	884064
C38, C39	0.3092	1296880

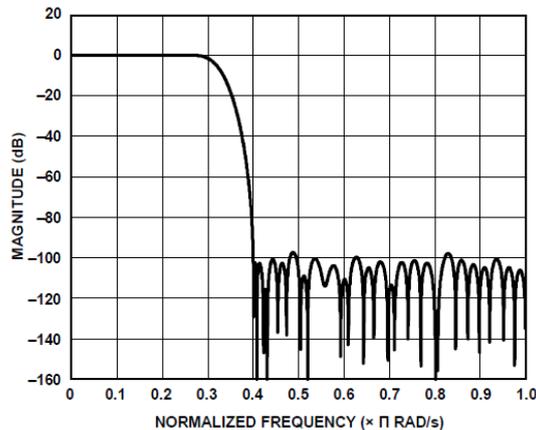


Figure 24. TB1 filter response

- **FB2 filter**

The FB2 decimation-5 low-pass FIR filter is implemented using a 48-tap, symmetrical, fixed-coefficient filter. Table 11 shows the FB2 filter coefficients, and Figure 25 shows the FB2 filter response.

Table 11. FB2 filter coefficients

FB2 coefficient value	Normalization coefficient	Decimal coefficient (21 digits)
C1, C48	0.000007	7
C2, C47	-0.000004	-4
C3, C46	-0.000069	-72
C4, C45	-0.000244	-256
C5, C44	-0.000544	-570
C6, C43	-0.000870	-912
C7, C42	-0.000962	-1009
C8, C41	-0.000448	-470
C9, C40	0.000977	1024
C10, C39	0.003237	3394
C11, C38	0.005614	5887
C12, C37	0.006714	7040
C13, C36	0.004871	5108
C14, C35	-0.001011	-1060
C15, C34	-0.010456	-10964
C16, C33	-0.020729	-21736
C17, C32	-0.026978	-28288
C18, C31	-0.023453	-24592
C19, C30	-0.005608	-5880
C20, C29	0.027681	29026
C21, C28	0.07272	76252
C22, C27	0.121223	127112
C23, C26	0.162346	170232
C24, C25	0.185959	194992

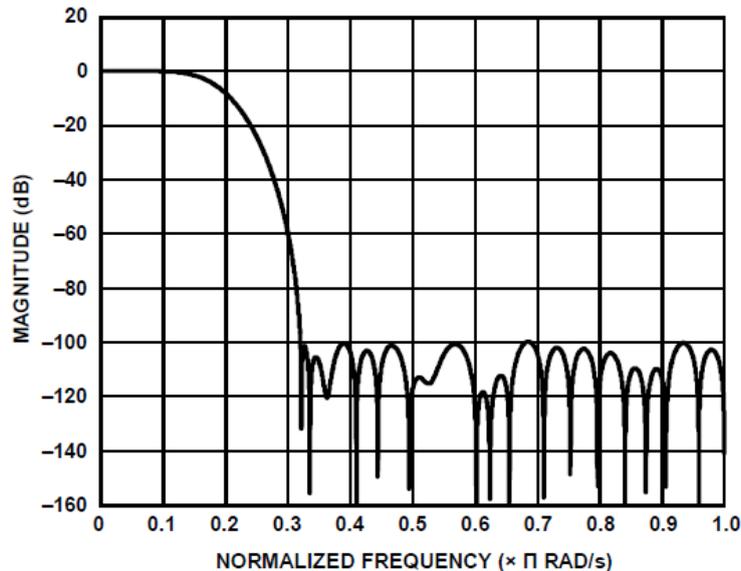


Figure 25. FB2 filter response

- **DDC gain stage**

Each DDC contains an independently controlled gain stage. Gain can be selected as 0dB or 6dB. When downmixing real input signals to baseband, it is recommended that the user enable the 6dB gain. No additional gain is needed when downmixing complex input signals to baseband. The optional 6dB gain can be used to compensate for signals with lower strength. When using the complex-to-real conversion stage, the 2x downsampling of the HB1 FIR filter is bypassed. The TB1 filter does not have a 6dB gain stage.

- **DDC Complex-Real Conversion**

Each DDC includes an independently controlled complex-to-real conversion module. This module reuses the last filter (HB1 FIR) of the filtering stage and, together with an $f_s/4$ complex mixer, upconverts the signal. After upconversion, the Q-section of the complex mixer is no longer needed and is discarded. The TB1 filter does not support complex-to-real conversion. Figure 26 shows a simplified block diagram of the complex-to-real conversion.

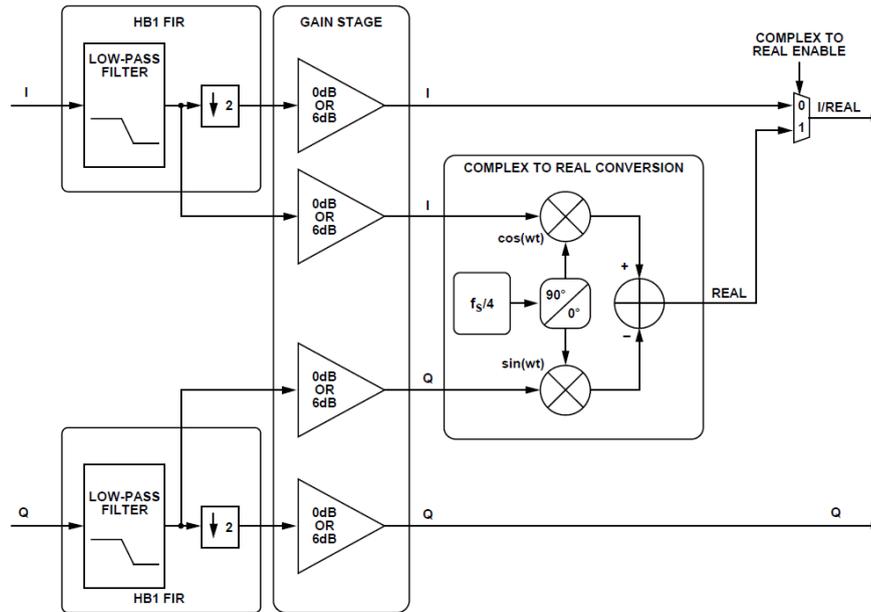


Figure 26. Conversion from Complex Numbers to Real Numbers

- DDC Hybrid Extraction Settings**

The ADCP9695-23 also supports DDCs with different decimation rates. In this case, the chip decimation rate must be set to the lowest decimation rate across all DDC channels. DDC samples with higher decimation rates are repeated to match the chip decimation rate. Only mixed decimation rates that are multiples of 2 are supported. For example, decimations of 1, 2, 4, 8, or 16 can be mixed together; decimations of 3, 6, 12, 24, or 48 can be mixed together; decimations of 5, 10, 20, or 40 can be mixed together. Table 12 shows the DDC sample mapping when the chip decimation rate differs from the DDC decimation rate. For example, if the chip decimation rate is set to 4x, DDC0 is set to use the HB2+HB1 filter (complex output 4x decimation), and DDC1 is set to use the HB4+HB3+HB2+HB1 filter (real output 8x decimation), the DDC1 output data is repeated twice, and Table 13 shows the final output samples.

Table 12. Sample Mapping When Chip Sampling Ratio (DCM) and DDC DCM Sample Index Do Not Match

Sample Index	DDC DCM = Chip DCM	DDC DCM = 2 × Chip DCM	DDC DCM = 4 × Chip DCM	DDC DCM = 8 × Chip DCM
0	N	N	N	N
1	N + 1	N	N	N
2	N + 2	N + 1	N	N
3	N + 3	N + 1	N	N
4	N + 4	N + 2	N + 1	N
5	N + 5	N + 2	N + 1	N
6	N + 6	N + 3	N + 1	N
7	N + 7	N + 3	N + 1	N
8	N + 8	N + 4	N + 2	N + 1
9	N + 9	N + 4	N + 2	N + 1
10	N + 10	N + 5	N + 2	N + 1
11	N + 11	N + 5	N + 2	N + 1
12	N + 12	N + 6	N + 3	N + 1
13	N + 13	N + 6	N + 3	N + 1
14	N + 14	N + 7	N + 3	N + 1
15	N + 15	N + 7	N + 3	N + 1
16	N + 16	N + 8	N + 4	N + 2
17	N + 17	N + 8	N + 4	N + 2
18	N + 18	N + 9	N + 4	N + 2
19	N + 19	N + 9	N + 4	N + 2
20	N + 20	N + 10	N + 5	N + 2
21	N + 21	N + 10	N + 5	N + 2
22	N + 22	N + 11	N + 5	N + 2
23	N + 23	N + 11	N + 5	N + 2
24	N + 24	N + 12	N + 6	N + 3
25	N + 25	N + 12	N + 6	N + 3
26	N + 26	N + 13	N + 6	N + 3
27	N + 27	N + 13	N + 6	N + 3
28	N + 28	N + 14	N + 7	N + 3
29	N + 29	N + 14	N + 7	N + 3
30	N + 30	N + 15	N + 7	N + 3
31	N + 31	N + 15	N + 7	N + 3

Table 13. DCM =4, DDC0 DCM=4 (complex number) and DDC1 DCM=8 (real number)

DDC Input sample	DDC0		DDC1	
	I port output	Q port output	I port output	Q port output
N	I0[N]	Q0[N]	I1[N]	N/A
N + 1	I0[N]	Q0[N]	I1[N]	N/A
N + 2	I0[N]	Q0[N]	I1[N]	N/A
N + 3	I0[N]	Q0[N]	I1[N]	N/A
N + 4	I0[N+1]	Q0[N+1]	I1[N]	N/A
N + 5	I0[N+1]	Q0[N+1]	I1[N]	N/A
N + 6	I0[N+1]	Q0[N+1]	I1[N]	N/A
N + 7	I0[N+1]	Q0[N+1]	I1[N]	N/A
N + 8	I0[N+2]	Q0[N+2]	I1[N+1]	N/A
N + 9	I0[N+2]	Q0[N+2]	I1[N+1]	N/A
N + 10	I0[N+2]	Q0[N+2]	I1[N+1]	N/A
N + 11	I0[N+2]	Q0[N+2]	I1[N+1]	N/A
N + 12	I0[N+3]	Q0[N+3]	I1[N+1]	N/A
N + 13	I0[N+3]	Q0[N+3]	I1[N+1]	N/A
N + 14	I0[N+3]	Q0[N+3]	I1[N+1]	N/A
N + 15	I0[N+3]	Q0[N+3]	I1[N+1]	N/A

- **DDC Example Configuration**

Table 14 describes the register settings for several DDC example configurations.

Table 14. DDC Configuration Example (per ADC channel pair)

Chip application layer	Chip extraction ratio	DDC Input Type	DDC output type	Each DDC bandwidth ¹	Number of virtual converters required	Register settings
1 DDC	2	plural	plural	40% × f _s	2	0x0200 = 0x01 (One DDC; I/Q selected) ; 0x0201 = 0x01 (Chip extraction 2) 0x0310 = 0x83 (Complex mixer; 0dB gain; Variable intermediate frequency; Complex output; HB1 filter) 0x0311 = 0x04 (DDC I input = ADC channel A; DDC Q input = ADC channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = Configure FTW and POW according to the requirements of the DDC0 application.
2 DDCs	4	plural	plural	20% × f _s	4	0x0200 = 0x02 (Two DDCs; I/Q selected) ; 0x0201 = 0x02 (4 chips extracted) 0x0310, 0x0330 = 0x80 (Complex mixer ; 0dB gain ; variable intermediate frequency ; complex output ; HB2+HB1 filter) 0x0311, 0x0331 = 0x04 (DDC I input = ADC channel A; DDC Q input = ADC channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = Configure FTW and POW according to the requirements of the DDC0 application. 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = Configure FTW and POW according to the requirements of the DDC1 application.
2 DDCs	4	plural	real numbers	10% × f _s	2	0x0200 = 0x22 (Two DDCs; only I can be selected) ; 0x0201 = 0x02 (4 chips extracted) 0x0310, 0x0330 = 0x89 (Complex mixer ; 0dB gain ; Variable intermediate frequency ; Real output ; HB3+HB2+HB1 filter) 0x0311, 0x0331 = 0x04 (DDC I input = ADC channel A; DDC Q input = ADC channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = Configure FTW and POW according to the requirements of the DDC0 application. 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = Configure FTW and POW according to the requirements of the DDC1 application.
2 DDCs	4	real numbers	real numbers	10% × f _s	2	0x0200 = 0x22 (Two DDCs; only I can be selected) ; 0x0201 = 0x02 (4 chips extracted) 0x0310, 0x0330 = 0x49 (Real mixer ; 6dB gain ; variable intermediate frequency ; real output ; HB3+HB2+HB1 filter) 0x0311 = 0x00 (DDC0 I input = ADC channel A; DDC0 Q input = ADC channel A) 0x0331 = 0x05 (DDC1 I input = ADC channel B; DDC1 Q input = ADC channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = Configure FTW and POW according to the requirements of the DDC0 application. 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = Configure FTW and POW according to the requirements of the DDC1 application.
2 DDCs	4	real numbers	plural	20% × f _s	4	0x0200 = 0x02 (Two DDCs; I/Q selected) ; 0x0201 = 0x02 (4 chips extracted) 0x0310, 0x0330 = 0x40 (Real mixer ; 6dB gain ; variable intermediate frequency ; complex output ; HB2+HB1 filter)

						<p>0x0311 = 0x00 (DDC0 I input = ADC channel A; DDC0 Q input = ADC channel A) 0x0331 = 0x05 (DDC1 I input = ADC channel B; DDC1 Q input = ADC channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = Configure FTW and POW according to the requirements of the DDC0 application. 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = Configure FTW and POW according to the requirements of the DDC1 application.</p>
2 DDCs	8	real numbers	real numbers	$5\% \times f_s$	2	<p>0x0200 = 0x22 (Two DDCs; only I can be selected) ; 0x0201 = 0x03 (8 chips extracted). 0x0310 , 0x0330 = 0x4A (Real mixer ; 6dB gain ; variable intermediate frequency ; real output ; HB4+HB3+HB2+HB1 filter) 0x0311 = 0x00 (DDC0 I input = ADC channel A; DDC0 Q input = ADC channel A) 0x0331 = 0x05 (DDC1 I input = ADC channel B; DDC1 Q input = ADC channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = Configure FTW and POW according to the requirements of the DDC0 application. 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = Configure FTW and POW according to the requirements of the DDC1 application.</p>
4 DDCs	8	real numbers	plural	$10\% \times f_s$	8	<p>0x0200 = 0x03 (Four DDCs; I/Q selected) ; 0x0201 = 0x03 (8 chips extracted) 0x0310, 0x0330, 0x0350, 0x0370 = 0x41 (Real mixer; 6dB gain; Variable intermediate frequency; Complex output; HB3+HB2+HB1 filter) 0x0311 = 0x00 (DDC0 I input = ADC channel A; DDC0 Q input = ADC channel A) 0x0331 = 0x00 (DDC1 I input = ADC channel A; DDC1 Q input = ADC channel A) 0x0351 = 0x05 (DDC2 I input = ADC channel B; DDC2 Q input = ADC channel B) 0x0371 = 0x05 (DDC3 I input = ADC channel B; DDC3 Q input = ADC channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = Configure FTW and POW according to the requirements of the DDC0 application. 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = Configure FTW and POW according to the requirements of the DDC1 application. 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = Configure FTW and POW according to the requirements of the DDC2 application. 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x038, 0x0381, 0x0382 = Configure FTW and POW according to the requirements of the DDC3 application.</p>
4 DDCs	8	real numbers	real numbers	$5\% \times f_s$	4	<p>0x0200 = 0x23 (Four DDCs; only I can be selected) ; 0x0201 = 0x03 (8 chips extracted) 0x0310, 0x0330, 0x0350, 0x0370 = 0x4A (Real mixer; 6dB gain; variable intermediate frequency; real output; HB4+HB3+HB2+HB1 filter) 0x0311 = 0x00 (DDC0 I input = ADC channel A; DDC0 Q input = ADC channel A) 0x0331 = 0x00 (DDC1 I input = ADC channel A; DDC1 Q input = ADC channel A) 0x0351 = 0x05 (DDC2 I input = ADC channel B; DDC2 Q input = ADC channel B) 0x0371 = 0x05 (DDC3 I input = ADC channel B; DDC3 Q input = ADC channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = Configure FTW and POW according to the requirements of the DDC0 application. 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = Configure FTW and POW according to the requirements of the DDC1 application.</p>

						<p>requirements of the DDC1 application. 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = Configure FTW and POW according to the requirements of the DDC2 application. 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x038, 0x0381, 0x0382 = Configure FTW and POW according to the requirements of the DDC3 application.</p>
4 DDCs	16	real numbers	plural	$5\% \times f_s$	8	<p>0x0200 = 0x03 (Four DDCs; I/Q selected) ; 0x0201 = 0x04 (16 chips extracted) 0x0310, 0x0330, 0x0350, 0x0370 = 0x42 (Real mixer; 6dB gain; Variable intermediate frequency; Complex output; HB4+HB3+HB2+HB1 filter) 0x0311 = 0x00 (DDC0 I input = ADC channel A; DDC0 Q input = ADC channel A) 0x0331 = 0x00 (DDC1 I input = ADC channel A; DDC1 Q input = ADC channel A) 0x0351 = 0x05 (DDC2 I input = ADC channel B; DDC2 Q input = ADC channel B) 0x0371 = 0x05 (DDC3 I input = ADC channel B; DDC3 Q input = ADC channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = Configure FTW and POW according to the requirements of the DDC0 application. 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = Configure FTW and POW according to the requirements of the DDC1 application. 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = Configure FTW and POW according to the requirements of the DDC2 application. 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x038, 0x0381, 0x0382 = Configure FTW and POW according to the requirements of the DDC3 application.</p>

¹ f_s is the ADC sampling rate

14. Digital Output

● JESD204B Interface Introduction

The ADCP9695-23 digital output is designed according to the JEDEC standard JESD204B ("Data Converter Serial Interface"). The ADCP9695-23 connects to digital processing devices via a serial interface (channel rates up to 15Gbps). Advantages of the JESD204B interface over LVDS include: less board space required for data interface wiring, and smaller packages for converters and logic devices.

● JESD204B Overview

The JESD204B data transmission module combines parallel data from an ADC into data frames and outputs serial data using 8B/10B encoding and data scrambling. During initial link establishment, special control characters are used to support link synchronization; subsequent synchronization is maintained through additional control characters embedded in the data stream. The ADCP9695-23 JESD204B data transmission module can map up to two real ADCs or eight virtual converters (when DDC is enabled). Links can be configured to use one, two, four, or eight JESD204B channels. The JESD204B specification references several parameters to define the link; these parameters must match between the JESD204B transmitter (ADCP9695-23 output) and the JESD204B receiver (logic device input).

The JESD204B link can be described by the following parameters:

- 1) L = Number of data paths / Converter (Number of data paths / Link) (The value for ADCP9695-23 is 1 , 2, or 4)
- 2) M = Number of converters / Number of converters (virtual converters / link) (The value for ADCP9695-23 is 1, 2, 4, or 8)
- 3) F = 8 bits per frame (the value for ADCP9695-23 is 1, 2, 4, 8, or 16).
- 4) N' = The number of bits for each sample (in JESD204B byte size) (The value for ADCP9695-23 is 8 or 16)
- 5) N = Converter resolution (the value of ADCP9695-23 is 7 to 16)
- 6) CS = Control bits / Sample size (The value of ADCP9695-23 is 0, 1, 2, or 3)
- 7) K = Number of frames per multiframe (the value for ADCP9695-23 is 4, 8, 12, 16, 20, 24, 28, or 32).
- 8) S = Number of samples transmitted / Single converter / Frame period (The value of ADCP9695-23 is automatically set according to L, M, F, and NE)
- 9) HD = High-density mode (ADCP9695-23 automatically sets L, M, F, and NE).
- 10) CF = Control Words / Frame Clock Cycle / Converter (Value for ADCP9695-23 is 0)

Figure 27 shows a simplified block diagram of the ADCP9695-23 JESD204B link. By default, the ADCP9695-23 is configured to use two converters and four channels. The data outputs of converter A are sent to SERDOUT0± and SERDOUT1±, and the data outputs of converter B are sent to SERDOUT2± and SERDOUT3±. The ADCP9695-23 allows for other configurations, such as combining the outputs of the two converters onto a single channel, or changing the mapping of the digital output paths of A and B. These modes are set via the SPI registers.

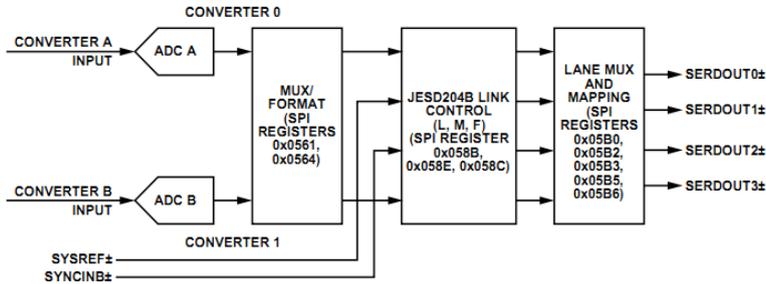


Figure 27. Simplified block diagram of the transmission link in full-bandwidth mode (register 0x0200=0x00)

By default, in the ADCP9695-23, each converter's 14-bit converter word is split into two octets (eight-bit data). Bits 13 (MSB) to 6 are located in the first octet. The second octet contains bits 5 to 0 (LSB) and two stop bits. The stop bits can be configured as zero or a pseudo-random number sequence. The stop bits can also be used as control bits to indicate overrange, SYSREF±, or fast detection output. The resulting two 8-bit words can be scrambled. Scrambling is optional, but it is recommended to enable this feature to avoid spectral spikes that occur when transmitting similar data patterns. The two 8-bit words are then encoded by an 8B/10B encoder. The 8B/10B encoder encodes eight data bits into a 10-bit character. Figure 28 shows how the 14-bit data is extracted from the ADC, how the stop bits are added, how the two 8-bit words are scrambled, and how the 8-bit words are encoded into two 10-bit characters. Figure 29 shows the default data format.

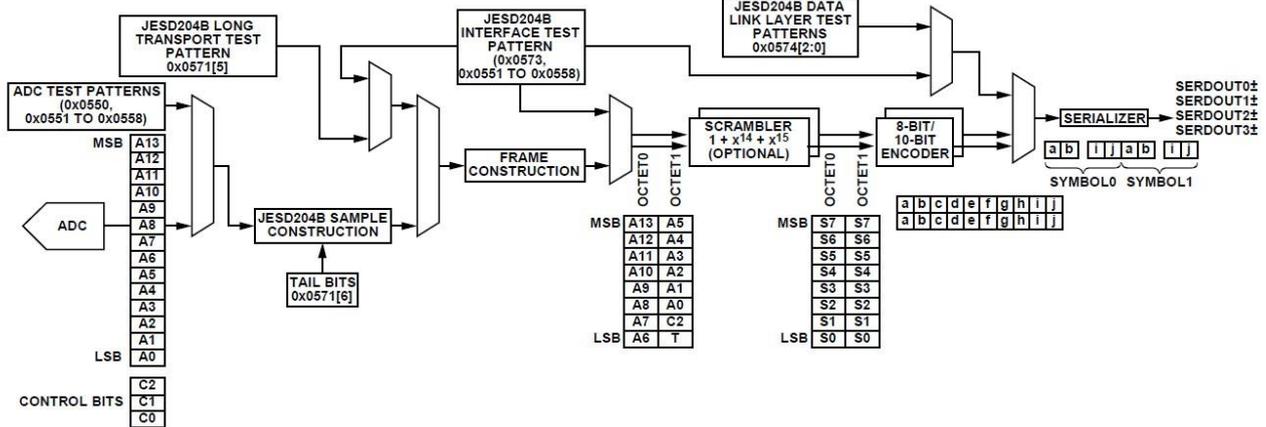


Figure 28. Display the ADC output data path for data frame transmission

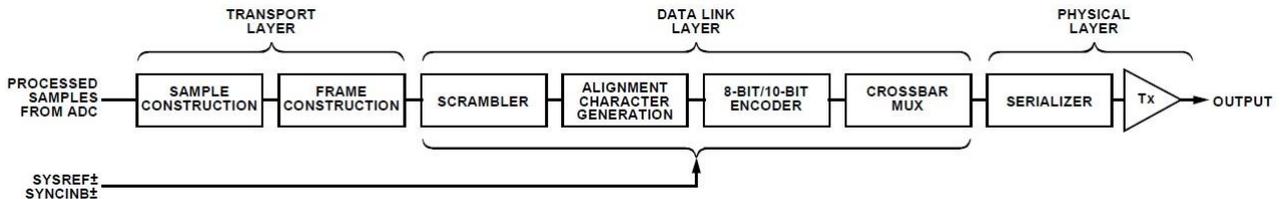


Figure 29. Data Flow

● Function Overview

The block diagram in Figure 29 shows the JESD204B data flow from sample input to physical output, which can be divided into the transport layer, data link layer, and physical layer. These layers are derived from the Open Source Initiative (OSI) model, which is widely used to describe the abstraction layers of communication systems.

1) Transport layer

The transport layer is responsible for packaging data (including samples and optional control bits) into JESD204B frames for mapping to 8-bit words. These 8-bit words are sent to the data link layer. The transport layer matches the data according to rules determined by the link parameters. Termination bits are added as needed to fill gaps. The number of termination bits in a sample can be determined using the following formula:

$$T = N' - N - CS$$

2) Data Link Layer

The data link layer is responsible for the low-level functions of transmitting data over the link, including scrambling data (optional), inserting control characters to support multi-chip synchronization/channel alignment/monitoring, and encoding 8-bit words into 10-bit symbols. The data link layer is also responsible for transmitting the Initial Channel Alignment Sequence (ILAS), which contains link configuration data that the receiver uses to verify the transport layer settings.

3) Physical layer

The physical layer consists of high-speed circuitry with a clock frequency equal to the serial clock rate. In this layer, parallel data is converted into high-speed differential serial data in 1, 2, or 4 channels.

● JESD204B Link Establishment

The ADCP9695-23 JESD204B transmitter (Tx) interface operates in Subclass 1 as defined in JEDEC standard 204B (July 2011 specification). The link establishment process consists of the following steps: code group synchronization and SYNCINB±, initial channel alignment sequence, user data, and error correction.

1) Code Group Synchronization (CGS) and SYNCINB±

CGS is the process by which the JESD204B receiver identifies the boundaries between 10-bit characters in the data stream. During the CGS stage, the JESD204B transmission module transmits $/K28.5/$ characters.

The receiver must use clock and data recovery (CDR) technology to locate $/K28.5/$ characters in the input data stream. The receiver sets the SYNCINB± pins of ADADCP9695-23 to a low level, sending a synchronization request. Then, the JESD204B Tx begins to send $/K/$ characters. Once the receiver is synchronized, it waits for the receiver to correctly receive at least 4 consecutive $/K/$ symbols, and then unsets the SYNCINB± pins. ADCP9695-23 then sends an ILAS at the next local multi-frame clock (LMFC) boundary.

The operation of the SYNCINB± pins can also be controlled by SPI. By default, the SYNCINB± signal is a differential LVDS mode signal, but it can also be driven in single-ended mode. For more information on configuring the operation of the SYNCINB± pins, refer to register 0x0572.

2) Initial Channel Alignment Sequence (ILAS)

Following CGS is ILAS, which begins at the next LMFC boundary. ILAS consists of four multiframe, with the $/R/$ character indicating the start and the $/A/$ character indicating the end. ILAS begins with the transmission of the $/R/$ character, followed by a multiframe of ramp data from 0 to 255. Link configuration data is transmitted in the second multiframe, starting with the third character. The second character is the $/Q/$ character, used to acknowledge that link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is not scrambled.

The ILAS sequence structure is shown in Figure 30. The four multi-frame sequences include:

1. Multiframe 1 begins with the character $/R/$ ($/K28.0/$) and ends with the character $/A/$ ($/K28.3/$).
2. Multiframe 2 begins with the $/R/$ character, followed by the $/Q/$ ($/K28.4/$) character, then 14 8-bit link configuration parameters (see Table 15), and finally ends with the $/A/$ character.
3. Multiframe 3 begins with the character $/R/$ ($/K28.0/$) and ends with the character $/A/$ ($/K28.3/$).
4. Multiframe 4 begins with the character $/R/$ ($/K28.0/$) and ends with the character $/A/$ ($/K28.3/$).

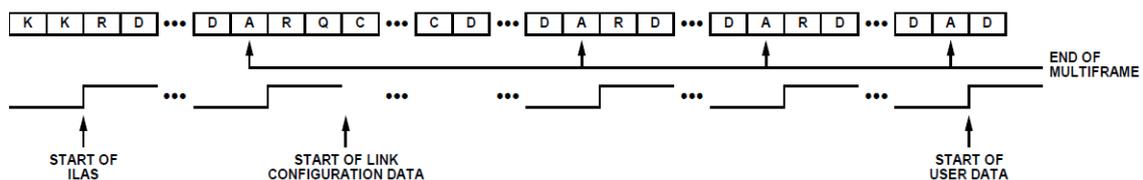


Figure 30. Initial Channel Alignment Sequence

Table 15. Control Characters Used in JESD204B

Abbreviation	Control symbols	8-bit value	10-bit value, RD=-1	10-bit value, RD=+1	Description
$/R/$	$/K28.0/$	000 11100	001111 0100	110000 1011	Multi-frame start
$/A/$	$/K28.3/$	011 11100	001111 0011	110000 1100	Channel alignment
$/Q/$	$/K28.4/$	100 11100	001111 0010	110000 1101	Link configuration data begins
$/K/$	$/K28.5/$	101 11100	001111 1010	110000 0101	Group synchronization
$/F/$	$/K28.7/$	111 11100	001111 1000	110000 0111	Frame alignment

15. User Data and Error Detection

After the initial channel alignment sequence is completed, user data is transmitted. Generally, all data within a single frame is considered user data. However, to monitor frame clock and multi-frame clock synchronization, a mechanism replaces characters with /F/ or /A/ alignment characters when data meets certain conditions. These conditions differ for unscrambled and scrambled data. Scrambling is enabled by default but can be disabled via SPI. For scrambled data, any 0xFC character at the end of a frame is replaced with /F/, and any 0xFD character at the end of a multi-frame is replaced with /A/. The JESD204B receiver (Rx) checks the received data stream for /F/ and /A/ characters, verifying that they appear only in their expected positions. If an unexpected /F/ or /A/ character is found, the receiver will enable dynamic realignment or set the SYNCINB± signal for more than four frames to initiate resynchronization. For unscrambled data, if the last character of two consecutive frames is the same, the second character will be replaced with /F/ (if it is at the end of a frame) or /A/ (if it is at the end of a multi-frame). The insertion of alignment characters can be modified via SPI. Frame Alignment Character Insertion (FACI) is enabled by default. For more information on link control, see register 0x0571.

- **8B/10B encoder**

The 8B/10B encoder converts 8-bit words into 10-bit symbols and inserts control characters into the stream as needed. The control characters used by the JESD204B are shown in Table 15. 8B/10B encoding ensures DC balance by using the same number of 0s and 1s on multiple symbols. Options for the 8B/10B interface are controllable via SPI, including bypass and inversion.

- **Physical layer (driver) output | Digital output, timing and control**

The ADCP9695-23 physical layer consists of drivers as specified in JEDEC standard 204B (July 2011). Each driver utilizes a 100Ω dynamic internal termination resistor to reduce reflection interference. A 100Ω differential termination resistor is placed at the input of each receiver to achieve a nominal receiver swing of $0.85 \times \text{DRVDD1}$ Vp-p. The swing can be adjusted via the SPI registers. AC coupling to the receiver is recommended. For more details, see registers 0x05C0 through 0x05C3.

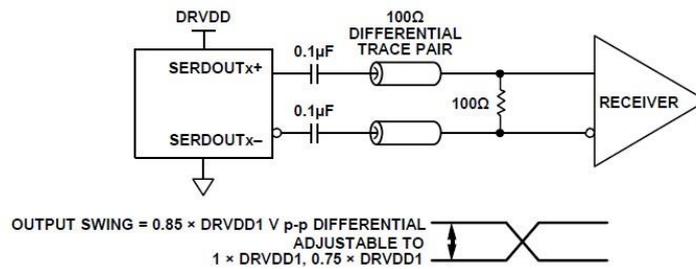


Figure 31. Example of AC-coupled digital output termination

The ADCP9695-23 digital outputs interface with custom ASIC and FPGA receivers, enabling excellent switching performance in high-noise environments. A single point-to-point network topology is recommended, with the single 100Ω differential termination resistor placed as close as possible to the receiver input. Lack of remote receiver termination or poor differential routing can lead to timing errors. To avoid such errors, trace lengths of less than 6 inches are recommended, with differential output traces close together and of equal length. Figure 32 shows an example of the ADCP9695-23 digital output data eye diagram, jitter histogram, and bathtub curve, with the channel operating at 16Gbps. The output data format is two's complement by default.

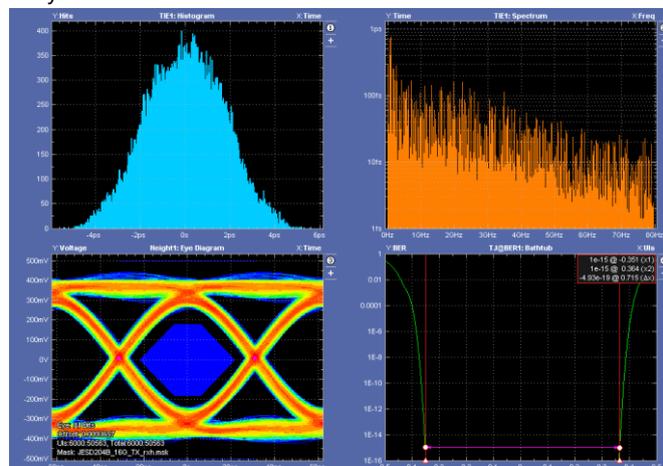


Figure 32. Digital Output Test Results: 100Ω Terminal at 16Gbps

- Phase-locked loop**

The PLL generates a clock that runs at the JESD204B channel rate. The PLL lock status can be checked in the PLL lock status bit (bit 7) of register 0x056F. Register 0x056F also has an unlocked (LOL) sticky bit (bit 3) to notify the user that an unlock has been detected. The sticky bit can be reset via a JESD204B link restart (register 0x0571=0x15, followed by register 0x0571=0x14). Bits [7:4] of the JESD204B channel rate control register 0x056E must be set to correspond to the channel rate. Table 16 shows the channel rates supported by the ADCP9695-23 using register 0x056E.

Table 16. Channel rates supported by ADCP9695-23 register 0x056E

Value	Lane speed
0x00	Lane speed = 6.75Gbps~13.5Gbps
0x10	Lane speed = 3.375Gbps~6.75Gbps
0x30	Lane speed = 13.5Gbps~15.5Gbps (default)
0x50	Lane speed = 1.6875Gbps~3.375Gbps

Table 16.1. ADCP9695-23 JESD204B Initialization

Name	Value	Description
0x1228	0x4F	Reset JESD204B startup circuit
0x1228	0x0F	JESD204B startup circuit is operating normally
0x1222	0x04	JESD204B-PLL Force Normal Operation Reset
0x1222	0x04	Reset JESD204B PLL calibration
0x1222	0x00	JESD204B PLL is operating normally
0x1262	0x08	The locking position is obviously lost
0x1262	0x00	Normal operation when the lock position is lost

Table 17 shows the supported JESD204B output configurations for a given number of virtual converters, with N'=16. Note that the serial channel rate for a given configuration should be within the supported range of 3.4Gbps to 15Gbps.

Table 17. JESD204B output configuration when N'=16¹

The number of supported virtual converters (the same as M)	JESD204B Serial Lane Rate ²	Supported extraction rate				JESD204B Transport Layer Settings ³								
		Lane speed =1.6875Gbps~3.375Gbps	Lane speed =3.375Gbps~6.75Gbps	Lane speed =6.75Gbps~13.5Gbps	Lane speed =13.5Gbps~16Gbps	L	M	F	S	HD	N	N'	CS	K
1	20xf _{OUT}	2,4,5,6,	1,2,3,	1,	N/A	1	1	2	1	0	8~16	16	0~3	See note ⁴
	20xf _{OUT}	2,4,5,6,	1,2,3,	1,	N/A	1	1	4	2	0	8~16	16	0~3	See note ⁴
	10xf _{OUT}	1,2,3,	1,	N/A	N/A	2	1	1	1	1	8~16	16	0~3	See note ⁴
	10xf _{OUT}	1,2,3,	1,	N/A	N/A	2	1	2	2	0	8~16	16	0~3	See note ⁴
	5xf _{OUT}	1,	1,	N/A	N/A	4	1	1	2	1	8~16	16	0~3	See note ⁴
	5xf _{OUT}	1,	N/A	N/A	N/A	4	1	2	4	0	8~16	16	0~3	See note ⁴
2	40xf _{OUT}	4,8,10,12	2,4,5,6	1,2,3,	1,	1	2	4	1	0	8~16	16	0~3	See note ⁴
	40xf _{OUT}	4,8,10,12	2,4,5,6,	1,2,3,	1,	1	2	8	2	0	8~16	16	0~3	See note ⁴
	20xf _{OUT}	2,4,5,6	1,2,3	N/A	N/A	2	2	2	1	0	8~16	16	0~3	See note ⁴
	20xf _{OUT}	2,4,5,6	1,2,3	N/A	N/A	2	2	4	2	0	8~16	16	0~3	See note ⁴
	10xf _{OUT}	1,2,3	1,	N/A	N/A	4	2	1	1	1	8~16	16	0~3	See note ⁴
	10xf _{OUT}	1,2,3	1,	N/A	N/A	4	2	2	2	0	8~16	16	0~3	See note ⁴
4	80xf _{OUT}	8,16,20,24	4,8,10,12	2,4,6,	2,	1	4	8	1	0	8~16	16	0~3	See note ⁴
	40xf _{OUT}	4,8,10,12,48	2,4,5,6	1,2,3,	1,	2	4	4	1	0	8~16	16	0~3	See note ⁴
	40xf _{OUT}	4,8,10,12	2,4,5,6,	1,2,3,	1,	2	4	8	2	0	8~16	16	0~3	See note ⁴
	20xf _{OUT}	2,4,5,6	1,2,3,	1,	N/A	4	4	2	1	0	8~16	16	0~3	See note ⁴
	20xf _{OUT}	2,4,5,6	1,2,3	1,	N/A	4	4	4	2	0	8~16	16	0~3	See note ⁴

¹. Due to internal clock requirements, some link parameters only support certain sampling rates.

² f_{ADC_CLK} is the ADC sampling rate; DCM = chip decimation rate; f_{OUT} is the output sampling rate = f_{ADC_CLK} / DCM ; SLR is the JESD204B serial channel rate. Due to the requirements of the internal clock divider, the following equations must be met: $SLR \geq 1.6875Gbps$ and $SLR \leq 15.5Gbps$; $SLR/40 \leq f_{ADC_CLK}$; least common multiple ($20 \times DCM \times f_{OUT} / SLR, DCM$) ≤ 64 . When $SLR \leq 15500Mbps$ and $> 13500 Mbps$, register 0x056E must be set to 0x30. When $SLR \leq 13500Mbps$ and $\geq 6750Mbps$, register 0x056E must be set to 0x00. When $SLR < 6750Mbps$ and $\geq 3375Mbps$, register 0x056E must be set to 0x10. When $SLR < 3375 Mbps$ and $\geq 1687.5 Mbps$, register 0x056E must be set to 0x50.

³. The JESD204B transport layer is described as follows: L is the number of lanes per link for each converter device; M is the number of virtual converters per converter device (virtual converters per link); F is the octet per frame; S is the number of samples transmitted per frame period

ADCP9695-23 Dual-Channel, 14-Bit, 1300 MSPS, A/D Converter

for each virtual converter; HD is high-density mode; N is the virtual converter resolution (in bits); N' is the total number of bits per sample (JESD204B word length); CS is the number of control bits per conversion sample; K is the number of frames per multiframe.

4. Only valid $K \times F$ values divisible by 4 are supported: For $F=1$, $K=20, 24, 28, 32$; For $F=2$, $K=12, 16, 20, 24, 28, 32$; For $F=4$, $K=8, 12, 16, 20, 24, 28, 32$; For $F=8$, $K=4, 8, 12, 16, 20, 24, 28, 32$; For $F=16$, $K=4, 8, 12, 16, 20, 24, 28, 32$.

● Example

This example demonstrates the flexibility of the ADCP9695-23 's digital and channel configurations with DDC options (two ADCs and two DDCs). The sampling rate is 1.3 GSPS; however, depending on the input/output speed capabilities of the receiving device, the outputs can be combined into two or four channels.

The settings are shown in Figure 33, with the following configuration:

- Two 14-bit converters at 1.3 GSPS
- Two DDC application layer modes with complex outputs (I/Q)
- Chip extraction ratio = 8
- DDC extraction ratio = 8

The JESD204B output configuration is as follows:

- Required virtual converters = 4
- Output sampling rate (f_{OUT}) = 1.3 GSPS / 8 = 162.5 MSPS

JESD204B supports the following output configurations:

- $N' = 16$ bits
- $N=14$ bits
- $L=2, M=4, F=4$ or $L=4, M=4, F=2$
- $CS=0$
- $K=32$
- Output serial line rate = 6.5Gbps per channel ($L=2$) or 3.25Gbps per channel ($L=4$)

For $L=2$, set the PLL control register 0x056E to 0x10.

For $L=4$, set the PLL control register 0x056E to 0x50.

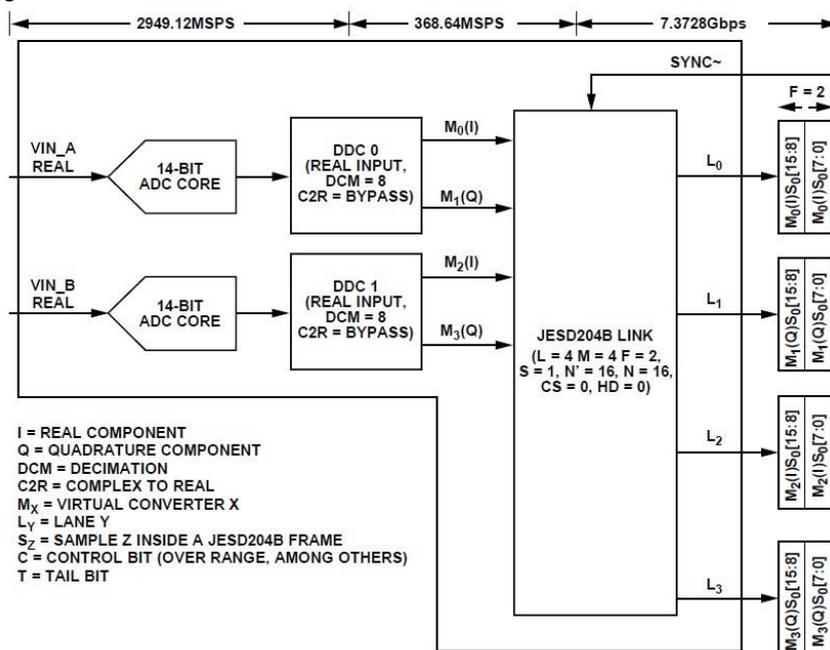


Figure 33. Two ADCs and Two DDCs

● Deterministic delay

The ADCP9695-23 supports JESD204B subclass 0 and subclass 1 operations. Register 0x0590 bits [7:5] set the subclass mode, which is set to subclass 1 operation mode by default (register 0x590, bit 5=1).

● Subclass 0 operation

If multi-chip synchronization is not required when operating in subclass 0 mode (register 0x590, bits [7:5]=000), the SYSREF input can be disconnected. In this mode, the JESD204B clock relationship between the JESD204B transmitter and receiver is arbitrary, but it does not affect the receiver's ability to capture and align channels within the link.

- **Subclass 1 operations**

The JESD204B protocol organizes data samples into octet bytes, frames, and multiframe, as described in the transport layer section. LMFC is synchronized with the start of these multiframe. In subclass 1 operation, the SYSREF signal is used to synchronize the LMFC of each device in or across multiple links, as shown in Figures 34. The JESD204B receiver uses multiframe boundaries and buffering to achieve cross-channel (even multiple device) operation and to implement a fixed delay between power cycles and link reset conditions.

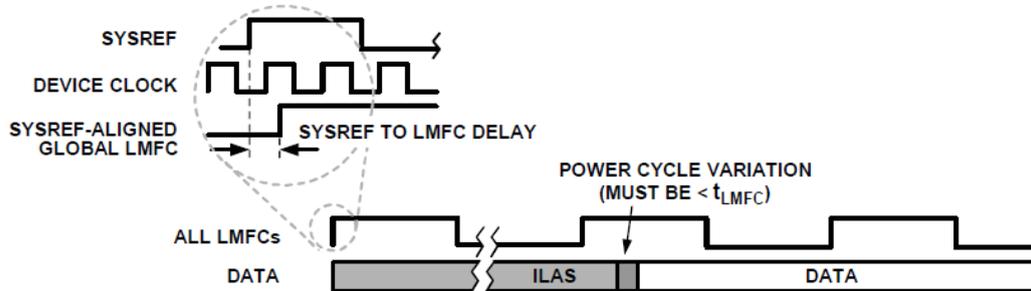


Figure 34. SYSREF and LMFC

- **Deterministic delay requirements**

Several key factors are required to implement deterministic delay in a JESD204B subclass 1 system.

- 1) The skewness of the $SYSREF_{\pm}$ signal distribution within the system must be less than the uncertainty required by the system.
- 2) Every device in the system must meet the $SYSREF_{\pm}$ setting and hold time requirements.
- 3) The total latency variation across all channels, links, and devices must be ≤ 1 LMFC period. This total latency includes both variable latency and fixed latency variations from channel to channel, link to link, and device to device within the system.

- **Set deterministic delay register**

The JESD204B receive buffer in the logic device buffers data that begins at the LMFC boundary. If the total link latency in the system is close to an integer multiple of the LMFC period, the data arrival time at the receive buffer may overlap with the LMFC boundary from one power cycle to the next. To ensure deterministic latency in this case, phase adjustment of the LMFC must be performed at the transmitter or receiver. Typically, the LMFC of the receiver is adjusted to fit the receive buffer. In the ADCP9695-23, this adjustment can be performed using the LMFC offset register (register 0x0578, bits [4:0]). This register delays the LMFC in frame clock increments, depending on the F parameter (the number of octets per channel per frame). For $F=1$, every four settings (0, 4, 8, etc.) are valid and result in a four-frame clock offset. For $F=2$, all other settings (0, 2, 4, etc.) are valid and result in a two-frame clock offset. For all other values of F, each setting results in a one-frame clock offset. As shown in Figure 35, when the link delay approaches the LMFC boundary, the local LMFC of the ADCP9695-23 can be adjusted to delay the time when data arrives at the receiver. Figure 36 shows how the receiver's LMFC is delayed to accommodate the timing of the receive buffer.

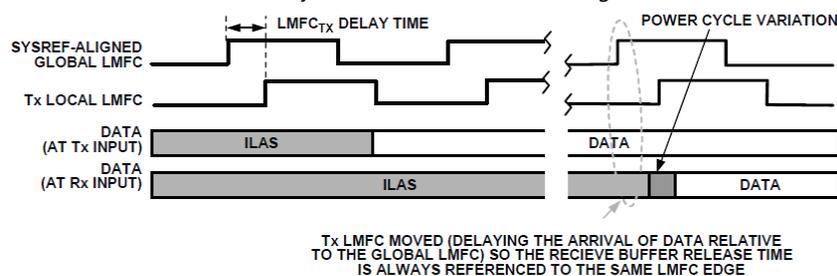


Figure 35. Adjusting JESD204B Tx LMFC in ADCP9695-23

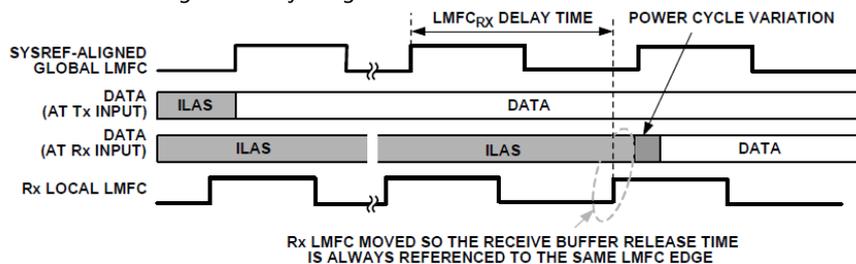


Figure 36. Adjusting the JESD204B Rx LMFC in the receiving equipment.

If the total delay in the system is not close to an integer multiple of the LMFC cycle, or if the LMFC phase at the clock source has been properly adjusted, a variable delay from one power cycle to the next can still occur. In this case, check if the SYSREF setup and hold time requirements are not being met by reading the SYSREF setup/hold monitor register (register 0x0128). This function is fully described in the SYSREF $_{\pm}$ setup/hold monitor section. If reading register 0x0128 shows a problem, it may be necessary to adjust the phase of SYSREF and/or the device clock (CLK $_{\pm}$).

16. Multi - chip synchronous setting

The flowchart in Figure 37 illustrates the internal mechanism for multi-chip synchronization in the ADCP9695-23. The synchronization mode bit (bit 0) in register 0x1FF determines the synchronization mode, and each mode involves a different application of the SYSREF signal.

- **Normal mode**

The default state of the synchronization mode bit is 0x0, which configures the ADCP9695-23 in normal synchronization mode. The JESD204B standard specifies the use of SYSREF to provide deterministic latency in a single link. Multi-chip synchronization can also be provided when applied to systems with multiple converters and logic devices. In Figure 37, this synchronization mode is referred to as normal mode. Follow the procedure outlined in the figure to ensure the ADCP9695-23 is configured appropriately.

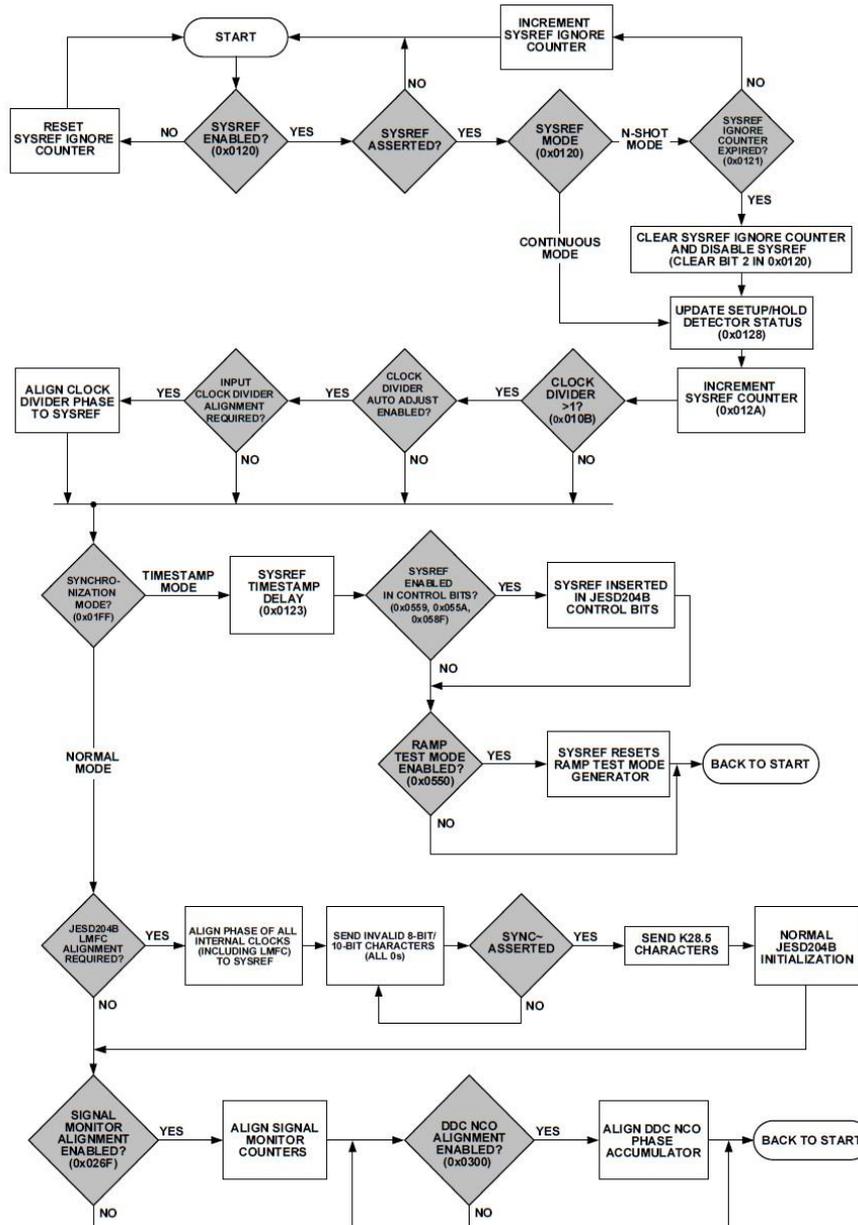


Figure 37. SYSREF captures scenes and multi-chip synchronization

- **Timestamp mode**

For the ADCP9695-23 full-bandwidth mode, the SYSREF input can also be used for timestamped samples. Timestamping is another method of multi-chip synchronization. Timestamping is particularly effective when synchronizing multiple devices to one or more logic devices; the logic devices simply buffer the data stream, identify the timestamped samples, and align them. Timestamped mode is enabled when the synchronization mode bit (register 0x01FF, bit 0) is set to 0x1. In this mode, SYSREF resets the sampling divider and the JESD204B clock, but the clock itself is not reset; instead, the corresponding sample is timestamped using the JESD204B control bits of that sample. The following additional settings are required to operate in timestamped mode:

- 1) Continuous or N-shot SYSREF must be enabled (register 0x0120, bits [2:1] are 1 or 2).
- 2) At least one control bit must be enabled (register 0x058F, bits [7:6] with a value of 1, 2 or 3).

Set the function of one of the control bits to SYSREF, as shown below:

- 1) If control bit 0 is used, register 0x0559 bits [3:0] = 5.
- 2) If control bit 1 is used, register 0x0559 bits [7:4] = 5.
- 3) If control bit 2 is used, register 0x055A bits [3:0] = 5.

Figure 38 shows how input samples that coincide with SYSREF are timestamped and ultimately output from the ADC. In this example, there are two control bits, and control bit 0 indicates which sample coincides with the rising edge of SYSREF.

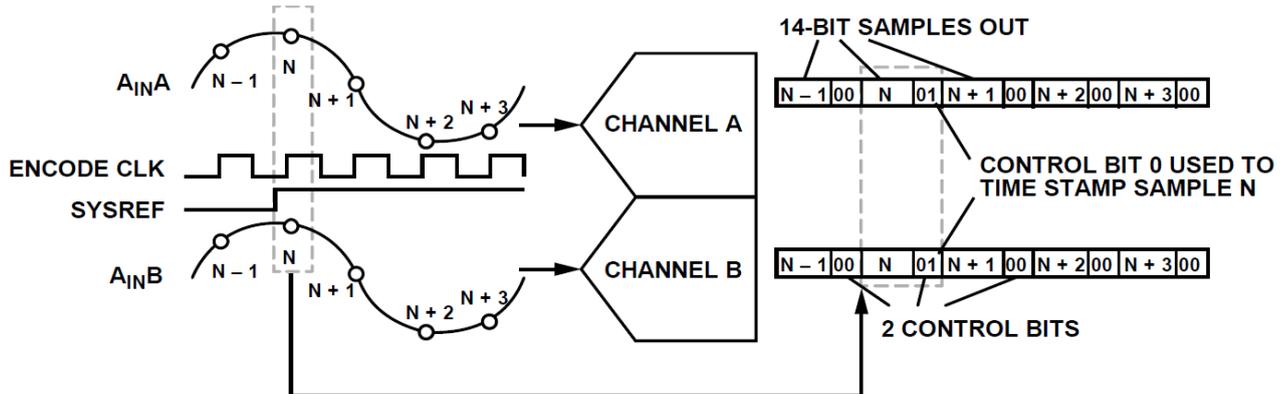


Figure 38. Timestamp CS=2 (register 0x058F, bits [7:6]=2), control bit 0 is SYSREF (register 0x0559, bits [3:0]=5)

The pipeline delay is the same for each channel. If needed, the timing of timestamped samples can be adjusted using the SYSREF timestamp delay register (register 0x0123). Timestamps are not supported in any ADCP9695-23 operating mode using decimation.

- **SYSREF input**

The SYSREF input signal serves as a high-precision system reference for deterministic delay and multi-chip synchronization. The ADCP9695-23 accepts single or periodic input signals. The SYSREF mode selection bit (register 0x0120, bits [2:1]) selects the input signal type and activates the SYSREF state machine when set. If in single (or N) mode (register 0x0120, bits [2:1] = 2), the SYSREF mode selection bit is cleared after an appropriate SYSREF edge is detected. The minimum pulse width is two $CLK \pm$ cycles. If the clock divider (register 0x010B, bits [3:0]) is set to a value other than divide by 1, this minimum pulse width requirement is multiplied by the division ratio (e.g., if set to divide by 8, the minimum pulse width is $16 CLK \pm$ cycles). When using a continuous SYSREF signal (register 0x0120, bits [2:1] = 1), the period of the SYSREF signal must be an integer multiple of LMFC. LMFC can be derived using the following formula:

$$LMFC = \text{ADC clock} / (S \times K)$$

Where: **S** is the number of samples per converter.

K is the number of frames in each multi-frame module.

When in sampling synchronization mode (normal mode, register 0x01FF, bit 0 = 0x0), the input clock divider, DDC, signal monitor, and JESD204B link all use the $SYSREF_{\pm}$ input for synchronization. The $SYSREF_{\pm}$ input can also be used to timestamp ADC samples or provide synchronization for multiple ADCP9695-23 devices. To achieve the highest level of timing accuracy, $SYSREF_{\pm}$ must meet setup and hold requirements relative to the CLK_{\pm} input.

- **SYSREF control function**

SYSREF, along with the input clock (CLK), is used as part of the synchronous timing interface and requires setup and hold times of -65ps and 95ps relative to CLK (see Figure 39). The ADCP9695-23 has several features to help customers meet these requirements. First, the SYSREF sampling event can be defined as a synchronous low-to-high transition or a synchronous high-to-low transition. The ADCP9695-23 allows sampling of the SYSREF signal using either the rising or falling edge of the input clock. Figures 39–42 illustrate all four possible combinations. The ADCP9695-23 has the ability to ignore a programmable number (up to 16) of SYSREF events. (The SYSREF ignoring function is enabled by setting bits [2:1] of the SYSREF mode register 0x0120 to 2'b10, which is labeled as N-shot mode). This feature is very useful for handling periodic SYSREF signals that require time

to stabilize after startup. Ignoring SYSREF before the clock in the system stabilizes avoids inaccurate SYSREF triggering. Figure 43 shows an example when the three SYSREF events are ignored.

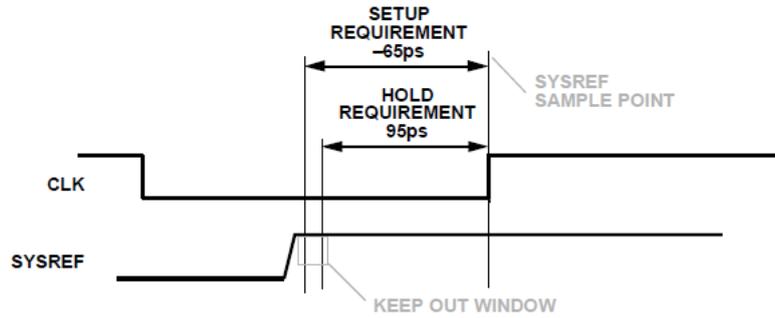


Figure 39. SYSREF setup and hold time requirements. SYSREF is captured using a rising edge clock.

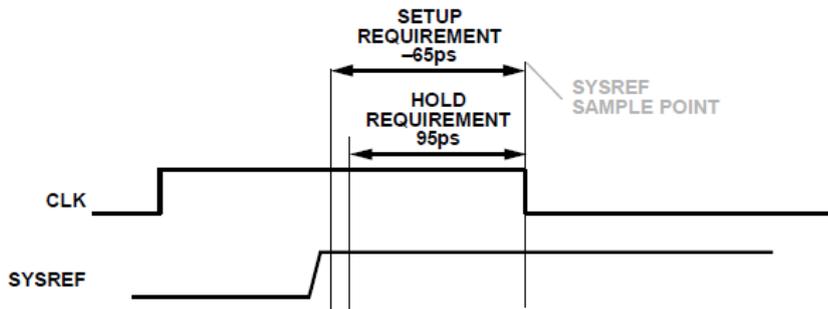


Figure 40. Capturing the low-to-high transition of SYSREF using the falling edge of the clock (register 0x0120, bit 4 = 1'b0, register 0x0120, bit 3 = 1'b1)

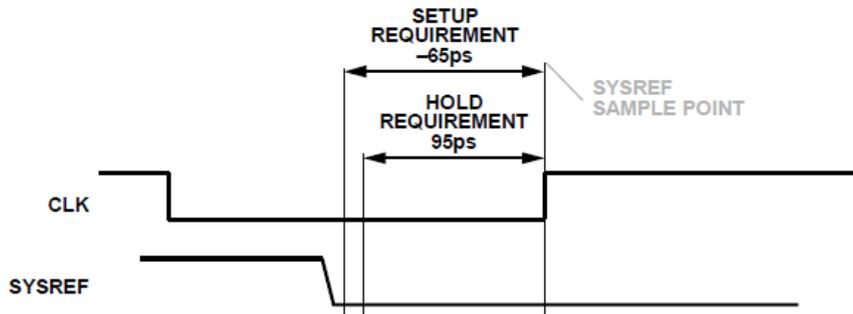


Figure 41. Capturing the high-to-low transition of SYSREF using the rising edge of the clock (register 0x0120, bit 4 = 1'b1, register 0x0120, bit 3 = 1'b0)

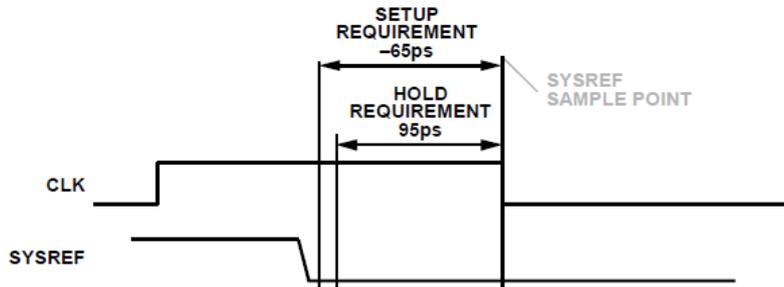


Figure 42. Capturing the high-to-low transition of SYSREF using the falling edge of the clock (register 0x0120, bit 4 = 1'b1, register 0x0120, bit 3 = 1'b1)

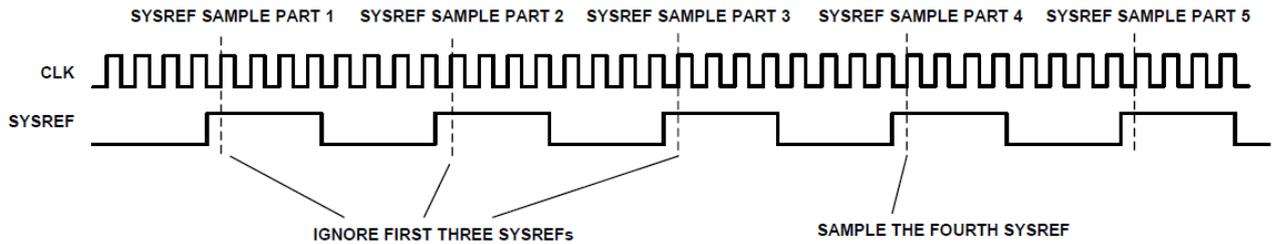


Figure 43. Example of SYSREF ignoring (SYSREF ignores counter, register 0x0121, bits [3:0]=3)

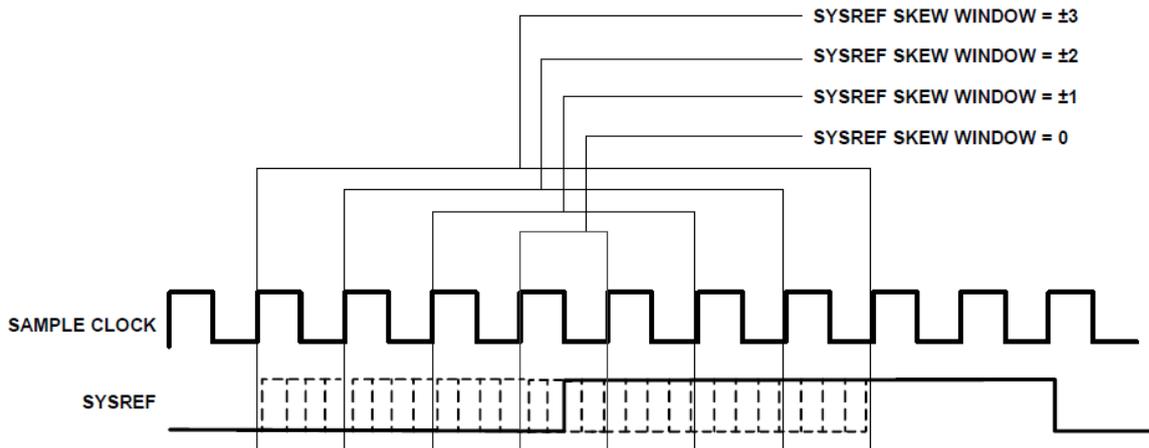


Figure 44. SYSREF Skew Window

In continuous SYSREF mode (register 0x0120, bits [2:1]=1), the ADCP9695-23 monitors the position of the internal LMFC and SYSREF edges. If SYSREF is captured with a clock edge other than the clock edge aligned with the LMFC, the ADCP9695-23 initiates resynchronization of the link. Because the ADCP9695-23 has input clock rates up to 2GHz, it provides another SYSREF-related function to accommodate periodic SYSREF signals when periodic precision capture is impractical or unnecessary. In this case, the ADCP9695-23 has a programmable SYSREF offset window, allowing the internal divider to remain undisturbed unless SYSREF appears outside the offset window. The SYSREF resolution skew window is set within the sampling clock cycle. If the SYSREF negative skew window is 1 and the positive skew window is 1, the total skew window is ± 1 sampling clock cycle. This means that as long as SYSREF is captured within ± 1 sampling clock cycle of the clock aligned with LMFC, the link continues to operate normally. If SYSREF has jitter, which could cause misalignment between SYSREF and LMFC, this feature allows the system to continue operating without resynchronization, while allowing the device to continue monitoring for larger timing errors not caused by jitter. For ADCP9695-23, the positive and negative skew windows are controlled by SYSREF (register 0x0122, bits [3:2]) and SYSREF (register 0x0122, bits [1:0]). Figure 4 shows the position information of the offset window settings relative to the internal divider phase 0. Negative skew is defined as occurring before the internal divider reaches phase 0, while positive skew is defined as occurring after the internal divider reaches phase 0.

- **SYSREF \pm Create and maintain window monitor**

To ensure effective SYSREF signal capture, the ADCP9695-23 features a SYSREF \pm setup and hold window monitor. This feature allows system designers to determine the position of the SYSREF \pm signal relative to the CLK \pm signal by reading the setup/hold margin on the register read interface. Figures 45 and 46 show the setup and hold status values for different stages of SYSREF \pm . The setup time detector returns the state of the SYSREF \pm signal before the CLK \pm edge, while the hold time detector returns the state of the SYSREF signal after the CLK \pm edge. Register 0x0128 stores the state of SYSREF \pm and informs the user whether the SYSREF \pm signal has been captured by the ADC. Table 18 shows a description of the contents of register 0x128 and how to interpret them.

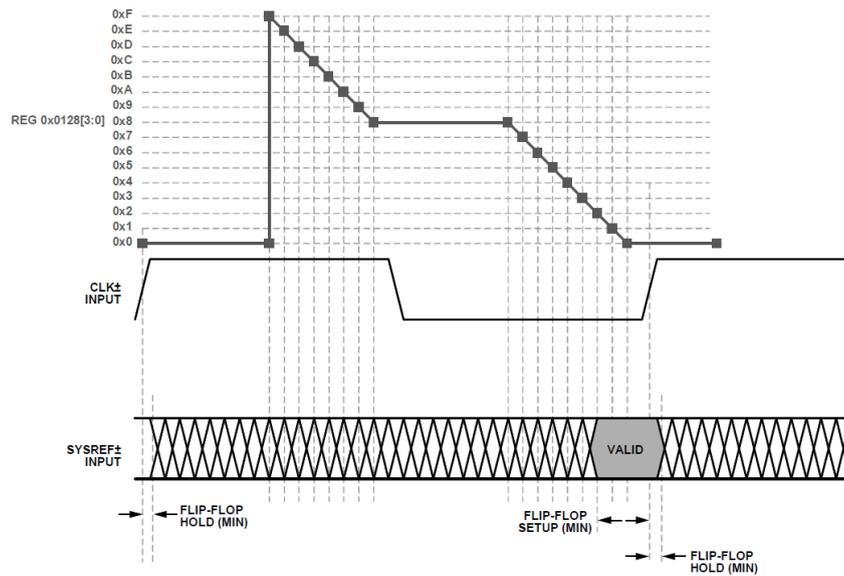


Figure 45. SYSREF ± Setup Time Detector

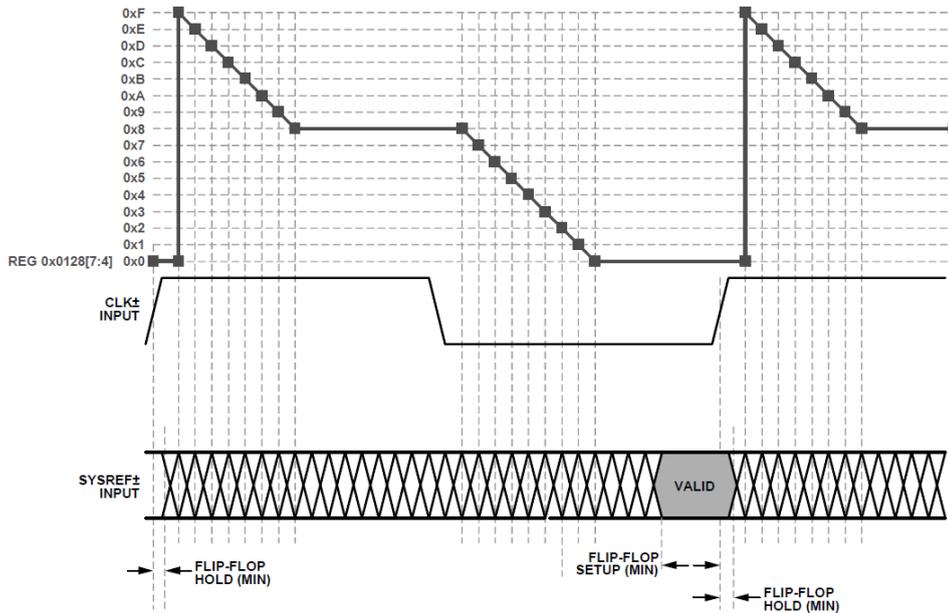


Figure 46. SYSREF ± Hold Time Detector

Table 18. SYSREF ± Setup/Hold Monitor, 0x0128

Register 0x0128, bits [7:4] hold state	Register 0x0128, bits [3:0] set status	Description
0x0	0x0 to 0x7	There may be a configuration error. The smaller this number, the smaller the setting margin.
0x0 to 0x8	0x8	No settings or holding errors (optimal holding balance).
0x8	0x9 to 0xF	No settings or hold error (optimal settings and hold margin).
0x8	0x0	No settings or error (optimal settings margin)
0x9 to 0xF	0x0	There may be a holding error. The larger this number, the smaller the holding margin.
0x0	0x0	There may be a setup or retention error.

Note: ① All ports marked with positive and negative (such as SYSREF±, etc.) should be used accurately according to the positive and negative markings. Under normal circumstances, register 0x0120[4] is 0; when the SYSREF± pin is reversed with the ± of the external clock circuit, register 0x0120[4] needs to be set to 1. ② It is recommended to set the setup and hold state to around 0x0128=0x8F (0x8F~0x8C). If the above conditions cannot be met, the setup and hold state can be set to 0x0128=0x80, but the SYSREF± signal needs to be adjusted left and right (moved more than 100ps left and right) to ensure that the state displayed in register 0x0128 is 0x80, or the SYSREF± signal is displayed as 0x80 when shifted left and

0x8F~0x8D when shifted right.

Suggested steps

Step 1: Confirm that the reference signal SYSREF is connected to the ADC port with the correct polarity. Reversing the polarity may cause synchronization errors.

Step 2: Adjust the delay between SYSREF and the clock to obtain the correct setup and hold time, and read back the 0x0128 register. For details, please refer to the SYSREF \pm Setup and Hold Window Monitor.

Step 3: Set register 0x0120<2:1> to select the synchronization mode. Configuring it to 04 is one-shot mode, and configuring it to 02 is continuous synchronization mode. At this time, the SYSREF cycle must be an integer multiple of the LMFC cycle.

To simultaneously perform DDC synchronization, register 300<1:0> needs to be enabled to select the DDC synchronization mode. 0x0300<1:0> configured as 03 is one-shot mode; synchronization is completed by issuing a synchronization SYSREF pulse after all ADCs are configured. 0x0300<1:0> configured as 01 is DDC Continuous mode. In this mode, the SYSREF frequency must meet the following two restrictions: the SYSREF period must be an integer multiple of the LMFC period, and it must also be an integer multiple of the NCO frequency.

17. Power - on configuration

Step 1: After the external clock and power supply stabilize, configure register 0x00 to reset the SPI of the chip.

Step 2: Configure the ADC's operating mode register.

Step 3: Reset the ADC Datapath.

Step 4: Set the multi-chip synchronization mode.

Example: Sampling rate 1300MSPS, two DDC real inputs, complex outputs, HB1+HB2+HB3 enabled, output decimation ratio 8, synchronization mode changed to one-shoot, wait for the clock, power supply and other ADC peripheral environment to stabilize before configuring the ADC:

● Preparation

- 1) Check if the \pm pin of the clock chip is consistent with SYSREF \pm . If they are consistent, set register 0x0120 to 0x04; otherwise, set it to 0x14.
- 2) In addition to meeting the above conditions, the setup and hold time between SYSREF and the clock must also be met. The setup and hold time status can be viewed by reading register 0x0128.

● Suggested steps

- 1) Register 0x00 is configured to 0x81 (SPI reset)
- 2) Wait 10ms
- 3) 0x0738 = 0x18; (Optional, can be ignored if the working environment is stable and there is no interference such as clock or power supply interference)
- 4) 0x073E = 0x08; (Optional, same as above)
- 5) Register 0x200 is configured to 0x22 (two DDC modes)
- 6) Register 0x201 is configured to 0x03 (chip extraction rate 8)
- 7) Register 0x310 is configured as 0x41 (6dB gain, DDC0: HB1+HB2+HB3, decimation rate 8)
- 8) Register 0x311 is configured to 0x00 (DDC0 input comes from channel A)
- 9) 0x316-0x31B Configure the NCO frequency in DDC0
- 10) Register 0x330 is configured as 0x41 (6dB gain, DDC1: HB1+HB2+HB3, decimation rate 8)
- 11) Register 0x331 is configured as 0x05 (decimation rate 8, DDC1 input from channel B)
- 12) 0x336-0x33B Configure the NCO frequency in DDC0
- 13) Register 0x58B is configured to 0x11 (L=2, scrambling enabled)
- 14) Register 0x58C is configured to 0x03 (F=4)
- 15) Register 0x58E is configured to 0x03 (M=4)
- 16) Register 0x56E is configured as 0x01 (3.375Gbps < line rate 6.5Gbps < 6.75Gbps)
- 17) Register 0x01 is configured to 0x02 (Datapath soft reset)
- 18) Register 0x0120 is configured to 0x00; synchronization is disabled
- 19) Register 0x0300 is configured to 0x00; DDC synchronization is disabled
- 20) 0x0001 = 0x02; Soft reset
- 21) Wait 10ms
- 22) Register 0x300 is configured as 0x03 (one-shoot mode)
- 23) Register 0x0121 is configured to 0x00; one-shoot mode is set
- 24) Register 0x0120 is configured to 0x04 (one-shoot mode)
- 25) Configure the clock chip to send SYSREF pulses

Note: Configuring 0x0738 to 0x18 and 0x073E to 0x08 will disable some online algorithms, and the SNR will decrease by about 1dB, but the ADC's anti-interference capability will be enhanced.

When the device is not powered off, after changing the working mode of the digital function, the recommended synchronous configuration steps are as follows: to configure the digital function mode; the user should make the configuration according to the actual situation. 1)

Configure 204B mode and lane speed; users configure lane speed according to their actual needs

- 2) 0x0120 = 0x00; Ensure synchronous shutdown
- 3) 0x0300 = 0x00; Ensure DDC is synchronously turned off
- 4) 0x0001 = 0x02; Soft reset
- 5) It is recommended to wait 10ms
- 6) 0x0300 = 0x03; Enable DDC synchronization, one-shoot
- 7) 0x0121 = 0x00; Set one-shoot mode
- 8) 0x0120 = 0x04; Enable synchronization
- 9) Configure the clock chip to send SYSREF pulses

18. Register Description

The ADC's SPI consists of three pins: SCLK, SDIO, and CSB (see Table 19). The SCLK (Serial Clock) pin is used to synchronize data read from and written to the ADC. The SDIO (Serial Data Input/Output) pin is a dual-function pin that can be used to send data to or read data from the internal ADC memory-mapped register. The CSB (Chip Select) pin is an active-low control pin that enables or disables read/write cycles.

Table 19. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. Serial shift clock input, used to synchronize read and write operations of the serial interface.
SDIO	Serial data input/output. Dual-function pin; typically used as either input or output, depending on the specific application. The relative position of the sent command and timing frame.
CSB	Chip select signal. Active low, this control pin is used to select the read/write cycle.

The falling edge of CSB and the rising edge of SCLK together determine the start of the frame. Figure 47 is a serial timing diagram.

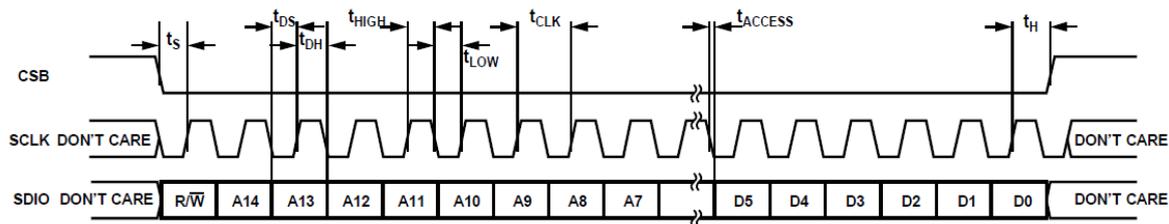


Figure 47. Serial Interface Timing Diagram

All data consists of 8-bit words. The first bit of each byte of serial data indicates whether a read or write command is issued. This allows the data transmission direction of the SDIO pin to be changed from input to output. In addition to the word length, the instruction cycle also determines whether the serial frame is a read or write operation, thus enabling chip programming and data retrieval from on-chip memory via the serial port. If the instruction is a readback operation, executing the readback will change the SDIO pin from input to output at the appropriate position in the serial frame. Data can be sent in either MSB-first or LSB-first mode. The chip defaults to MSB-first mode upon power-up, but the data transmission mode can be changed via the SPI port configuration register.

• Memory mapping

Each address in the memory-mapped register table is 8 bits. The memory map is divided into the following parts:

- 1) Analog circuit SPI registers (0x0000 to 0x000F)
- 2) Clock/SYSREF/Chip Power-Down Pin Control Register (0x003F to 0x01FF)
- 3) Chip operating mode control registers (0x0200 to 0x0201)
- 4) Fast detection and signal monitoring control registers (0x0245 to 0x027A)
- 5) DDC function registers (0x0300 to 0x03CD)
- 6) Digital output and test mode registers (0x0550 to 0x05CB and 0x1222 to 0x1262)
- 7) Programmable filter control and coefficient registers (0x0DF8 to 0x0F7F)
- 8) VREF/Analog Input Control Registers (0x18A6 to 0x1A4D and 0x0701 to 0x073B)

The memory-mapped registers record the hexadecimal value of each address in detail. For example, the default hexadecimal value for register address 0x0561 is 0x01, which means the least significant bit is 1 and the rest are 0.

• Default value

After a reset, critical registers are loaded with their default values. The default values for these registers are stored in the memory-mapped register table.

• Logic Level

The logic level terminology is explained as follows:

- 1) "Bit set" means "the bit has been set to logic 1" or "the bit has been written to logic 1".
- 2) "Clear bit" means "this bit has been set to logic 0" or "this bit has been written to logic 0".
- 3) X represents an irrelevant bit.

• Channel-specific registers

Some channel setting functions, such as the buffer control register (register 0x1A4C), can have different values for each channel. In this case, the register and bit addresses are essentially the same for each channel. These registers and bits can be accessed by setting the appropriate channel A or channel B register 0x0008. If both bits are set, subsequent writes will affect the registers of both channels. During a read cycle, only channel A or channel B is set when reading the register. If both bits are set during an SPI read cycle, the value for channel A is returned.

• Memory-mapped register table

Address	Name	Bit	Bit Name	Set Up	Description	Reset	Access
0x0000	SPI Configuration A	7	Soft reset mirror (Self-reset)	0 1	When a soft reset is issued, the user must wait 5 milliseconds before writing to other registers to allow sufficient time for the bootloader to complete. Do nothing. Reset SPI and registers (self-clear).	0x0	R/W Self-reset
		6	LSB Priority Mirroring	1 0	For all SPI operations, the least significant bit is shifted first. For all SPI operations, the most significant bit is shifted first.	0x0	R/W
		5	Address boosting mirror	0 1	Multi-byte SPI operations cause the address to automatically decrement. Multi-byte SPI operations cause the address to increment automatically.	0x0	R/W
		[4:3]	Reserve		Reserved.	0x0	Read
		2	Address Improvement	0 1	Multi-byte SPI operations cause the address to automatically decrement. Multi-byte SPI operations cause the address to increment automatically.	0x0	R/W
		1	LSB priority	1 0	For all SPI operations, the least significant bit is shifted first. For all SPI operations, the most significant bit is shifted first.	0x0	R/W
		0	Soft reset (Self-reset)	0 1	When a soft reset is issued, the user must wait 5 milliseconds before writing to other registers to allow sufficient time for the bootloader to complete. Do nothing. Reset SPI and registers (self-clear).	0x0	Read / Write, Self-Reset
		0x0001	SPI Configuration B	[7:2]	Reserve		Reserved.
1	Data path soft reset (self-clearing)			0 1	Normal operation. Data path soft reset (self-clearing).	0x0	Read / Write, Self-Reset
0	Reserve				Reserved.	0x0	Read
0x0002	Chip configuration (local)	[7:2]	Reserve		Reserved.	0x0	Read
		[1:0]	Channel power mode	00 10 11	Channel power mode. Normal mode (power on). Standby mode; disable digital data path clock; enable JESD204B interface. Power-down mode; disable digital data channel clock; digital data path hold reset; disable JESD204B interface.	0x0	R/W
0x0008	Device index	[7:2]	Reserve		Reserved.	0x0	Read
		1	Channel B	0 1	ADC Core B does not receive the next SPI command. ADC Core B receives the next SPI command.	0x0	Read
		0	Channel A	0 1	ADC Core B does not receive the next SPI command. ADC Core B receives the next SPI command.	0x1	R/W
0x000A	Scratch pad	[7:0]	Grabbing board		Chip grabbing board register. This register provides a consistent memory location for software debugging.	0x0	R/W
0x000B	SPI revision	[7:0]	SPI Revision	0x01 00000001	SPI revision register. Version 1.0 (Revised) 1.0 (Revised).	0x1	Read
0x000C	Vendor ID LSB	[7:0]	Supplier ID LSB		Supplier ID[7:0]	0x56	Read
0x000D	Vendor ID	[7:0]	Supplier ID		Supplier ID[15:8]	0x04	Read

	MSB		MSB				
0x000F	Transfer	[7:1]	Reserve		Reserved.	0x0	Read
		0	Chip conversion	0	Self-reset chip conversion bit. When DDC phase update mode (register 0x0300 , bit 7) = 1 , this bit is used to update the DDC FTW/POW/MAW/MBW increment and phase offset registers, making it possible to synchronously update the DDC mixer frequency. This bit is also used to update the coefficients of the programmable filter (PFILT). Do nothing. The bit is only cleared after the transfer is complete.	0x0	R/W
				1	The self-clear bit is used to synchronize data transfer from the master register to the slave register.		

● **Clock/SYSREF/Chip Power-Down Pin Control Register**

Address	Name	Bit	Bit Name	Set Up	Description	Reset	Access
0x003F	Chip PDWN pin (local)	7	PDWN packaging disabled for local chips	0 1	The function is determined by register 0x0040 , bits [7:6] . Enable power-down pin (PDWN/STBY) (default). Disable / ignore the power-down pin (PDWN/STBY)	0x0	R/W
		[6:0]	Reserve		Reserved.	0x0	Read
0x0040	Chip Pin Control 1	[7:6]	Chip PDWN pin function	00 01 10	External power-down pin function. The external power-down pin (PDWN/STBY) has higher priority than the channel power-on mode bit. The PDWN/STBY pin is only used in register 0x0040 , with bits [7:6] = 00 or 01. Power-down pin (default). Use an external power-down pin (PDWN/STBY) to bring the chip into full power-down mode. Standby pin. Use an external power-down pin (PDWN/STBY) to put the chip into standby mode. Disable pins. Ignore power-down pins (PDWN/STBY).	0x0	R/W
		[5:3]	Chip FD_B/GPIO_B0 pin functions	000 004 110 111	Quickly detect the function of B/GPIO B0 pin. Quickly detect the B output. JESD204B LMFC output. The pin function is determined by register 0x0041 , bits [7:4]. Disabled. Weak power-down configuration is set to input (default).	0x7	R/W
		[2:0]	Chip FD_A/GPIO_A0 functions	000 001 110 111	Quickly detect the function of A/GPIO A0 pin. Quickly detect the output of A. JESD204B LMFC output. The pin function is determined by register 0x0041 , bits [3:0] . Disabled. Weak power-down configuration is set to input (default).	0x7	R/W
0x0041	Chip Pin Control 2	[7:4]	Chip FD_B/GPIO_B0 functions	0000 0001 1000 1001	Quickly detect the auxiliary function of B/GPIO B0 pin (only used when register 0x0040 , bits [5:3]=110). Chip GPIO B0 input (NCO channel selection). Chip-based input transmission. The next trigger output of the master controller (MNT0). Subordinate to the next trigger input (SNTI).	0x0	R/W
		[3:0]	Auxiliary functions of chip FD_A/GPIO_A	0000 0001	Quick detection of A/GPIO B0 pin auxiliary function (only used in register 0x0040 , bits [2:0]=110). Chip GPIO A0 input (NCO channel selection). Chip-based input transmission.	0x0	R/W

			0 pins	1000 1001	The next trigger output of the master controller (MNTO). Subordinate to the next trigger input (SNTI).		
0x0108	Clock divider control	[7:3]	Reserve		Reserved.	0x0	Read
		[2:0]	Input clock divider (CLK+pins)	00 01 11	1 divider 2- frequency divider 4 -way crossover	0x0	R/W
0x0109	Clock divider phase (local)	[7:4]	Reserve		Reserved.	0x0	Read
		[3:0]	Clock divider phase offset	0000 0001 0010 ... 1110 1111	0 input clock cycle delay. ½ input clock cycle delay (reverse clock). 1 Input clock cycle delay. ... 7 Input clock cycle delay. 7½ input clock cycle delay.	0x0	R/W
0x010A	Clock divider and SYSREF control	7	Clock divider automatic phase adjustment enabled		Automatic phase adjustment of the clock divider is enabled. When enabled, register 0x0129 , bits [3:0] contain the phase of the divider captured by SYSREF . Actual divider phase offset = register 0x0129 , bits [3:0] + register 0x0109 , bits [3:0] . SYSREF does not change the clock divider phase (disabled). SYSREF automatically adjusts the clock divider phase (enabled).	0x0	R/W
		[6:4]	Reserve		Reserved.	0x0	Read
		[3:2]	Clock divider negative skew window	00 01 10 11	Clock divider negative skew window (measures ½ of the input device clock). Ignores ½ clock cycles preceding the input device clock, ignoring captured SYSREF transitions. Only used when register 0x010A, bit 7 = 1. Register 0x010A, bits [3:2] + Register 0x010A, bits [1:0] < Register 0x0108 , bits [2:0] . Skew allows some uncertainty in the SYSREF sample without interfering with the input clock divider. Furthermore, SYSREF must be disabled when changing the control field (register 0x0120 , bits [2:1] = 0x0). 00 No negative tilt; SYSREF must be captured accurately. 01 Half of the devices have a negative clock tilt. 10 1. Negative clock skew of the device. 11 1.5 Device clock has a negative tilt.	0x0	R/W
		[1:0]	Clock divider positive skew window	00 01 10 11	Clock divider positive skew window (measures ½ input device clock). Number of clock cycles after the input device clock by which captured SYSREF transitions are ignored. Only used when register 0x010A, bit 7=1 . Register 0x010A, bits [3:2] + Register 0x010A, bits [1:0] < Register 0x0108 , bits [2:0] . Skew allows some uncertainty in SYSREF sampling without interfering with the input clock divider. Furthermore, SYSREF must be disabled when changing the control field (register 0x0120 , bits [2:1]=0x0). 00 No negative tilt; SYSREF must be captured accurately. 01 Half of the equipment clocks are tilting. 10 1. The device clock is tilted. 11 1.5 The device clock is tilting.	0x0	R/W

0x010B	Clock divider SYSREF status	[7:4]	Reserve		Reserved.	0x0	Read
		[3:0]	Clock divider SYSREF offset		Clock divider phase state (measured over 1/2 clock cycle). Phase offset is applied to the internal clock divider phase that captures the SYSREF signal. Used only when register 0x010A , bit 7 = 1. When register 0x010A , bit 7 = 1 , register 0x010A , bits [3:2] = 0 decimal, register 0x10A , bits [1:0] = 0 decimal, clock divider SYSREF offset = register 0x0129 , bits [3:0] .	0x0	Read
0x0110	Clock delay control	[7:3]	Reserve		Reserved.	0x0	Read
		[2:0]	Clock delay mode selection	000 010 011 100 110	Clock delay mode selection. Used in conjunction with registers 0x0111 and 0x0112 . No clock delay. Fine-grained delay: Only 0 to 16 delay steps are valid. Fine delay (lowest jitter): Only 0 to 16 delay steps are effective. Fine-grained delay: All 192 delay steps are valid. Fine-grained delay enabled (all 192 delay steps are enabled). Ultra-fine-grained delay enabled (all 128 delay steps are enabled).	0x0	R/W
0x0111	Clock super fine delay (local)	[7:0]	Ultra-fine clock delay adjustment		Clock Ultra-Fine Delay Adjustment. This is an unsigned control used to adjust the ultra-fine sampling clock delay in 0.25ps steps. These bits are only used in register 0x0110 , with bits [2:0] = 010 or 110 . 0x00=0 delay steps ... 0x08 = 8 delay steps ... 0x80=128 delay steps	0x0	R/W
0x0112	Clock fine delay (local)	[7:0]	Set fine clock delay		Fine-tuning the clock delay. This is an unsigned control used to adjust the fine-tuning sampling clock offset in 1.725ps steps. These bits are only used in register 0x0110 , bits [2:0] = 0x2 , 0x3 , 0x4 , or 0x6 . Minimum value = 0. Maximum value = 192. Increment = 1. Units are delay steps. 0x00 = 0 delay steps ... 0x08 = 8 delay steps ... 0xC0=192 Delay steps	0xC0	R/W
0x011B	Clock status	[7:1]	Reserve		Reserved.	0x0	Read
		0	Input clock detection	0 1	Clock detection status. Input clock not detected. Detect / lock the input clock.	0x0	Read
0x011C	Clock Duty Cycle Stabilizer 1 control (local)	[7:2]	Reserve		Reserved.	0x0	R/W
		1	DCS1 enabled	0 1	Clock DCS1 is enabled. DCS1 bypass. DCS1 is enabled.	0x1	R/W
		0	DCS1 powered on	0 1	Clock DCS1 is powered on. DCS1 lost power. DCS1 is powered on.	0x1	R/W
0x011E	Clock Duty Cycle Stabilizer 2	[7:2]	Reserve		Reserved.	0x0	R/W
		1	DCS2 enabled	0 1	Clock DCS2 is enabled. DCS2 bypass. DCS2 is enabled.	0x1	R/W
		0	DCS2		Clock DCS2 is powered on.	0x1	R/W

	control		powered on	0 1	DCS2 lost power. DCS2 is powered on.		
0x0120	SYSREF Control 1	7	Reserve		Reserved.	0x0	Read
		6	SYSREF ± flag reset	0 1	Normal operation. SYSREF± flag retain reset (set / retain error flag clear).	0x0	R/W
		5	Reserve		Reserved.	0x0	R/W
		4	SYSREF ± Conversion Selection	0 1	When using the selected CLK± edge, SYSREF± is effective during low-to-high transitions. To change this setting, SYSREF± mode selection must be disabled. When using the selected CLK± edge, SYSREF± is effective during low-to-high transitions. To change this setting, SYSREF± mode selection must be disabled.	0x0	R/W
		3	CLK± Edge Selection	00 01	on the rising edge of the CLK± input. on the falling edge of the CLK± input.	0x0	R/W
		[2:1]	SYSREF ± mode selection	0 1 10	Disable continued N-shot	0x0	R/W
		0	Reserve		Reserved.	0x0	Read
0x0121	SYSREF Control 2	[7:4]	Reserve		Reserved.	0x0	Read
		[3:0]	SYSREF N- shot ignore counter selection	0000 0001 0010 0011 ... 1110 1111	Only the next SYSREF± transformation (do not ignore). Ignore the first SYSREF± transformation. Ignore the first two SYSREF± transformations. Ignore the first three SYSREF± transformations. ... Ignore the first 14 SYSREF ± transformations. Ignore the first 15 SYSREF ± transformations.	0x0	R/W
0x0122	SYSREF Control 3	[7:4]	Reserve		Reserved.	0x0	Read
		[3:2]	SYSREF window negative	00 01 10 11	The number of clock cycles of the captured SYSREF transition is ignored before the sampling clock. No negative skew; SYSREF must be captured accurately. A sample clock with negative skew. Two sample clocks with negative skew. Three sample clocks with negative skew.	0x0	R/W
		[1:0]	SYSREF window is		The number of clock cycles of the captured SYSREF transition is ignored before the sampling clock. No positive skew; SYSREF must be captured accurately. A sample clock with positive skew. Two sample clocks with positive skew. Three sample clocks with positive skew.	0x0	R/W
0x0123	SYSREF Control 4	7	Reserve		Reserved.	0x0	Read
		[6:0]	SYSREF ± timestamp delay, bits [6:0]		SYSREF ± timestamp delay (in converter sampling clock cycles). 0 :0 Sampling clock cycle delay. 1:1 sampling clock cycle delay. ... 127:127 sampling clock cycle delay.	0x00	R/W
0x0128	SYSREF Status 1	[7:4]	SYSREF ± Maintain State		SYSREF± maintains its state.	0x0	Read
		[3:0]	SYSREF ± Settings		SYSREF ± settings status.	0x0	Read
0x0129	SYSREF	[7:4]	Reserve		Reserved.	0x0	Read

	Status 2	[3:0]	Clock divider phase when capturing SYSREF		<p>SYSREF divider phase. Indicates the phase of the divider when capturing SYSREF.</p> <p>0000 = In phase</p> <p>0001 = SYSREF ± 1/2 clock cycle delay.</p> <p>0010 = SYSREF ± 1 cycle delay compared to the clock .</p> <p>0011 = SYSREF± delayed by 1.5 input clock cycles.</p> <p>0100 = SYSREF ± delayed by 2 input clock cycles.</p> <p>...</p> <p>1111 = SYSREF ± delayed by 7.5 input clock cycles.</p>	0x0	Read
0x012A	SYSREF Status 3	[7:0]	SYSREF counter increments bits [7:0] when SYSREF is captured .		<p>SYSREF counter. The run counter increments whenever a SYSREF± event is captured. Reset via register 0x0120, bit 6.</p> <p>Wraps around 255. These bits are read only if register 0x0120, bits [2:1] are set to disabled.</p>	0x0	Read
0x01FF	Chip sync mode	[7:1]	Reserve		Reserved.	0x0	Read
		0	Synchronous mode	0x0	<p>JESD204B Synchronization Mode. The SYSREF signal resets all internal clock dividers. This mode is used to synchronize multiple chips, as specified in the JESD204B standard. If the phase of any divider must be changed, the JESD204B link will be disconnected.</p>	0x0	R/W
				0x1	<p>Timestamp mode. The SYSREF signal does not reset the internal clock divider. In this mode, the JESD204B link and signal monitor are unaffected by the SYSREF signal. The SYSREF signal timestamps the sample as it passes through the ADC and is used as a control bit in the JESD204B output word.</p>		

- Chip operating mode control register

Address	Name	Bit	Bit Name	Set Up	Description	Reset	Access
0x0200	Chip mode	[7:6]	Reserve		Reserved.	0x0	R/W
		5	Chip Q ignored	0 1	The chip real number (I) is the only option. Choose real numbers (I) and complex numbers (Q). Select only real numbers (I), ignore complex numbers (Q).	0x0	R/W
		4	Reserve		Reserved.	0x0	read
		[3:0]	Chip application models	0000 0001 0010 0011	Full bandwidth mode (default). One DDC mode (DDC0 only). Two DDC modes (DDC0 and DDC1 only). Four DDC modes (DDC0, DDC1, DDC2 and DDC3).	0x0	R/W
0x0201	Chip decimation ratio	[7:4]	Reserve		Reserved.	0x0	read
		[3:0]	Chip extraction ratio	0000 0001 1000 0010 0101 1001 0011 0110 1010 0111 0100 1101 1011 1110 1111 1100	Chip extraction ratio. Full sampling rate (1x sampling, DDCs bypass). 2x draw 3x draw 4x draw 5x draw 6x draw 8x draw 10x draw 12x draw 15x draw 16x draw 20x draw 24x draw 30x draw 40x draw 48x extraction	0x0	R/W

• Fast detection box signal detection control register

Address	Name	Bit	Bit Name	Set Up	Description	Reset	Access
0x0245	Fast detect control (local)	[7:4]	Reserve		Reserved.	0x0	Read
		3	Force FD_A/FD_B pins	0 1	Quickly check the normal operation of the pins. Force a value on the fast detection pin (see bit 2).	0x0	R/W
		2	Forced values for FD_A/FD_B pins		When forced output is applied, the fast detection output pin of this channel is set to this value.	0x0	R/W
		1	Reserve		Reserved.	0x0	Read
		0	Enable fast detection output	0 1	Disable rapid detection. Enable rapid detection.	0x0	R/W
0x0247	Fast detection up LSB (local)	[7:0]	Quickly detect the upper limit of the threshold		Fast detection of the upper threshold LSBs. Compared to fine ADC amplitude, this register contains 8 LSBs with a programmable 13-bit upper threshold.	0x0	R/W
0x0248	Fast detection up MSB (local)	[7:5]	Reserve		Reserved.	0x0	Read
		[4:0]	Quickly detect the upper limit of the threshold		Fast detection of the upper threshold LSBs. Compared to fine ADC amplitude, this register contains 8 LSBs with a programmable 13-bit upper threshold.	0x0	R/W
0x0249	Fast detection low LSB (local)	[7:0]	Quick detection threshold lower limit		Fast detection of threshold lower limit LSBs. Compared to fine ADC amplitude, this register contains 8 LSBs with a programmable 13-bit threshold lower limit.	0x0	R/W
0x024A	Fast detection of low MSB (local)	[7:5]	Reserve		Reserved.	0x0	Read
		[4:0]	Quick detection threshold lower limit		Fast detection of low-threshold LSBs. Compared to fine-tuned ADC amplitude, this register contains 8 LSBs with programmable 13-bit lower threshold.	0x0	R/W
0x024B	Fast detect dwell LSB (local)	[7:0]	Quickly detect dwell time		Quickly detect the LSBs of the dwell time counter target. This is the load value of the 16-bit counter used to determine how long the ADC data must remain below the lower threshold before the FD_x pin is reset to 0.	0x0	R/W
0x024C	Fast detect dwell MSB (local)	[7:0]	Quickly detect dwell time		Quickly detect the LSBs of the dwell time counter target. This is the load value of the 16-bit counter used to determine how long the ADC data must remain below the lower threshold before the FD_x pin is reset to 0.	0x0	R/W
0x026F	Signal monitor sync control	[7:2]	Reserve		Reserved.	0x0	Read
		1	Next synchronization mode of the signal monitor	0 1	The next synchronization mode for the signal monitor. Persistent mode. Next synchronization mode. Only the next valid edge of the SYSREF± pin is used for the synchronization signal monitor block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF is captured, register 0x026F, bit 0, is cleared. The SYSREF± pin must be an integer multiple of the signal monitor cycle for this function to work correctly in continuous mode.	0x0	R/W
		0	Signal monitor synchronization mode	0 1	Enable signal monitor synchronization mode. Disable synchronization. If register 0x026F has bit 1=1, then only the next valid	0x0	R/W

					edge of the SYSREF± pin is used for the synchronization signal monitor block. Subsequent edges of the SYSREF± pin are ignored. This bit is cleared when the next SYSREF signal is received. The SYSREF± input pin must be enabled to synchronize the signal monitor block.		
0x0270	Signal monitor control (local)	[7:0]	Reserve		Reserved.	0x0	Read
		1	Peak detector	0 1	Disable peak detector. Enable peak detector.	0x0	R/W
		0	Reserve		Reserved.	0x0	Read
0x0271	Signal Monitor Period 0 (local)	[7:0]	Signal monitor cycle [7:0]		Bits [7:0] of the 24-bit value set the number of output clock cycles on which the signal monitor performs its operation. Only even values are supported.	0x0	R/W
0x0272	Signal Monitor Period 1 (local)	[7:0]	Signal monitor cycle [15:8]		The 24-bit value [15:8] sets the number of output clock cycles on which the signal monitor performs its operation. Only even values are supported.	0x0	R/W
0x0273	Signal Monitor Period 2 (local)	[7:0]	Signal monitor cycle [23:16]		Bits [23:16] of the 24-bit value set the number of output clock cycles on which the signal monitor performs its operation. Only even values are supported.	0x0	Read
0x0274	Signal monitor status control (local)	[7:5]	Reserve		Reserved.	0x0	Read
		4	Results Update	1	Update the signal monitor status register, from register 0x0275 to register 0x0278. Self-clear.	0x0	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	Result selection	001	The peak detector is placed on the status readback signal.	0x0	R/W
0x0275	Signal Monitor Status 0 (local)	[7:0]	Signal monitor result [7:0]		Signal monitor status result. This 20-bit value contains the status result calculated by the signal monitor block.	0x0	Read
0x0276	Signal Monitor Status 1 (local)	[7:0]	Signal monitor results [15:8]		Signal monitor status results.	0x0	Read
0x0277	Signal Monitor Status 2 (local)	[7:4]	Reserve		Reserved.	0x0	Read
		[3:0]	Signal monitor results [19:16]		Signal monitor status results.	0x0	Read
0x0278	Signal monitor status frame counter (local)	[7:0]	Period calculation result [7:0]		The signal monitor's frame counter status bit. The frame counter increments each time the period counter expires.	0x0	Read
0x0279	Signal monitor serial frame counter (local)	[7:2]	Reserve		Reserved.	0x0	Read
		[1:0]	Enable signal monitor output via JESD204B	00 01	Disabled. Enable.	0x0	R/W
0x027A	SPORT over JESD204B input selection (local)	[7:6]	Reserve		Reserved.	0x0	Read
		1	Select output via JESD204B input.	0 1	The signal monitor selects the serial framer input. When each individual bit is 1, the corresponding signal statistics are transmitted within the frame. Disabled. Peak detector data is inserted into the serial frame.	0x1	R/W
		0	Reserve		Reserved.	0x0	Read

• **DDC function register (see the Digital Down Inverter (DDC) section)**

Address	Name	Bit	Bit Name	Set Up	Description	Reset	Access
0x0300	DDC SYNC control	7	DDC FTW/POW/MAW update mode	0 1	Select the DDC FTW/POW/MAW/MBW update mode. Real-time/continuous updates. FTW/POW/MAW/MBW values are updated immediately. When setting the chip's transmission bit (register 0x000F, bit 0), the FTW/POW/MAW/MBW values are updated synchronously.	0x0	R/W
		[6:5]	Reserve		Reserved.	0x0	Read
		4	DDC NCO Soft Reset	0 1	This bit can be used to synchronize all NCOs within the DDC block. Normal operation. DDC remains reset.	0x0	R/W
		[3:2]	Reserve		Reserved.	0x0	Read
		1	DDC next synchronization	0 1	Continuous mode. The SYSREF frequency must be an integer multiple of the NCO frequency for this function to work correctly in continuous mode. Only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF signal is found, the DDC synchronization mode bit (register 0x0300, bit 0) is cleared.	0x0	R/W
		0	DDC Synchronization Mode		The SYSREF± input pin must be enabled to synchronize DDCs. Disable synchronization. Enable synchronization. If register 0x0300 has bit 1=1, only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Ignore subsequent edges of the SYSREF± pin. Clear this bit when the next SYSREF signal is received.	0x0	R/W
0x0310	DDC0 control	7	DDC0 Mixer Selection	0 1	Real number mixer (I and Q inputs must come from the same real number channel). Complex mixer (I and Q must come from independent, real and imaginary quadrature ADC receive channels; analog demodulator).	0x0	R/W
		6	DDC0 gain selection	0 1	The gain can be used to compensate for the 6dB loss associated with downmixing the input signal to baseband and filtering out its negative components. 0dB gain. 6dB gain (multiplied by 2)	0x0	R/W
		[5:4]	DDC0 Intermediate Frequency (IF) Mode	00 01 10 11	Variable mid-frequency mode. 0Hz Intermediate Frequency Mode. fs Hz intermediate frequency mode. Test mode.	0x0	R/W
		3	DDC0 Complex to Real Number Conversion Enabled	0 1	Complex (I and Q) outputs contain valid data. Outputs only real numbers (I). Complex-to-real conversion is enabled. Uses an additional fs mix to convert to real numbers.	0x0	R/W
		[2:0]	DDC0 extraction rate	000	DDC0 filter selection. HB1+HB2 filter selection: 2x decimation (enable complex to real), or 4x decimation (disable complex to real).	0x0	R/W

			selection	001	HB1+HB2+HB3 filter selection: 4x decimation (enable complex to real), or 8x decimation (disable complex to real).		
				010	HB1+HB2+HB3+HB4 filter selection: 8x decimation (enable complex to real), or 16x decimation (disable complex to real).		
				011	Filter selection: 1x decimation (enable complex to real conversion), or 2x decimation (disable complex to real conversion).		
				100	HB1+TB2 filter selection: 3x decimation (enable complex to real), or 6x decimation (disable complex to real).		
				101	HB1+HB2+TB2 filter selection: 6x decimation (enable complex to real), or 12x decimation (disable complex to real).		
				110	HB1+HB2+HB3+TB2 filter selection: 12x decimation (enable complex to real), or 24x decimation (disable complex to real).		
				111	The extraction is determined by register 0x0311, bits [7:4].		
0x0311	DDCO input select	[7:4]		0000	It is only valid when register 0x0310, bits [2:0] = 3'b111. TB2+HB4+HB3+HB2+HB1 filter selection: 48x decimation (complex to real number disabled), or 24x decimation (complex to real number enabled).	0x0	R/W
				0010	FB2+HB1 filter selection: 10x decimation (complex to real number disabled), or 5x decimation (complex to real number enabled).		
				0011	FB2+HB2+HB1 filter selection: 20x decimation (complex to real number disabled), or 10x decimation (complex to real number enabled).		
				0100	FB2+HB3+HB2+HB1 filter selection: 40x decimation (complex to real number disabled), or 20x decimation (complex to real number enabled).		
				0111	TB1 filter selection: 3x decimation (1.5x decimation is not supported).		
	1000	FB2+TB1 filter selection: 15x decimation (7.5x decimation is not supported).					
	1001	HB2+FB2+TB1 filter selection: 30x decimation (15x decimation is not supported).					
		3	Reserve		Reserved.	0x0	Read
		2	DDCO Q Input Selection	0	Channel A.	0x0	R/W
				1	Channel B.		
		1	Reserve		Reserved.	0x0	Read
		0	DDCO 1 Input Selection	0	Channel A.	0x0	R/W
				1	Channel B.		
0x0314	DDCO NCO control	[7:4]	DDCO NCO Channel Selection Mode	0000	For edge control, the internal counter feeds after register 0x0314, reaching the value of bit [3:0].	0x0	R/W
				0001	Use register 0x0314, bits [3:0]. GPIO_B0, GPIO_A0.		
				1000	The internal counter increments on the rising edge of the GPIO_A0 pin.		
				1010	The internal counter increments on the rising edge of the GPIO_B0 pin.		
		[3:0]	DDCO NCO register mapping channel selection	0000	NCO channel selection register mapping control.	0x0	R/W
				0001	Select NCO channel 0.		
				0010	Select NCO channel 1.		
				0011	Select NCO channel 2.		
				0100	Select NCO channel 3.		
				0101	Select NCO channel 4.		
				0110	Select NCO channel 5.		
				0111	Select NCO channel 6.		

				1000	Select NCO channel 8.		
				1001	Select NCO channel 9.		
				1010	Select NCO channel 10.		
				1011	Select NCO channel 11.		
				1100	Select NCO channel 12.		
				1101	Select NCO channel 13.		
				1110	Select NCO channel 14.		
				1111	Select NCO channel 15.		
0x0315	DDC0 phase control	[7:4]	Reserve		Reserved.	0x0	Read
		[3:0]	DDC0 Phase Update Index		Index the NCO channels whose phase and offset have been updated. The update method is based on the DDC phase update mode, which can be continuous or require chip transfer. Update NCO channel 0. Update NCO channel 1. Update NCO channel 2. Update NCO channel 3.	0x0	R/W
0x0316	DDC0 Phase Increment 0	[7:0]	DDC0 phase increment [7:0]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0317	DDC0 Phase Increment 1	[7:0]	DDC0 phase increment [15:8]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0318	DDC0 Phase Increment 2	[7:0]	DDC0 phase increment [23:16]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0319	DDC0 Phase Increment 3	[7:0]	DDC0 phase increment [31:24]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x031A	DDC0 Phase Increment 4	[7:0]	DDC0 phase increment [39:32]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x031B	DDC0 Phase Increment 5	[7:0]	DDC0 phase increment [47:40]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x031D	DDC0 Phase Offset 0	[7:0]	DDC0 phase offset [7:0]		Two POWs that supplement NCO.	0x0	R/W
0x031E	DDC0 Phase Offset 1	[7:0]	DDC0 phase offset [15:8]		Two POWs that supplement NCO.	0x0	R/W
0x031F	DDC0 Phase Offset 2	[7:0]	DDC0 phase offset [23:16]		Two POWs that supplement NCO.	0x0	R/W
0x0320	DDC0	[7:0]	DDC0		Two POWs that supplement NCO.	0x0	R/W

	Phase Offset 3		phase offset [31:24]								
0x0321	DDC0 Phase Offset 4	[7:0]	DDC0 phase shift [39:32]		Two POWs that supplement NCO.	0x0	R/W				
0x0322	DDC0 Phase Offset 5	[7:0]	DDC0 phase offset [47:40]		Two POWs that supplement NCO.	0x0	R/W				
0x0327	DDC0 test enable	[7:3]	Reserve		Reserved.	0x0	Read				
		2	DDC0 Q output test mode enabled		Q samples always use test mode B block. Use channel-related register 0x0550, bits [3:0], to select the test mode. Test mode is disabled. Test mode is enabled.	0x0	R/W				
		1	Reserve		Reserved.	0x0	Read				
		0	DDC0 1 Output Test Mode Enabled		Sample I always uses test mode A block. Use channel-related register 0x0550, bits [3:0], to select the test mode. Test mode is disabled. Test mode is enabled.	0x0	R/W				
0x0330	DDC1 control	7	DDC1 Mixer Selection	0	Real number mixer (I and Q inputs must come from the same real number channel).	0x0	R/W				
				1	Complex mixer (I and Q must come from independent, real and imaginary quadrature ADC receive channels; analog demodulator).						
		6	DDC1 gain selection	0	0	0	0dB gain.	0x0	R/W		
						1	6dB gain (multiplied by 2)				
				[5:4]	DDC1 intermediate frequency mode	00	Variable intermediate frequency mode.			0x0	R/W
						01	0Hz intermediate frequency mode.				
10	f _s intermediate frequency mode.	10	f _s intermediate frequency mode.	0x0	R/W						
		11	Test mode.								
3	DDC1 Complex to Real Number Conversion Enabled		Complex (I and Q) outputs contain valid data. Outputs only real numbers (I). Complex-to-real conversion is enabled. Uses an additional f _s mix to convert to real numbers.	0x0	R/W						
[2:0]	DDC1 extraction rate selection		Decimation filter selection. 000 HB1+HB2 filter selection: 2x decimation (complex to real number enabled), or 4x decimation (complex to real number disabled). 001 HB1+HB2+HB3 filter selection: 4x decimation (complex to real number enabled), or 8x decimation (complex to real number disabled). 010 HB1+HB2+HB3+HB4 filter selection: 8x decimation (complex to real number enabled), or 16x decimation (complex to real number disabled). 011 HB1 filter selection: 1x decimation (complex to real number enabled), or 2x decimation (complex to real number disabled). 100 HB1+TB2 filter selection: 3x decimation (complex to real number enabled), or 6x decimation (complex to real number disabled).	0x0	R/W						

				101	HB1+HB2+TB2 filter selection: 6x decimation (complex to real number enabled), or 24x decimation (complex to real number disabled).								
				110	HB1+HB2+HB3+TB2 filter selection: 12x decimation (complex to real number enabled), or 24x decimation (complex to real number disabled).								
				111	Extraction determined by register 0x0331, bits [7:4].								
0x0331	DDC1 input select	[7:4]	DDC1 extraction rate selection	00	It is only valid when register 0x0310, bits [2:0] = 3'b111. TB2+HB4+HB3+HB2+HB1 filter selection: 48x decimation (complex to real number disabled), or 24x decimation (complex to real number enabled).	0x0	R/W						
				0010	FB2+HB1 filter selection: 10x decimation (complex to real number disabled), or 5x decimation (complex to real number enabled).								
				0011	FB2+HB2+HB1 filter selection: 20x decimation (complex to real number disabled), or 10x decimation (complex to real number enabled).								
				0100	FB2+HB3+HB2+HB1 filter selection: 40x decimation (complex to real number disabled), or 20x decimation (complex to real number enabled).								
				0111	TB1 filter selection: 3x decimation (1.5x decimation is not supported).								
				1000	FB2+TB1 filter selection: 15x decimation (7.5x decimation is not supported).								
				1001	HB2+FB2+TB1 filter selection: 30x decimation (15x decimation is not supported).								
		3	Reserve		Reserved.	0x0	Read						
		2	DDC1 Q Input Selection	0	Channel A.	0x1	R/W						
				1	Channel B.								
		1	Reserve		Reserved.	0x0	Read						
		0	DDC1 I Input Selection	0	Channel A.	0x1	R/W						
				1	Channel B.								
0x0334	DDC1 NCO control	[7:4]	DDC1 NCO Channel Selection Mode	0000	For edge control, the internal counter feeds when the value of bits [3:0] in register 0x0334 is reached.	0x0	R/W						
				0001	Use register 0x0334, bits [3:0].								
				0010	PIO_BO, GPIO_A0.								
				0011	GPIO_B1, GPIO_A1.								
				0100	GPIO_A1, GPIO_A0.								
				0101	GPIO_B1, GPIO_B0.								
				0110	GPIO_B1,GPIO_A1,GPIO_B0,GPIO_A0.								
				0111	GPIO_B1,GPIO_B0,GPIO_A1,GPIO_A0.								
				1000	The internal counter increments on the rising edge of the GPIO_A0 pin.								
				1001	The internal counter increments on the rising edge of the GPIO_A1 pin.								
				1010	The internal counter increments on the rising edge of the GPIO_B0 pin.								
				1011	The internal counter increments on the rising edge of the GPIO_B1 pin.								
								[3:0]	DDC1 NCO Register Mapping Channel Selection	0000	NCO channel selection register mapping control.	0x0	R/W
										0001	Select NCO channel 0.		
				0010	Select NCO channel 1.								
				0011	Select NCO channel 2.								
				0100	Select NCO channel 3.								
				0101	Select NCO channel 4.								
				0110	Select NCO channel 5.								
				0111	Select NCO channel 6.								
				1000	Select NCO channel 7.								

				1000	Select NCO channel 8.		
				1001	Select NCO channel 9.		
				1010	Select NCO channel 10.		
				1011	Select NCO channel 11.		
				1100	Select NCO channel 12.		
				1101	Select NCO channel 13.		
				1110	Select NCO channel 14.		
				1111	Select NCO channel 15.		
0x0335	DDC1 phase control	[7:4]	Reserve		Reserved.	0x0	Read
		[3:0]	DDC1 Phase Update Index	0000 0001 0010 0011	Index the NCO channels whose phase and offset have been updated. The update method is based on the DDC phase update mode, which can be continuous or require chip transfer. Update NCO channel 0. Update NCO channel 1. Update NCO channel 2. Update NCO channel 3.	0x0	R/W
0x0336	DDC1 Phase Increment 0	[7:0]	DDC1 phase increment [7:0]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0337	DDC1 Phase Increment 1	[7:0]	DDC1 phase increment [15:8]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0338	DDC1 Phase Increment 2	[7:0]	DDC1 phase increment [23:16]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0339	DDC1 Phase Increment 3	[7:0]	DDC1 phase increment [31:24]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x033A	DDC1 Phase Increment 4	[7:0]	DDC1 phase increment [39:32]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x033B	DDC1 Phase Increment 5	[7:0]	DDC1 phase increment [47:40]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x033D	DDC1 Phase Offset 0	[7:0]	DDC1 phase offset [7:0]		Two POWs that supplement NCO.	0x0	R/W
0x033E	DDC1 Phase Offset 1	[7:0]	DDC1 phase shift [15:8]		Two POWs that supplement NCO.	0x0	R/W
0x033F	DDC1 Phase Offset 2	[7:0]	DDC1 phase shift [23:16]		Two POWs that supplement NCO.	0x0	R/W
0x0340	DDC1 Phase Offset 3	[7:0]	DDC1 phase shift [31:24]		Two POWs that supplement NCO.	0x0	R/W

0x0341	DDC1 Phase Offset 4	[7:0]	DDC1 phase shift [39:32]		Two POWs that supplement NCO.	0x0	R/W
0x0342	DDC1 Phase Offset 5	[7:0]	DDC1 phase shift [47:40]		Two POWs that supplement NCO.	0x0	R/W
0x0347	DDC1 test enable	[7:3]	Reserve		Reserved.	0x0	Read
		2	DDC1 Q output test mode enabled	0 1	Q samples always use test mode block B. The test mode is selected using the channel-dependent register 0x0550, bits [3:0]. Test mode is disabled. Test mode is enabled.	0x0	R/W
		1	Reserve		Reserved.	0x0	Read
		0	DDC1 I Output Test Mode Enabled	0 1	Sample I always uses test mode A block. The test mode is selected using the channel-dependent register 0x0550, bits [3:0]. Test mode is disabled. Test mode is enabled.	0x0	R/W
0x0350	DDC2 control	7	DDC2 Mixer Selection	0	Real number mixer (I and Q inputs must come from the same real number channel).	0x0	R/W
				1	Complex mixer (I and Q must come from independent, real and imaginary quadrature ADC receive channels; analog demodulator).		
		6	DDC2 Gain Selection	0	The gain can be used to compensate for the 6dB loss associated with downmixing the input signal to baseband and filtering out its negative components. dB gain.	0x0	R/W
				1	dB gain (multiplied by 2).		
		[5:4]	DDC2 intermediate frequency mode	00 01 10 11	Variable mid-frequency mode. 0Hz intermediate frequency mode. f_s Hz intermediate frequency mode. Test mode.	0x0	R/W
		3	DDC2 Complex to Real Number Conversion Enabled	0	Complex (I and Q) outputs contain valid data.	0x0	R/W
1	Outputs only real numbers (I). So complex it's practically enabled. Uses an additional f_s mix to convert to real numbers.						
[2:0]	DDC2 extraction rate selection	000 001 010 011 100 101 110	Decimation filter selection. HB1+HB2 filter selection: 2x decimation (complex to real number enabled), or 4x decimation (complex to real number disabled). HB1+HB2+HB3 filter selection: 4x decimation (complex to real number enabled), or 8x decimation (complex to real number disabled). HB1+HB2+HB3+HB4 filter selection: 8x decimation (complex to real number enabled), or 16x decimation (complex to real number disabled). HB1 filter selection: 1x decimation (complex to real number enabled), or 2x decimation (complex to real number disabled). HB1+TB2 filter selection: 3x decimation (complex to real number enabled), or 6x decimation (complex to real number disabled). HB1+HB2+TB2 filter selection: 6x decimation (complex to real number enabled), or 12x decimation (complex to real number disabled). HB1+HB2+HB3+TB2 filter selection: 12x decimation (complex to real number enabled), or 24x decimation (complex to real number disabled).	0x0	R/W		

				111	disabled). Extraction determined by register 0x0351, bits [7:4].				
0x0351	DDC2 input select	[7:4]	DDC2 extraction rate selection	000	It is only valid when register 0x0310, bits [2:0] = 3'b111. TB2+HB4+HB3+HB2+HB1 filter selection: 48x decimation (complex to real number disabled), or 24x decimation (complex to real number enabled).	0x0	R/W		
				0010	FB2+HB1 filter selection: 10x decimation (complex to real number disabled), or 5x decimation (complex to real number enabled).				
				011	FB2+HB2+HB1 filter selection: 20x decimation (complex to real number disabled), or 10x decimation (complex to real number enabled).				
				100	FB2+HB3+HB2+HB1 filter selection: 40x decimation (complex to real number disabled), or 20x decimation (complex to real number enabled).				
	3	Reserve			Reserved.	0x0	Read		
	2	DDC2 Q Input Selection		0	Channel A.	0x0	R/W		
				1	Channel B.				
	1	Reserve			Reserved.	0x0	Read		
	0	DDC2 I Input Selection		0	Channel A.	0x0	R/W		
				1	Channel B				
0x0354	DDC2 NCO control	[7:4]	DDC2 NCO Channel Select mode	0000	For edge control, the internal counter feeds when the value of bits [3:0] in register 0x0354 is reached.	0x0	R/W		
				0001	Use register 0x0354, bits [3:0].				
				0010	PIO_BO, GPIO_A0.				
				0011	GPIO_B1, GPIO_A1.				
				0100	GPIO_A1, GPIO_A0.				
				0101	GPIO_B1, GPIO_B0.				
				0110	GPIO_B1,GPIO_A1,GPIO_B0,GPIO_A0.				
				0111	GPIO_B1,GPIO_B0,GPIO_A1,GPIO_A0.				
				1000	The internal counter increments on the rising edge of the GPIO_A0 pin.				
				1001	The internal counter increments on the rising edge of the GPIO_A1 pin.				
				1010	The internal counter increments on the rising edge of the GPIO_B0 pin.				
				1011	The internal counter increments on the rising edge of the GPIO_B1 pin.				
			[3:0]	DDC2 NCO Register Mapping Channel Selection			NCO channel selection register mapping control.	0x0	R/W
						0000	Select NCO channel 0.		
						0001	Select NCO channel 1.		
						0010	Select NCO channel 2.		
				0011	Select NCO channel 3.				
				0100	Select NCO channel 4.				
				0101	Select NCO channel 5.				
				0110	Select NCO channel 6.				
				0111	Select NCO channel 7.				
				1000	Select NCO channel 8.				
				1001	Select NCO channel 9.				
				1010	Select NCO channel 10.				
				1011	Select NCO channel 11.				
				1100	Select NCO channel 12.				
				1101	Select NCO channel 13.				
				1110	Select NCO channel 14.				
				1111	Select NCO channel 15.				
0x0355	DDC2	[7:4]	Reserve		Reserved.	0x0	Read		

	phase control	[3:0]	DDC2 Phase Update Index	0000 0001 0010 0011	Index the NCO channel whose phase and offset have been updated. The update method is based on the DDC phase update mode and can be continuous or require chip transfer. Update NCO channel 0. Update NCO channel 1. Update NCO channel 2. Update NCO channel 3.	0x0	R/W
0x0356	DDC2 Phase Increment 0	[7:0]	DDC2 phase increment [7:0].		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0357	DDC2 Phase Increment 1	[7:0]	DDC2 phase increment [15:8]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0358	DDC2 Phase Increment 2	[7:0]	DDC2 phase increment [23:16]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0359	DDC2 Phase Increment 3	[7:0]	DDC2 phase increment [31:24]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x035A	DDC2 Phase Increment 4	[7:0]	DDC2 phase increment [39:32]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x035B	DDC2 Phase Increment 5	[7:0]	DDC2 phase increment [47:40]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x035D	DDC2 Phase Offset 0	[7:0]	DDC2 phase offset [7:0]		Two POWs that supplement NCO.	0x0	R/W
0x035E	DDC2 Phase Offset 1	[7:0]	DDC2 phase shift [15:8]		Two POWs that supplement NCO.	0x0	R/W
0x035F	DDC2 Phase Offset 2	[7:0]	DDC2 phase shift [23:16]		Two POWs that supplement NCO.	0x0	R/W
0x0360	DDC2 Phase Offset 3	[7:0]	DDC2 phase shift [31:24]		Two POWs that supplement NCO.	0x0	R/W
0x0361	DDC2 Phase Offset 4	[7:0]	DDC2 phase shift [39:32]		Two POWs that supplement NCO.	0x0	R/W
0x0362	DDC2 Phase Offset 5	[7:0]	DDC2 phase shift [47:40]		Two POWs that supplement NCO.	0x0	R/W
0x0367	DDC2 test enable	[7:3]	Reserve		Reserved.	0x0	Read
		2	DDC2 Q output test		Q samples always use test mode B block. The test mode is selected using the channel-dependent register 0x0550, bits [3:0].	0x0	R/W

			mode enabled	0 1	Test mode disabled Test mode enabled		
		1	Reserve		Reserved.	0x0	Read
		0	DDC2 I Output Test Mode Enabled	0 1	Sample I always uses test mode A block. The test mode is selected using the channel-dependent register 0x0550, bits [3:0]. Test mode disabled Test mode is enabled.	0x0	R/W
0x0370	DDC3 control	7	DDC3 Mixer Selection	0 1	Real number mixer (I and Q inputs must come from the same real channel). Complex mixer (I and Q must come from independent, real and imaginary quadrature ADC receive channels; analog demodulator).	0x0	R/W
		6	DDC3 Gain Selection	0 1	The gain can be used to compensate for the 6dB loss associated with downmixing the input signal to baseband and filtering out its negative components. 0dB gain. 6dB gain (multiplied by 2).	0x0	R/W
		[5:4]	DDC3 Intermediate Frequency Mode	00 01 10 11	Variable mid-frequency mode. 0Hz intermediate frequency mode. f_s Hz intermediate frequency mode. Test mode.	0x0	R/W
		3	DDC3 Complex to Real Number Conversion Enabled	0 1	Complex (I and Q) outputs contain valid data. Outputs only real numbers (I). So complex it's practically enabled. Uses an additional f_s mix to convert to real numbers.	0x0	R/W
		[2:0]	DDC3 extraction rate selection	000 001 010 011 100 101 110 111	Decimation filter selection. HB1+HB2 filter selection: 2x decimation (complex to real number enabled), or 4x decimation (complex to real number disabled). HB1+HB2+HB3 filter selection: 4x decimation (complex to real number enabled), or 8x decimation (complex to real number disabled). HB1+HB2+HB3+HB4 filter selection: 8x decimation (complex to real number enabled), or 16x decimation (complex to real number disabled). HB1 filter selection: 1x decimation (complex to real number enabled), or 2x decimation (complex to real number disabled). HB1+TB2 filter selection: 3x decimation (complex to real number enabled), or 6x decimation (complex to real number disabled). HB1+HB2+TB2 filter selection: 6x decimation (complex to real number enabled), or 12x decimation (complex to real number disabled). HB1+HB2+HB3+TB2 filter selection: 12x decimation (complex to real number enabled), or 24x decimation (complex to real number disabled). Extraction determined by register 0x0351, bits [7:4].	0x0	R/W
0x0371	DDC3 input select	[7:4]	DDC3 extraction rate selection	000 010 011	It is only valid when register 0x0310, bits [2:0] = 3'b111. TB2+HB4+HB3+HB2+HB1 filter selection: 48x decimation (complex to real number disabled), or 24x decimation (complex to real number enabled). FB2+HB1 filter selection: 10x decimation (complex to real number disabled), or 5x decimation (complex to real number enabled). FB2+HB2+HB1 filter selection: 20x decimation (complex to real number	0x0	R/W

				100	disabled), or 10x decimation (complex to real number enabled). FB2+HB3+HB2+HB1 filter selection: 40x decimation (complex to real number disabled), or 20x decimation (complex to real number enabled).		
		3	Reserve		Reserved.	0x0	Read
		2	DDC3 Q Input Selection	0 1	Channel A. Channel B.	0x0	R/W
		1	Reserve		Reserved.	0x0	Read
		0	DDC3 Q Input Selection	0 1	Channel A. Channel B.	0x0	R/W
0x0374	DDC3 NCO control	[7:4]	DDC3 NCO Channel Selection Mode	0000 0001 0010 0011 0100 0101 0110 1000 1001 1010 1011	For edge control, the internal counter feeds when the value of bits [3:0] in register 0x0374 is reached. Use register 0x0374, bits [3:0]. PIO_BO, GPIO_AO. GPIO_B1, GPIO_A1. GPIO_A1, GPIO_A0. GPIO_B1, GPIO_B0. GPIO_B1,GPIO_A1,GPIO_B0,GPIO_A0. GPIO_B1,GPIO_B0,GPIO_A1,GPIO_A0. The internal counter increments on the rising edge of the GPIO_A0 pin. The internal counter increments on the rising edge of the GPIO_A1 pin. The internal counter increments on the rising edge of the GPIO_B0 pin. The internal counter increments on the rising edge of the GPIO_B1 pin.	0x0	R/W
		[3:0]	DDC3 NCO Register Mapping Channel Selection	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	NCO channel selection register mapping control. Select NCO channel 0. Select NCO channel 1. Select NCO channel 2. Select NCO channel 3. Select NCO channel 4. Select NCO channel 5. Select NCO channel 6. Select NCO channel 7. Select NCO channel 8. Select NCO channel 9. Select NCO channel 10. Select NCO channel 11. Select NCO channel 12. Select NCO channel 13. Select NCO channel 14. Select NCO channel 15.	0x0	R/W
0x0375	DDC3 phase control	[7:4]	Reserve		Reserved.	0x0	Read
		[3:0]	DDC3 Phase Update Index	0000 0001 0010 0011	Index the NCO channel whose phase and offset have been updated. The update method is based on the DDC phase update mode and can be continuous or require chip transfer. Update NCO channel 0. Update NCO channel 1. Update NCO channel 2. Update NCO channel 3.	0x0	R/W
0x0376	DDC3 Phase	[7:0]	DDC3 phase		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W

	Increment 0		increment [7:0]				
0x0377	DDC3 Phase Increment 1	[7:0]	DDC3 phase increment [15:8]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0378	DDC3 Phase Increment 2	[7:0]	DDC3 phase increment [23:16]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x0379	DDC3 Phase Increment 3	[7:0]	DDC3 phase increment [31:24]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x037A	DDC3 Phase Increment 4	[7:0]	DDC3 phase increment [39:32]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x037B	DDC3 Phase Increment 5	[7:0]	DDC3 phase increment [47:40]		FTW. Two complementary phase increment values of NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s) / 2^{48}$.	0x0	R/W
0x037D	DDC3 Phase Offset 0	[7:0]	DDC3 phase offset [7:0]		Two POWs that supplement NCO.	0x0	R/W
0x037E	DDC3 Phase Offset 1	[7:0]	DDC3 phase shift [15:8]		Two POWs that supplement NCO.	0x0	R/W
0x037F	DDC3 Phase Offset 2	[7:0]	DDC3 phase shift [23:16]		Two POWs that supplement NCO.	0x0	R/W
0x0380	DDC3 Phase Offset 3	[7:0]	DDC3 phase shift [31:24]		Two POWs that supplement NCO.	0x0	R/W
0x0381	DDC3 Phase Offset 4	[7:0]	DDC3 phase shift [39:32]		Two POWs that supplement NCO.	0x0	R/W
0x0382	DDC3 Phase Offset 5	[7:0]	DDC3 phase shift [47:40]		Two POWs that supplement NCO.	0x0	R/W
0x0387	DDC3 test enable	[7:3]	Reserve		Reserved.	0x0	Read
		2	DDC3 Q output test mode enabled	0 1	Q samples always use test mode B block. The test mode is selected using the channel-dependent register 0x0550, bits [3:0]. Test mode disabled Test mode is enabled.	0x0	R/W
		1	Reserve		Reserved.	0x0	Read
		0	DDC3 I Output Test Mode Enabled	0 1	Sample I always uses test mode A block. The test mode is selected using the channel-dependent register 0x0550, bits [3:0]. Test mode disabled Test mode is enabled.	0x0	R/W
0x0390	DDC0 Phase Increment	[7:0]	DDC0 phase		Molecular correction term for the phase accumulator MAW.	0x0	R/W

	Frac A0		increment fractal A[7:0]				
0x0391	DDC0 Phase Increment Frac A1	[7:0]	DDC0 phase increment fractal A[15:8]		Molecular correction terms for MAW.	0x0	R/W
0x0392	DDC0 Phase Increment Frac A2	[7:0]	DDC0 phase increment fractal A[23:16]		Molecular correction terms for MAW.	0x0	R/W
0x0393	DDC0 Phase Increment Frac A3	[7:0]	DDC0 phase increment fractal A[31:24]		Molecular correction terms for MAW.	0x0	R/W
0x0394	DDC0 Phase Increment Frac A4	[7:0]	DDC0 phase increment fractal A[39:32]		Molecular correction terms for MAW.	0x0	R/W
0x0395	DDC0 Phase Increment Frac A5	[7:0]	DDC0 phase increment fractal A[47:40]		Molecular correction terms for MAW.	0x0	R/W
0x0398	DDC0 Phase Increment Frac B0	[7:0]	DDC0 phase increment fractal B[7:0]		The denominator correction term of the phase accumulator MBW.	0x0	R/W
0x0399	DDC0 Phase Increment Frac B1	[7:0]	DDC0 phase increment fractal B[15:8]		MBW's denominator correction term.	0x0	R/W
0x039A	DDC0 Phase Increment Fraction B2	[7:0]	DDC0 phase increment fractal B[23:16]		MBW's denominator correction term.	0x0	R/W
0x039B	DDC0 Phase Increment Fraction B3	[7:0]	DDC0 phase increment fractal B[31:24]		MBW's denominator correction term.	0x0	R/W
0x039C	DDC0 Phase Increment Fraction B4	[7:0]	DDC0 phase increment fractal		MBW's denominator correction term.	0x0	R/W

			B[39:32]				
0x039 D	DDC0 Phase Increment Fraction B5	[7:0]	DDC0 phase increment fractal B[47:40]		MBW's denominator correction term.	0x0	R/W
0x03A0	DDC1 Phase Increment Frac A0	[7:0]	DDC1 phase increment fractal A[7:0]		Molecular correction terms for MAW.	0x0	R/W
0x03A1	DDC1 Phase Increment Frac A1	[7:0]	DDC1 phase increment fractal A[15:8]		Molecular correction terms for MAW.	0x0	R/W
0x03A2	DDC1 Phase Increment Fraction A2	[7:0]	DDC1 phase increment fractal A[23:16]		Molecular correction terms for MAW.	0x0	R/W
0x03A3	DDC1 Phase Increment Fraction A3	[7:0]	DDC1 phase increment fractal A[31:24]		Molecular correction terms for MAW.	0x0	R/W
0x03A4	DDC1 Phase Increment Frac A4	[7:0]	DDC1 Phase Increment Fractal A[39:32]		Molecular correction terms for MAW.	0x0	R/W
0x03A5	DDC1 Phase Increment Frac A5	[7:0]	DDC1 Phase Increment Fractal A[47:40]		Molecular correction terms for MAW.	0x0	R/W
0x03A8	DDC1 Phase Increment Fraction B0	[7:0]	DDC1 phase increment fractal B[7:0]		MBW's denominator correction term.	0x0	R/W
0x03A9	DDC1 Phase Increment Fraction B1	[7:0]	DDC1 phase increment fractal B[15:8]		MBW's denominator correction term.	0x0	R/W
0x03AA	DDC1 Phase Increment Fraction B2	[7:0]	DDC1 phase increment fractal B[23:16]		MBW's denominator correction term.	0x0	R/W
0x03A	DDC1 Phase	[7:0]	DDC1		MBW's denominator correction term.	0x0	R/W

B	Increment Fraction B3		phase increment fractal B[31:24]				
0x03AC	DDC1 Phase Increment Fraction B4	[7:0]	DDC1 phase increment fractal B[39:32]		MBW's denominator correction term.	0x0	R/W
0x03AD	DDC1 Phase Increment Fraction B5	[7:0]	DDC1 phase increment fractal B[47:40]		MBW's denominator correction term.	0x0	R/W
0x03B0	DDC2 Phase Increment FracA0	[7:0]	DDC2 phase increment fractal A[7:0]		Molecular correction terms for MAW.	0x0	R/W
0x03B1	DDC2 Phase Increment FracA1	[7:0]	DDC2 phase increment fractal A[15:8]		Molecular correction terms for MAW.	0x0	R/W
0x03B2	DDC2 Phase Increment FracA2	[7:0]	DDC2 phase increment fractal A[23:16]		Molecular correction terms for MAW.	0x0	R/W
0x03B3	DDC2 Phase Increment FracA3	[7:0]	DDC2 phase increment fractal A[31:24]		Molecular correction terms for MAW.	0x0	R/W
0x03B4	DDC2 Phase Increment FracA4	[7:0]	DDC2 phase increment fractal A[39:32]		Molecular correction terms for MAW.	0x0	R/W
0x03B5	DDC2 Phase Increment FracA5	[7:0]	DDC2 phase increment fractal A[47:40]		Molecular correction terms for MAW.	0x0	R/W
0x03B8	DDC2 Phase Increment Frac B0	[7:0]	DDC2 phase increment fractal B[7:0]		MBW's denominator correction term.	0x0	R/W
0x03B9	DDC2 Phase Increment Fraction B1	[7:0]	DDC2 phase increment		MBW's denominator correction term.	0x0	R/W

			fractal B[15:8]				
0x03BA	DDC2 Phase Increment Fraction B2	[7:0]	DDC2 phase increment fractal B[23:16]		MBW's denominator correction term.	0x0	R/W
0x03BB	DDC2 Phase Increment Fraction B3	[7:0]	DDC2 phase increment fractal B[31:24]		MBW's denominator correction term.	0x0	R/W
0x03BC	DDC2 Phase Increment Fraction B4	[7:0]	DDC2 phase increment fractal B[39:32]		MBW's denominator correction term.	0x0	R/W
0x03BD	DDC2 Phase Increment Frac B5	[7:0]	DDC2 phase increment fractal B[47:40]		MBW's denominator correction term.	0x0	R/W
0x03C0	DDC3 Phase Increment Frac A0	[7:0]	DDC3 Phase Increment Fractal A[7:0]		Molecular correction terms for MAW.	0x0	R/W
0x03C1	DDC3 Phase Increment Frac A1	[7:0]	DDC3 Phase Increment Fractal A[15:8]		Molecular correction terms of MAW	0x0	R/W
0x03C2	DDC3 Phase Increment Fraction A2	[7:0]	DDC3 Phase Increment Fractal A[23:16]		Molecular correction terms of MAW	0x0	R/W
0x03C3	DDC3 Phase Increment Fraction A3	[7:0]	DDC3 Phase Increment Fractal A[31:24]		Molecular correction terms of MAW	0x0	R/W
0x03C4	DDC3 Phase Increment Frac A4	[7:0]	DDC3 Phase Increment Fractal A[39:32]		Molecular correction terms of MAW	0x0	R/W
0x03C5	DDC3 Phase Increment Frac A5	[7:0]	DDC3 Phase Increment Fractal A[47:40]		Molecular correction terms of MAW	0x0	R/W

0x03C8	DDC3 Phase Increment Fraction B0	[7:0]	DDC3 Phase Increment Fractal B[7:0]		MBW's denominator correction term.	0x0	R/W
0x03C9	DDC3 Phase Increment Fraction B1	[7:0]	DDC3 Phase Increment Fractal B[15:8]		MBW's denominator correction term.	0x0	R/W
0x03CA	DDC3 Phase Increment Fraction B2	[7:0]	DDC3 Phase Increment Fractal B[23:16]		MBW's denominator correction term.	0x0	R/W
0x03CB	DDC3 Phase Increment Fraction B3	[7:0]	DDC3 Phase Increment Fractal B[31:24]		MBW's denominator correction term.	0x0	R/W
0x03CC	DDC3 Phase Increment Fraction B4	[7:0]	DDC3 Phase Increment Fractal B[39:32]		MBW's denominator correction term.	0x0	R/W
0x03CD	DDC3 Phase Increment Frac B5	[7:0]	DDC3 Phase Increment Fractal B[47:40]		MBW's denominator correction term.	0x0	R/W

• Data output and test mode

Address	Name	Bit	Bit Name	Set Up	Description	Reset	Access		
0x0550	ADC test mode control (local)	7	User mode selection	0	Test mode user mode selection. This bit is only used in register 0x0550 when bits [3:0] = 4'b1000 (user input mode). Otherwise, it is ignored. User mode 1 is found in the User Mode 1 MSB (0x0552) and User Mode 1 LSB (0x0551) registers. User mode 2 is located in the User Mode 2 MSB (0x0554) and User Mode 2 LSB (0x0553) registers, and so on. Continuous / Repeating Mode. Each user pattern (1 , 2 , 3 , and 4) is placed on the output for one clock cycle, then repeated. (Outputs include the following user patterns: 1 , 2 , 3 , 4 , 1 , 2 , 3 , 4 , 1 , 2 , 3 , 4 , etc.)	0x0	R/W		
		1		Single mode. Output each user pattern (1 , 2 , 3 , and 4) followed by all zeros. (Output the following user patterns: 1 , 2 , 3 , 4 , followed by all zeros.)					
		6	Reserve		Reserved.	0x0	Read		
		5	Reset PN long generator	0	The test mode is a long pseudo-random number test generator reset. Long PN junction activated.	1	Long PN junctions are prohibited.	0x0	R/W
		4	Reset PN short generator	0	The test mode is a short pseudo-random number test generator reset. Long PN junction activated.	1	Long PN junctions are prohibited.	0x0	R/W
	[3:0] Test mode selection			0000	Test pattern generator selection. Shut down (normal operation).	0x0	R/W		
			0001	Intermediate level short code.					
			0010	Full scale.					
			0011	Negative full scale.					
			0100	Alternating chessboard.					
			0101	PN sequence (long).					
			0110	PN sequence (short).					
			0111	between 1 and 0 characters.					
			1000	User-mode test mode (used with register 0x0550 , bit 7 , and User-mode 1 , User-mode 2 , User-mode 3 , and User-mode 4 registers).					
			1111	Ramp output.					
0x0551	User Pattern 1 LSB	[7:0]	User Mode 1 [7:0]		User test mode 1 least significant byte.	0x0	R/W		
0x0552	User Pattern 1 MSB	[7:0]	User Mode 1 [15:8]		User test mode 1 least significant byte.	0x0	R/W		
0x0553	User Pattern 2 LSB	[7:0]	User Mode 2 [7:0]		User test mode 2 least significant byte.	0x0	R/W		
0x0554	User Pattern 2 MSB	[7:0]	User Mode 2 [15:8]		User test mode 2 least significant byte.	0x0	R/W		
0x0555	User Pattern 3 LSB	[7:0]	User Mode 3 [7:0]		User test mode 3 least significant byte.	0x0	R/W		
0x0556	User Pattern 3 MSB	[7:0]	User Mode 3 [15:8]		User test mode 3 least significant byte.	0x0	R/W		
0x0557	User Pattern 4	[7:0]	User Mode 4		User test mode 4 least significant byte.	0x0	R/W		

	LSB		[7:0]				
0x0558	User Pattern 4 MSB	[7:0]	User Mode 4 [15:8]		User test mode 4 least significant byte.	0x0	R/W
0x0559	Output Mode Control 1	[7:4]	Converter control bit 1 select	0000 0001 0010 0011 0101	Lower (1'b0). Overrange position. Signal detector bit. Fast Detection (FD) bit. SYSREF.	0x0	R/W
		[3:0]	Converter control bit 0 select	0000 0001 0010 0011 0101	Lower (1'b0). Overrange position. Signal detector bit. Fast Detection (FD) bit. SYSREF.	0x0	R/W
0x055A	Output Mode Control 1	[7:4]	Reserve		Reserved.	0x0	read
		[3:0]	Converter control bit 2 selection	0000 0001 0010 0011 0101	Lower (1'b0). Overrange position. Signal detector bit. Fast Detection (FD) bit. SYSREF .	0x0	R/W
0x0561	Out sample mode	[7:3]	Reserve		Reserved.	0x0	Read
		2	Sample reversal	0 1	ADC sampling data is not reversed. ADC sampling data is inverted.	0x0	R/W
		[1:0]	Data format selection	00 01	Offset binary. Two complements (default).	0x0	R/W
0x0562	Out over-range clear	[7:0]	Data format overrange clearing	0 1	Over-range clear bit (one bit per virtual converter). Writing a 1 to the over-range clear bit will clear the corresponding over-range sticky bit. Overrange position enabled. Excessive amounts are cleared.	0x0	R/W
0x0563	Out over-range status	[7:0]	Data format overrange	0 1	Out-of-range sticky bit status (one bit per virtual converter). Writing a 1 to the out-of-range clear bit will clear the corresponding out-of-range sticky bit. No over-range was detected. Excessive amounts were observed.	0x0	Read
0x0564	Out channel select	[7:1]	Reserve		Reserved.	0x0	Read
		0	Converter channel switching control		Normal channel sorting. Channel switching is enabled.	0x0	R/W
0x056E	PLL control	[7:4]	JESD204B Channel Rate Control	0000 0001 0011 0101	Channel rates range from 6.75 Gbps to 13.5 Gbps . Channel rates range from 3.375 Gbps to 6.75 Gbps . Channel rates range from 13.5 Gbps to 16 Gbps . Channel rates range from 1.6875 Gbps to 3.375 Gbps .	0x0	R/W
		[3:0]	Reserve		Reserved.	0x0	Read
0x056F	PLL status	7	PLL locked state	0 1	Unlocked. locking.	0x0	Read
		[6:4]	Reserve		Reserved.	0x0	Read
		3	PLL lockout lost		Viscous position loss. This indicates that a lock loss occurred at a certain time. It can be cleared by setting register 0x0571 , bit 0 .		

		[2:0]	Reserve		Reserved.		
0x0570	$f_s \times 4$ configuration	[7:0]		0xFE 0xFF	See the $f_s \times 4$ mode section. Enable $f_s \times 4$ mode. L=8 ; M=2 ; F=2 ; S=4 ; N'=16 ; N=16 ; CS = 0; CF = 0; HD = 0. Disable $f_s \times 4$ mode. L, M and F are set by register 0x058B, bits [4:0]; register 0x58E, bits [7:0]; and register 0x058C, bits [7:0], respectively.	0xFF	R/W
0x0571	JESD204B Link Control 1	7	Standby mode	0 1	Standby mode forces all converter samples to be zero. Standby mode forces code group synchronization (/K28.5/characters).	0x0	R/W
		6	End bit (t) PN	0 1	Disabled. Enabled.	0x0	R/W
		5	Long transport layer test	0 1	Disable the JESD204B test sample. Enable JESD204B test samples. Send a long transport layer test sample sequence on all link channels (as described in JESD204B Section 5.1.6.3).	0x0	R/W
		4	Channel synchronization	0 1	Disable FACI usage /K28.7/ . Enable FACI using /K28.3/ and /K28.7/ .	0x1	R/W
		[3:2]	ILAS sequence pattern	00 01 11	Disable the initial channel alignment sequence (JESD204B Section 5.3.3.5). Enable the initial channel alignment sequence (JESD204B Section 5.3.3.5). The initial channel alignment sequence is always in test mode. JESD204B data link layer test mode, in which repeated channel alignment sequences are sent on all channels (as described in JESD204B Section 5.3.3.8.2).	0x1	R/W
		1	FACI	0 1	Enable frame alignment character insertion (JESD204B Section 5.3.3.4). Disable frame alignment character insertion. For debugging purposes only (JESD204B Section 5.3.3.4).	0x0	R/W
		0	Link control	0 1	Enable the JESD204B serial transmission link. The /K28.5/ characters of the transmitted code group synchronization are controlled by the SYNC~ pin. JESD204B serial transmission link power failure (retains reset and clock gating).	0x0	R/W
0x0572	JESD204B Link Control 2	[7:6]	SYNCINB ± pin control	00 10 11	Normal mode. Ignore SYNCINB± (force CGS). Ignore SYNCINB± (Force ILAS/ User Data).	0x0	R/W
		5	SYNCINB ± pin reversal	0 1	The SYNCINB± pin is not reversed. SYNCINB± pin reverse.	0x0	R/W
		4	SYNCINB ± pin type	0 1	LVDS differential pair SYNC~ input. CMOS single-ended SYNC~ input. Use SYNCINB+ .	0x0	R/W
		3	Reserve		Reserved.	0x0	Read
		2	8-bit /10-bit bypass	0 1	8-bit /10-bit enabled. 8-bit /10-bit bypass (most significant bit is 2).	0x0	R/W
		1	8-bit /10-bit inversion	0 1	Normal. Reverse the symbols a, b, c, d, e, f, g, h, i, and j.	0x0	R/W
		0	Reserve		Reserved.	0x0	R/W
0x0573	JESD204B Link Control 3	[7:6]	Checksum mode	00 01 10 11	The checksum is the sum of all 8-bit registers in the link configuration table. The checksum is the sum of all individual link configuration fields (LSB aligned). Disable checksum (set to zero). For testing purposes only. Not used.	0x0	R/W
		[5:4]	Test	0	N' Sample Input.	0x0	R/W

			injection point	1 10	10 -bit data output from 8- bit /10- bit (for PHY testing). 8 -bit data at the input of the scrambler.		
		[3:0]	JESD204B test mode	0000 0001 0010 0011 0100 0101 0110 0111 1000 1110 1111	Normal operation (test mode disabled). Alternating chessboard. between 1 and 0 characters. 31 -bit PN sequence: $x^{31} + x^{28} + 1$. 23 -bit PN sequence: $x^{23} + x^{18} + 1$. 15 -bit PN sequence: $x^{15} + x^{14} + 1$. 9 -bit PN sequence: $x^9 + x^5 + 1$. 7 -bit PN sequence: $x^7 + x^6 + 1$. Ramp output. Continuous / repeated user testing. Single-user testing.	0x0	R/W
0x0574	JESD204 B Link Control 4	[7:4]	ILAS delay	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	After SYNCINB± reset is released, ILAS is transmitted in the first LMFC . After SYNCINB± reset is released, ILAS is transmitted in the second LMFC . After SYNCINB± reset is released, ILAS is transmitted in the third LMFC . After SYNCINB± reset is released, ILAS is transmitted in the fourth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the fifth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the sixth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the seventh LMFC . After SYNCINB± reset is released, ILAS is transmitted in the eighth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the ninth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the tenth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the eleventh LMFC . After SYNCINB± reset is released, ILAS is transmitted in the twelfth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the thirteenth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the fourteenth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the fifteenth LMFC . After SYNCINB± reset is released, ILAS is transmitted in the sixteenth LMFC .	0x0	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	Link layer test mode	000 001 010 011 100 101 110 111	Normal operation (link layer test mode disabled). /D21.5/ . Reserved. Reserved. Modify the PRAT test sequence. JSPAT test sequence. JTSPAT test sequence. Reserved.	0x0	R/W
0x0578	JESD204 B LMFC offset	[7:5]	Reserve		Reserved.	0x0	Read
		[4:0]	LMFC phase offset value		LMFC phase offset value (in frame clocks). See the deterministic delay section.	0x0	R/W
0x0580	JESD204 B DID configuration	[7:0]	JESD204B T×DID value		JESD204B Serial Device Identifier (DID) number.	0x0	R/W

0x0581	JESD204B BID configuration	[7:4]	Reserve		Reserved.	0x0	Read
		[3:0]	JESD204B T×BID value		JESD204B BID number (extended to DID).	0x0	R/W
0x0583	JESD204B LIDO configuration	[7:5]	Reserve		Reserved.	0x0	Read
		[4:0]	Channel 0 LID value		JESD204B serial channel identification (LID) number for channel 0 .	0x0	R/W
0x0584	JESD204B LID1 configuration	[7:5]	Reserve		Reserved.	0x0	Read
		[4:0]	Channel 1 LID value		JESD204B serial LID number for channel 1 .	0x1	R/W
0x0585	JESD204B LID2 configuration	[7:5]	Reserve		Reserved.	0x0	Read
		[4:0]	Channel 2 LID value		JESD204B serial LID number for channel 2 .	0x2	R/W
0x0586	JESD204B LID3 configuration	[7:5]	Reserve		Reserved.	0x0	Read
		[4:0]	Channel 3 LID value		JESD204B serial LID number for channel 3 .	0x3	R/W
0x058B	JESD204B scrambling and number of lanes (L) configuration	7	JESD204B Scrambling (SCR)	0 1	JESD204B scrambler disabled (SCR=0). JESD204B scrambler enabled (SCR=1).	0x1	R/W
		[6:5]	Reserve		Reserved.	0x0	R/W
		[4:0]	JESD204B Channel (L)	0x0 0x1 0x3	One channel per link (L=1). Two channels per link (L=2). 4 channels per link (L=4)	0x7	R/W
0x058C	JESD204B link number of octets per frames (F)	[7:0]	JESD204B F Configuration	0000 0001 0010 0011 0101 0111 1111	8 -bit words per frame in JESD204B (F=0x058C[7:0]+1) . F=1 . F=2 . F=3 . F=4 . F=6 . F=8 . F=16 .	0x0	R/W
0x058D	JESD204B link number of octets per frames (K)	[7:5]	Reserve		Reserved.	0x0	Read
		[4:0]	JESD204B K Configuration		JESD204B frame count per multiframe (K=0x058C[4:0]+1) . Only used when F×K is divisible by 4 .	0x1F	R/W
0x058E	JESD204B link number of converters (M)	[7:0]	JESD204B M Configuration	000 001 011 111	Number of converters per device link in JESD204B (M = JESD204B M configuration) . The link is connected to a virtual converter (M=1). The link connects to two virtual converters (M=2). The link connects to four virtual converters (M=4). The link connects to eight virtual converters (M=8).	0x1	R/W
0x058F	JESD204B	[7:6]	CS) per	000	No control bit (CS=0).	0x0	R/W

	B number of control bits (CS) and ADC resolution (N)		sample	001 010 011	1 control bit (CS=1), only control bit 2 . 2 control bits (CS=2), only control bit 2 and control bit 1 . 3 control bits (CS=3), all control bits (control bit 2 , control bit 1 and control bit 0).		
		5	Reserve		Reserved.	0x0	Read
		[4:0]	ADC converter resolution (N)	00110 00111 01000 01001 01010 01011 01100 01101 01110 01111	N = 7 - bit resolution. N = 8 -bit resolution. N = 9 -bit resolution. N = 10 -bit resolution. N = 11 -bit resolution. N = 12 -bit resolution. N = 13 -bit resolution. N = 14 -bit resolution. N = 15 -bit resolution. N = 16 -bit resolution.	0xF	R/W
0x0590	JESD204 B SCV NP Configuration	[7:5]	Subclass support	000 001	Subclass 0 . Subclass 1 .	0x1	R/W
		[4:0]	ADC bits per sample (N')	00111 01011 01111	N'=8 . N'=12 . N'=16 .	0xF	R/W
0x0591	JESD204 B JV S Configuration	[7:5]	Reserve		Reserved.	0x0	Read
		[4:0]	Samples per converter frame period		Samples for each converter frame period (S=0x0591[4:0]+1) .	0x0	Read
0x0592	JESD204 B HD CF Configuration	7	HD value	0 1	High-density format is disabled. High-density format enabled.	0x0	Read
		[6:5]	Reserve		Reserved.	0x0	Read
		[4:0]	(CF) per link per frame clock cycle		The number of control words per link per frame clock cycle (CF=Register0x0592,Bits[4:0]) .	0x0	Read
0x05A0	JESD204 B Checksum 0 configuration	[7:0]	Checksum 0 SERDOUT 0± check value		The serial checksum value for channel 0. Calculated automatically for each channel. And (all configuration parameters for channel 0) mod 256 .	0xC3	Read
0x05A1	JESD204 B Checksum 1 configuration	[7:0]	Checksum 1 SERDOUT 0± check value		The serial checksum value for channel 1. Calculated automatically for each channel. And (all configuration parameters for channel 1) mod 256 .	0xC4	Read
0x05A2	JESD204 B Checksum 2 configuration	[7:0]	Checksum 2 SERDOUT 0± check value		The serial checksum value for channel 2. Calculated automatically for each channel. And (all configuration parameters for channel 2) mod 256 .	0xC5	Read

0x05A3	JESD204B Checksum 3 configuration	[7:0]	Checksum 3 SERDOUT 0± check value		The serial checksum value for channel 3. Calculated automatically for each channel. And (all configuration parameters for channel 3) mod 256 .	0xC6	Read
0x05B0	JESD204B lane power-down	7	Reserve		Reserved.	0x0	R/W
		6	JESD204B Lane 3 power-down	0 1	Physical channel 3 is forced to shut down. SERDOUT3± is working normally. SERDOUT3± power off.	0x0	R/W
		5	Reserve		Reserved.	0x0	R/W
		4	JESD204B Lane 2 power-down	0 1	Physical channel 2 is forced to shut down. SERDOUT2± is working normally. SERDOUT2± power off.	0x0	R/W
		3	Reserve		Reserved.	0x0	R/W
		2	JESD204B Lane 1 power-down	0 1	Physical channel 1 is forced to shut down. SERDOUT1± is working normally. SERDOUT1± power off.	0x0	R/W
		1	Reserve		Reserved.	0x0	R/W
		0	JESD204B Lane 0 power-down	0 1	Physical channel 0 is forced to shut down. SERDOUT0± is working normally. SERDOUT0± power off.	0x0	R/W
0x05B2	JESD204B Lane Assign 1	7	Reserve		Reserved.	0x0	Read
		[6:4]	Reserve		Reserved.	0x0	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	SERDOUT 0 ± Channel Assignment	000 001 010 011	Physical channel 0 is allocated. Logical channel 0 (default). Logical channel 1 . Logical channel 2 . Logical channel 3 .	0x0	R/W
0x05B3	JESD204B Lane Assign 2	7	Reserve		Reserved.	0x0	Read
		[6:4]	Reserve		Reserved.	0x1	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	SERDOUT 1 ± Channel Assignment	000 001 010 011	Physical channel 1 is allocated. Logical channel 0 . Logical channel 1 (default). Logical channel 2 . Logical channel 3 .	0x1	R/W
0x05B5	JESD204B Lane Assign 3	7	Reserve		Reserved.	0x0	Read
		[6:4]	Reserve		Reserved.	0x2	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	SERDOUT 2± Channel Assignment	000 001 010 011	Physical channel 2 allocation. Logical channel 0 . Logical channel 1 . Logical channel 2 (default). Logical channel 3 .	0x2	R/W
0x05B6	JESD204B Lane Assign 4	7	Reserve		Reserved.	0x0	Read
		[6:4]	Reserve		Reserved.	0x3	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	SERDOUT 3±	000	Physical channel 3 allocation. Logical channel 0 .	0x3	R/W

			Channel Assignment	001 010 011	Logical channel 1 . Logical channel 2 . Logical channel 3 (default).		
0x05BF	SERDO UTx± data invert	7	Reserve		Reserved.	0x0	R/W
		6	Reverse SERDOUT 3± data	0 1	Reverse the SERDOUT3± data. normal. Reverse.	0x0	R/W
		5	Reserve		Reserved.	0x0	R/W
		4	Reverse SERDOUT 2± data	0 1	Reverse the SERDOUT2± data. Normal. Reverse.	0x0	R/W
		3	Reserve		Reserved.	0x0	R/W
		2	Reverse SERDOUT 1± data	0 1	Reverse the SERDOUT1± data. Normal. Reversed.	0x0	R/W
		1	Reserve		Reserved.	0x0	R/W
		0	Reverse SERDOUT 0± data	0 1	Reverse the SERDOUT0± data. Normal. Reversed.	0x0	R/W
0x05C0	JESD204 B Swing Adjust 1	7	Reserve		Reserved.	0x0	Read
		[6:4]	Reserve		Reserved.	reser ve	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	SERDOUT 0± Voltage Swing Adjust- ment	000 001 010	SERDOUT0± output swing level. 1.0×DRVDD1 . 0.850×DRVDD1 . 0.750×DRVDD1 .	0x0	R/W
0x05C1	JESD204 B Swing Adjust 2	7	Reserve		Reserved.	0x0	Read
		[6 : 4]	Reserve		Reserved.	0x0	R/W
		3	Reserve		Reserved.	0x0	Read
		[2 : 0]	SERDOUT 1± Voltage Swing Adjust- ment	000 001 010	SERDOUT1± output swing level. 1.0×DRVDD1 . 0.850×DRVDD1 . 0.750×DRVDD1 .	0x0	R/W
0x05C2	JESD204 B Swing Adjust 3	7	Reserve		Reserved.	0x0	Read
		[6:4]	Reserve		Reserved.	0x0	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	SERDOUT 2± Voltage Swing Adjust- ment	000 001 010	SERDOUT2± output swing level. 1.0×DRVDD1 . 0.850×DRVDD1 . 0.750×DRVDD1 .	0x0	R/W
0x05C3	JESD204 B Swing Adjust 4	7	Reserve		Reserved.	0x0	Read
		[6:4]	Reserve		Reserved.	0x0	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	SERDOUT 3±	000	SERDOUT3± output swing level. 1.0×DRVDD1 .	0x0	R/W

			Voltage Swing Adjustment	001 010	0.850×DRVDD1 . 0.750×DRVDD1 .		
0x05C4	SERDO UT0 de-emphasis select	7	Post-tap activation	0 1	The tap is activated afterward. Disabled. Enabled.	0x0	R/W
		[6:4]	Set the back tap level of SERDOUT 1±	000 001 010 011 100	Set the tap level. 0 dB . 3 dB . 6 dB . 9 dB . 12 dB .	0x0	R/W
		[3:0]	Reserve		Reserved.	0x0	R/W
0x05C6	SERDO UT1 de-emphasis select	7	Post-tap activation	0 1	The tap is activated afterward. Disabled. Enabled.	0x0	R/W
		[6:4]	Set the back tap level of SERDOUT 2±	000 001 010 011 100	Set the tap level. 0 dB . 3 dB . 6 dB . 9 dB . 12 dB .	0x0	R/W
		[3:0]	Reserve		Reserved.	0x0	R/W
		[3:0]	Reserve		Reserved.	0x0	R/W
0x05C8	SERDO UT2 de-emphasis select	7	Post-tap activation	0 1	The tap is activated afterward. Disabled. Enabled.	0x0	R/W
		[6:4]	Set the back tap level of SERDOUT 4±	000 001 010 011 100	Set the tap level. 0 dB . 3 dB . 6 dB . 9 dB . 12 dB .	0x0	R/W
		[3:0]	Reserve		Reserved.	0x0	R/W
0x05CA	SERDO UT3± pre-emphasis select	7	Post-tap activation	0 1	The tap is activated afterward. Disabled. Enabled.	0x0	R/W
		[6:4]	Set the back tap level of SERDOUT 6±	000 001 010 011 100	Set the tap level. 0 dB . 3 dB . 6 dB . 9 dB . 12 dB .	0x0	R/W
		[3:0]	Reserve		Reserved.	0x0	R/W
		[3:0]	Reserve		Reserved.	0x0	R/W
0x1222	JESD204B PLL calibration	[7:0]	JESD204B Phase-Locked Loop Calibration Reset	0x00 0x04	See Table 16.1 The JESD204B phase-locked loop is working normally. Reset the JESD204B phase-locked loop calibration.	0x0	R/W

0x1228	JESD204B PLL start-up control	[7:0]	JESD204B Phase-Locked Loop Calibration Startup Circuit Reset	0x0F 0x4F	See Table 16.1 JESD204B startup circuit is in normal working condition. Reset the JESD204B startup circuit.	0x0	R/W
0x1262	JESD204B PLL LOL bit control	[7:0]	JESD204B Phase-Locked Loop Loss Clearance		See Table 16.1 The system works normally even when the lock is lost. Clear lost locks.	0x0	R/W

• Programmable Filter Lite (PFILT) Control and Coefficient Register

Address	Name	Bit	Bit Name	Set Up	Description	Reset	Access
0x0DF8	Programmable filter control	[7:3]	Reserve		Reserved.	0x0	Write
		[2:0]	Programmable filter mode	000	Disable (filter bypass).		
				001	Single filter (X only). $DOUT_I[n] = DIN_I[n] * X_I[n]$ $DOUT_Q[n] = DIN_Q[n] * X_Q[n]$		
				010	Single filter (X and Y together). $DOUT_I[n] = DIN_I[n] * XY_I[n]$ $DOUT_Q[n] = DIN_Q[n] * XY_Q[n]$		
				100	Cascaded filter (X to Y). $DOUT_I[n]=DIN_I[n]*X_I[n]*Y_I[n]$ $DOUT_Q[n]=DIN_Q[n]*X_Q[n]*Y_Q[n]$ $DOUT_Q[n]=DIN_Q[n]*X_Q[n]*Y_Q[n]$		
				101	Complex filter. $DOUT_I[n]=DIN_I[n]*X_I[n]+DIN_Q[n]*Y_Q[n]$ $DOUT_Q[n]=DIN_Q[n]*X_Q[n]+DIN_I[n]*Y_I[n]$		
				110	Half-complex filter. $DOUT_I[n]=DIN_I[n]$ $DOUT_Q[n]=DIN_Q[n]*XY_Q[n]+DIN_I[n]*XY_I[n]$		
				111	Real number 96-tap filter. $DOUT_I[n] = DIN_I[n] * XY_I[n]$. $DOUT_Q[n] = DIN_Q[n] * XY_Q[n]$		
0x0DF9	PFILT gain			7	Reserve		Reserved.
		[6:4]	PFILT Y gain		Programmable Filter (PFILT) Y Gain 100 = Reserved. 101 = Reserved. 110 = -12 dB loss. 111 = -6dB loss. 000: 0dB gain. 001: +6 dB gain. 010: +12 dB gain. 011: Reserved.	0x0	R/W
		3	Reserve		Reserved.	0x0	Read
		[2:0]	PFILT X gain		Programmable Filter (PFILT) X Gain. 100 = Reserved. 101 = Reserved. 110 = -12 dB loss. 111 = -6dB loss. 000: 0dB gain. 001: +6 dB gain. 010: +12 dB gain. reserv011: Edit.	0x0	R/W
0x0E00 to 0x0E7F	Programmable Filter	[7:0]	Programmable filter X coefficients from 0 to 127		The coefficient is only applied after setting the chip transmission bit (register 0x000F, bit 0).	0x0	R/W
0x0F00 to 0x0F7F	Programmable Filter Y Coefficient x	[7:0]	Programmable filter Y coefficients from 0 to 127		The coefficient is only applied after setting the chip transmission bit (register 0x000F, bit 0).	0x0	R/W

• VREF/Analog Input Control Register

Address	Name	Bit	Bit Name	Set Up	Description	Reset	Access			
0x0701	DC offset calibration control (local)	[7:0]	DC offset calibration control	0x06	Disabled.	0x06	R/W			
			DC offset calibration control	0x86	Enabled.					
0x073B	DC Offset Calibration Control 2 (local)	[7:0]	DC Offset Calibration Accumulator Reset	0xB7	Synchronous reset DC offset calibration accumulator.	0xB7	R/W			
			DC Offset Calibration Accumulator Reset	0x37	Accumulator reset (for 0x0701=0x06). Accumulator reset release (for 0x0701=0x86).					
0x18A6	VREF control	[7:1]	Reserve		Reserved.	0x0	Read			
			0	VREF control	0	Internal reference clock signal.	0x0	R/W		
0x18E3	External VCM buffer control	7	Reserve		Reserved.	0x0	Read			
			6	External V _{CM} buffer	0	Disabled.	0x0	R/W		
			1	External V _{CM} buffer	1	Enabled.	0x0	R/W		
0x18E3	External VCM buffer control	[5:0]	External V _{CM} buffer [5:0]		See the input common mode section.	0x0	R/W			
			External V _{CM} buffer [5:0]		See the input common mode section.	0x0	R/W			
0x18E6	Temperature diode export	[7:0]	Temperature diode placement selection	0x00	Central diode output. VREF pin = high level-Z.	0x0	R/W			
			Temperature diode placement selection	0x01	Central diode output. VREF pin = 1x diode voltage output.					
			Temperature diode placement selection	0x02	Central diode output. VREF pin = 20x diode voltage output.					
			Temperature diode placement selection	0x03	Central diode output. VREF pin = GND.					
			Temperature diode placement selection	0x40	Channel A diode output. VREF pin = high level-Z.					
			Temperature diode placement selection	0x41	Channel A diode output. VREF pin = 1x diode voltage output.					
			Temperature diode placement selection	0x42	Channel A diode output. VREF pin = 20x diode voltage output.					
			Temperature diode placement selection	0x43	Channel A diode output. VREF pin = GND.					
			Temperature diode placement selection	0x50	Channel B diode output. VREF pin = high level-Z.					
			Temperature diode placement selection	0x51	Channel B diode output. VREF pin = 1x diode voltage output.					
0x1908	Analog input control (local)	[7:3]	Reserve		Reserved.	0x0	Read			
			2	Enable DC coupling	0	Optimize analog input for AC coupling.	0x0	R/W		
0x1908	Analog input control (local)	[1:0]	Reserve		Reserved.	0x0	Read			
			1	Enable DC coupling	1	Optimize analog input for DC coupling.	0x0	R/W		
			Reserve		Reserved.	0x0	Read			
0x1910	Input full-scale control (local)	[7:4]	Reserve		Reserved.	0x0	Read			
			[3:0]	Full-scale voltage		Full-scale voltage setting.	0xD	R/W		
				1000	1.13 V pp differential voltage.					
				1001	1.25 V pp differential voltage.					
				1101	1.7 V pp differential voltage.					
				1110	1.81 V pp differential voltage.					
				1111	1.93 V pp differential voltage.					
				0000	2.04 V pp differential voltage.					
0x1A48	High frequency setting (local)	[7:0]	High frequency setting	0x14	The first Nyquist operation.	0x14			R/W	
			High frequency setting	0x54	A second or higher Nyquist operation.					
0x1A4C	Buffer Control 1 (local)	[7:6]	Reserve		Reserved.	0x0	Read			
			[5:0]	Buffer control 1		Input buffer main current 1. See the Analog Input Buffer Control and SFDR Optimization section.	0x0	R/W		
0x1A4C	Buffer Control 1 (local)	[5:0]	001111	The buffer current is set to 300 μA .						
			000100	The buffer current is set to 400 μA .						
			001001	The buffer current is set to 500 μA .						
			011110	The buffer current is set to 600 μA .						
			100011	The buffer current is set to 700 μA .						
			101000	The buffer current is set to 800 μA .						
			101101	The buffer current is set to 900 μA .						
			110010	The buffer current is set to 1000 μA .						
			0x1A4D	Buffer Control 2 (local)	[7:6]	Reserve		Reserved.	0x0	Read
						[5:0]	Buffer control 2		Input buffer main current 2. See the Analog Input Buffer Control and SFDR Optimization section.	0x0
0x1A4D	Buffer Control 2 (local)	[5:0]	001111	The buffer current is set to 300 μA .						
			000100	The buffer current is set to 400 μA .						
			001001	The buffer current is set to 500 μA .						
			011110	The buffer current is set to 600 μA .						
			100011	The buffer current is set to 700 μA .						
			101000	The buffer current is set to 800 μA .						
			101101	The buffer current is set to 900 μA .						
			110010	The buffer current is set to 1000 μA .						

19. Precautions

● Product installation precautions:

- 1) Please pay attention to the orientation of the components when soldering to avoid soldering them incorrectly.
- 2) All instruments and meters used for circuit debugging must have a good, unified ground. The PCB design must ensure proper grounding and power decoupling.
- 3) Care should be taken not to reverse the power supply or short-circuit the input/output terminals with the power supply, as this can easily damage the circuit.
- 4) This product has a moisture sensitivity rating of MSL3. The permissible time for the product to be exposed to the external environment after being removed from the moisture-proof bag, dried, or baked, until reflow soldering is : $\leq 30^{\circ}\text{C}/60\text{RH}\%$, 168h.
- 5) If the storage conditions of the device cannot be controlled or traced, please strictly follow the baking process of 125°C for 24 hours before electrical assembly.
- 6) If the ambient temperature and humidity of the electrical installation environment cannot be guaranteed to be $\leq 30^{\circ}\text{C}/60\text{RH}\%$, please complete the soldering within 12 hours after baking.
- 7) After the product is baked, it is very easy to generate static electricity, so ESD protection should be taken into account during all operations.
- 8) When using leaded reflow soldering (Sn63Pb37) for board-level assembly, the recommended peak temperature range is $210^{\circ}\text{C}\sim 220^{\circ}\text{C}$, and the maximum peak temperature should not exceed 235°C . The dwell time within $\pm 5^{\circ}\text{C}$ of the peak temperature should be $\leq 20\text{s}$, and the dwell time above the liquidus line should be $60\sim 90\text{s}$. The heating rate is $2\sim 4^{\circ}\text{C}/\text{s}$, and the cooling rate is $\leq 2^{\circ}\text{C}\sim 6^{\circ}\text{C}$.
- 9) When using lead-free reflow soldering (SAC305) for board-level assembly, the recommended peak temperature range is $230^{\circ}\text{C}\sim 245^{\circ}\text{C}$, and the maximum peak temperature should not exceed 260°C . The dwell time within $\pm 5^{\circ}\text{C}$ of the peak temperature should be $\leq 20\text{s}$, and the dwell time above the liquidus line should be $60\sim 90\text{s}$. The heating rate is $2\sim 4^{\circ}\text{C}/\text{s}$, and the cooling rate is $\leq 2^{\circ}\text{C}\sim 6^{\circ}\text{C}$.
- 10) If the hybrid assembly process requires increased temperature, the device body temperature should be ensured not to exceed 260°C . (The device body temperature measurement point is located on the upper surface of the device during reflow soldering).
- 11) The surface treatment of the soldering end of this product is nickel-gold/OSP (depending on the actual situation), but the gold content is less than 3%, so there will be no gold brittleness and no need for tinning.
- 12) If mandatory tinning is required, tinning should be performed according to the "National Aerospace Industry Standard QJ3267 Technical Requirements for Tinning Process of Electronic Components". Note that components must be dried before tinning, the tinning temperature should not exceed 300°C , the heating time for each of the four leads should be less than 5 seconds, the heating time for the heat sink surface should be less than 30 seconds, and the number of tinning operations should not exceed one.

● Product usage precautions:

- 1) It is recommended to reset the circuit first after powering on (set 0x81 to the 0x0000 register) before using it.
- 2) It is recommended to pay attention to the ambient temperature and ensure proper heat dissipation during actual use.
- 3) After configuring digital functions such as DDC and 204B, it is recommended to perform a soft reset of the data path (set 0x0001 register to 0x02).
- 4) If the input signal exceeds the rated input range, it is recommended to perform a soft reset of the data path after it returns to the normal input range. Note that all ports marked with positive and negative (such as SYSREF \pm , etc.) should be used in accordance with the positive and negative markings. Under normal circumstances, register 0x0120[4] is 0; when the SYSREF \pm pin is reversed with the \pm pin of the external clock circuit, register 0x0120[4] should be set to 1.
- 5) If a drastic change in the circuit's peripheral configuration (such as clock or power supply) causes a function interruption, it is recommended to perform a soft reset of the data path (set 0x0001 register to 0x02) once the peripheral configuration is restored.
- 6) Setting 0x0738 to 0x18 and 0x073e to 0x08 disables some online algorithms, which will reduce the SNR by about 1dB, but improve the ADC's anti-interference capability.

● Product protection precautions:

- 1) Electrostatic charges can easily accumulate on the human body and testing equipment and may discharge imperceptibly. Although this product has dedicated ESD protection circuitry, permanent device damage may occur upon exposure to high-energy electrostatic discharges. Therefore, appropriate ESD precautions are recommended to avoid device performance degradation or malfunction.
- 2) Exceeding the absolute maximum ratings may result in permanent damage to the device. These are only the rated maximum values and do not guarantee that the device will function properly under these conditions or under any other conditions beyond those shown in this datasheet. Prolonged operation at the absolute maximum ratings will affect the reliability of the device.
- 3) Plastic-encapsulated circuits are prone to moisture absorption, which can lead to delamination. When using them, care should be taken to keep the surrounding environment dry. When storing them, they should be vacuum-packed and stored in a dry environment at room temperature.

20. Common Faults and Troubleshooting Methods

- 1) No signal output: Check if the power supply voltage, input signal, and clock are correctly applied.
- 2) Device malfunction: Identify the device's operating mode and confirm that the configuration is correct.
- 3) Device malfunction: Check the power supply and ensure the power supply voltage is stable.

21. Packaging Information

External dimensions

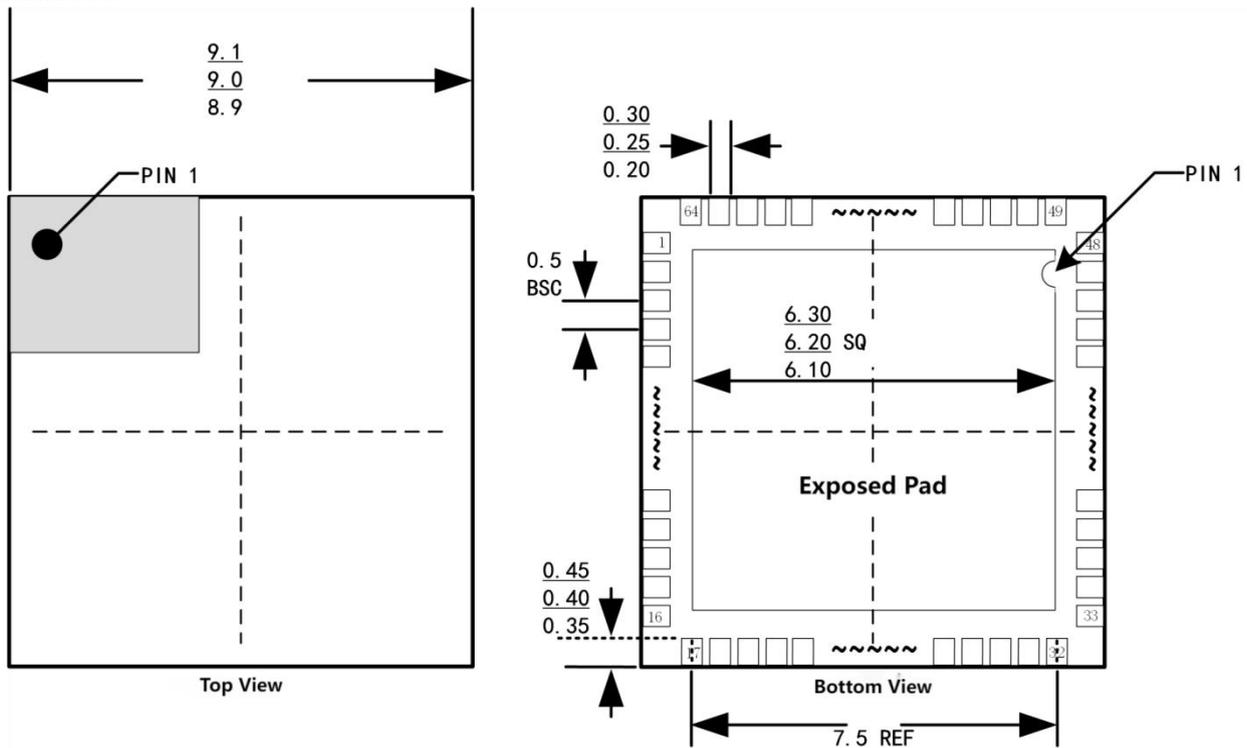


Figure 48. 64-pin QFN package

The unit of measurement for the dimensions shown in the illustration is mm.

22. Ordering Guide

Model	Temperature range	Package Description	Package
ADCP9695-23	-40 °C to +85°C	QFN-64	260/Reel