ADCP9689-32，Dual-Channel, 14-Bit, 2.6 GSPS ADC

1. Features

- Dual- channel 1-4 bit analog-to-digital converter
- 2.6GSPS conversion rate
- Integrated digital downconverter (DDCs) and programmable FIR filter
- SPI control interface
- JESD204B data output interface
- Operating temperature range: -40℃ to +85℃
- BGA196 package

2. Applications

- Multimode digital receiver
- Phased array radar
- Software radio
- Satellite receiver
- Instruments and Meters

3. Overview

The functional block diagram of the ADCP9689-32 dual-channel 14-bit 2.6GSPS analog-to-digital converter is shown in Figure 1. This device incorporates on-chip buffers and sample-and-hold circuitry, specifically designed for low power consumption, small size, and ease of use. It is designed for sampling wideband analog signals up to 9GHz. The device is optimized for wide input bandwidth, high sampling rates, and excellent linearity. This dual-channel ADC core employs a multi-stage, differential pipelined architecture and integrates output error correction logic. Each ADC has a wide-bandwidth input, supporting a variety of user-selectable input ranges. An integrated reference voltage source simplifies the design. Both the analog input and clock signals are differential input signals. A programmable threshold detector monitors the input signal power using the ADC's fast-detection output bit. If the input signal level exceeds the programmable threshold, the fast-detection indicator goes high. Due to the extremely short delay of this threshold indicator, users can quickly reduce the system gain, thereby avoiding over-range phenomena at the ADC input.

Users can configure the high-speed serial output based on Subclass 1 JESD204B to various single-channel, dual-channel, quad-channel, and eight-channel configurations according to the DDC configuration and the acceptable channel rate of the receiving logic device. Multi-device synchronization support is available via the SYSREF± and SYNCINB± input pins.

4. Device packaging information

Product Model	Packaging Type	Package Size
ADCP9689-32	BGA196	12mm×12mm

5. Functional Block Diagram

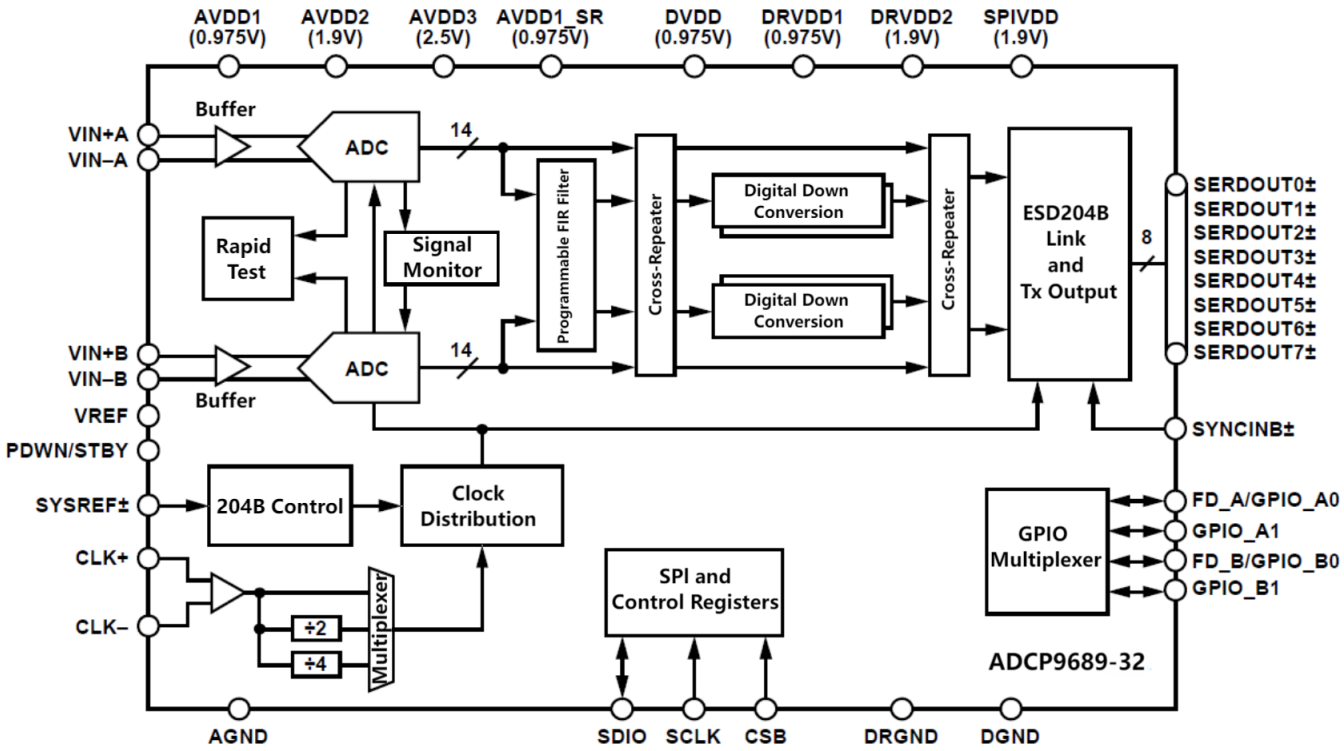

Figure 1. Functional Block Diagram

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Email：info@dsown.com

6. Pin Configuration and Functions

1	2	3	4	5	6	7	8	9	10	11	12	13	14	
AVDD2	AVDD2	AVDD1	AVDD1	AVDD1	AGND	CLK+	CLK–	AGND	AVDD1	AVDD1	AVDD1	AVDD2	AVDD2	A
AVDD2	AVDD2	AVDD1	AVDD1	AGND	AGND	AGND	AGND	AGND	AGND	AVDD1	AVDD1	AVDD2	AVDD2	B
AVDD2	AVDD2	AVDD1	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD1	AVDD2	AVDD2	C
AVDD3	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD3	D
VIN–B	AGND	AGND	AGND	AGND	AGND	AVDD1_SR	AGND	AGND	AGND	AGND	AGND	AGND	VIN–A	E
VIN+B	AGND	AGND	AGND	AGND	AGND	SYSREF+	SYSREF–	AGND	AGND	AGND	AGND	AGND	VIN+A	F
AVDD3	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD3	G
AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	VREF	AGND	AGND	AGND	AGND	H
AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	J
AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	K
DGND	GPIO_B1	SPI_VDD	FD_B/ GPIO_B0	CSB	SCLK	SDIO	PDWN/ STBY	FD_A/ GPIO_A0	SPI_VDD	GPIO_A1	DGND	DGND	DGND	L
DGND	DGND	DRGND	DRGND	DRVDD1	DRVDD1	DRVDD1	DRVDD1	DRGND	DRGND	DRVDD1	DRVDD	DRVDD2	DVDD	M
DVDD	DVDD	DRGND	SERDOUT7+	SERDOUT6+	SERDOUT5+	SERDOUT4+	SERDOUT3+	SERDOUT2+	SERDOUT1+	SERDOUT0+	DRGND	SYNCINB+	DVDD	N
DVDD	DVDD	DRGND	SERDOUT7–	SERDOUT6–	SERDOUT5–	SERDOUT4–	SERDOUT3–	SERDOUT2–	SERDOUT1–	SERDOUT0–	DRGND	SYNCINB–	DVDD	P

Figure 2. BGA196 Pin diagram

Pin Functions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
A1	AVDD2	Analog power supply (1.9V)	H1	AGND	Analog ground
A2	AVDD2	Analog power supply (1.9V)	H2	AGND	Analog ground
A3	AVDD1	Analog power supply (0.975V)	H3	AGND	Analog ground
A4	AVDD1	Clock domain analog power supply (0.975V)	H4	AGND	Analog ground
A5	AVDD1	Clock domain analog power supply (0.975V)	H5	AGND	Analog ground
A6	AGND	Clock domain analog ground	H6	AGND	Analog ground
A7	CLK+	Clock input (+)	H7	AGND	Analog ground
A8	CLK-	Clock input (−)	H8	AGND	Analog ground
A9	AGND	Clock domain analog ground	H9	AGND	Analog ground
A10	AVDD1	Clock domain analog power supply (0.975V)	H10	VREF	Reference power supply
A11	AVDD1	Clock domain analog power supply (0.975V)	H11	AGND	Analog ground
A12	AVDD1	Analog power supply (0.975V)	H12	AGND	Analog ground
A13	AVDD2	Analog power supply (1.9V)	H13	AGND	Analog ground
A14	AVDD2	Analog power supply (1.9V)	H14	AGND	Analog ground
B1	AVDD2	Analog power supply (1.9V)	J1	AGND	Analog ground
B2	AVDD2	Analog power supply (1.9V)	J2	AGND	Analog ground
B3	AVDD1	Analog power supply (0.975V)	J3	AGND	Analog ground
B4	AVDD1	Clock domain analog power supply (0.975V)	J4	AGND	Analog ground
B5	AGND	Analog ground	J5	AGND	Analog ground
B6	AGND	Clock domain analog ground	J6	AGND	Analog ground
B7	AGND	Clock domain analog ground	J7	AGND	Analog ground
B8	AGND	Clock domain analog ground	J8	AGND	Analog ground
B9	AGND	Clock domain analog ground	J9	AGND	Analog ground
B10	AGND	Analog ground	J10	AGND	Analog ground
B11	AVDD1	Clock domain analog power supply (0.975V)	J11	AGND	Analog ground
B12	AVDD1	Analog power supply (0.975V)	J12	AGND	Analog ground
B13	AVDD2	Analog power supply (1.9V)	J13	AGND	Analog ground
B14	AVDD2	Analog power supply (1.9V)	J14	AGND	Analog ground
C1	AVDD2	Analog power supply (1.9V)	K1	AGND	Isolated ground
C2	AVDD2	Analog power supply (1.9V)	K2	AGND	Isolated ground
C3	AVDD1	Analog power supply (0.975V)	K3	AGND	Isolated ground
C4	AGND	Analog ground	K4	AGND	Isolated ground
C5	AGND	Analog ground	K5	AGND	Isolated ground
C6	AGND	Clock domain analog ground	K6	AGND	Isolated ground
C7	AGND	Clock domain analog ground	K7	AGND	Isolated ground
C8	AGND	Clock domain analog ground	K8	AGND	Isolated ground
C9	AGND	Clock domain analog ground	K9	AGND	Isolated ground
C10	AGND	Analog ground	K10	AGND	Isolated ground
C11	AGND	Analog ground	K11	AGND	Isolated ground
C12	AVDD1	Analog power supply (0.975V)	K12	AGND	Isolated ground
C13	AVDD2	Analog power supply (1.9V)	K13	AGND	Isolated ground
C14	AVDD2	Analog power supply (1.9V)	K14	AGND	Isolated ground
D1	AVDD3	Analog power supply (2.5V)	L1	DGND	Digital ground
D2	AGND	Analog ground	L2	GPIO_B1	General purpose I/O port B1 bit
D3	AGND	Analog ground	L3	SPI_VDD	SPI digital power supply (1.9V)
D4	AGND	Analog ground	L4	FD_B/GPIO_B0	B channel rapid detection/General IO port B0 position

D5	AGND	Analog ground	L5	CSB	SPI chip select input
D6	AGND	Analog ground	L6	SCLK	SPI clock input
D7	AGND	Clock domain analog ground	L7	SDIO	SPI input/output terminals
D8	AGND	Clock domain analog ground	L8	PDWN/STBY	Power off/sleep terminal
D9	AGND	Analog ground	L9	FD_A/GPIO_A0	Channel A Fast Detection / General I/O Port A0 Bit
D10	AGND	Analog ground	L10	SPI_VDD	SPI digital power supply (1.9V)
D11	AGND	Analog ground	L11	GPIO_A1	General purpose I/O port A1 bit
D12	AGND	Analog ground	L12	DGND	Digital ground
D13	AGND	Analog ground	L13	DGND	Digital ground
D14	AVDD3	Analog power supply (2.5V)	L14	DGND	Digital ground
E1	VINB−	Channel B differential analog input (−)	M1	DGND	Digital ground
E2	AGND	Analog ground	M2	DGND	Digital ground
E3	AGND	Analog ground	M3	DRGND	Digital drive ground
E4	AGND	Analog ground	M4	DRGND	Digital drive ground
E5	AGND	Analog ground	M5	DRVDD1	Digital drive power supply (0.975V)
E6	AGND	SYSREF domain simulation	M6	DRVDD1	Digital drive power supply (0.975V)
E7	AVDD1_SR	SYSREF domain power supply (0.975V)	M7	DRVDD1	Digital drive power supply (0.975V)
E8	AGND	SYSREF domain simulation	M8	DRVDD1	Digital drive power supply (0.975V)
E9	AGND	Analog ground	M9	DRGND	Digital drive ground
E10	AGND	Analog ground	M10	DRGND	Digital drive ground
E11	AGND	Analog ground	M11	DRVDD1	Digital drive power supply (0.975V)
E12	AGND	Analog ground	M12	DRGND	Digital drive ground
E13	AGND	Analog ground	M13	DRVDD2	Digital drive power supply (1.9V)
E14	VINA−	Channel A differential analog input (−)	M14	DVDD	Digital power supply (0.975V)
F1	VINB+	Channel B differential analog input (+)	N1	DVDD	Digital power supply (0.975V)
F2	AGND	Analog ground	N2	DVDD	Digital power supply (0.975V)
F3	AGND	Analog ground	N3	DRGND	Digital drive ground
F4	AGND	Analog ground	N4	SERDOUT7+	Channel 7 outputs data (+)
F5	AGND	Analog ground	N5	SERDOUT6+	Channel 6 outputs data (+)
F6	AGND	Analog ground	N6	SERDOUT5+	Channel 5 outputs data (+)
F7	SYSREF+	System reference chip synchronization (+)	N7	SERDOUT4+	Channel 4 output data (+)
F8	SYSREF-	System reference chip synchronization (−)	N8	SERDOUT3+	Channel 3 output data (+)
F9	AGND	Analog ground	N9	SERDOUT2+	Channel 2 output data (+)
F10	AGND	Analog ground	N10	SERDOUT1+	Channel 1 output data (+)
F11	AGND	Analog ground	N11	SERDOUT0+	Channel 0 outputs data (+)
F12	AGND	Analog ground	N12	DRGND	Digital drive ground
F13	AGND	Analog ground	N13	SYNCINB+	Synchronize (+)
F14	VINA+	Channel A differential analog input (+)	N14	DVDD	Digital power supply (0.975V)
G1	AVDD3	Analog power supply (2.5V)	P1	DVDD	Digital power supply (0.975V)
G2	AGND	Analog ground	P2	DVDD	Digital power supply (0.975V)
G3	AGND	Analog ground	P3	DRGND	Digital drive ground
G4	AGND	Analog ground	P4	SERDOUT7−	Channel 7 output data (−)
G5	AGND	Analog ground	P5	SERDOUT6−	Channel 6 output data (−)
G6	AGND	Analog ground	P6	SERDOUT5−	Channel 5 output data (−)
G7	AGND	Analog ground	P7	SERDOUT4−	Channel 4 output data (−)
G8	AGND	Analog ground	P8	SERDOUT3−	Channel 3 output data (−)
G9	AGND	Analog ground	P9	SERDOUT2−	Channel 2 output data (−)
G10	AGND	Analog ground	P10	SERDOUT1−	Channel 1 output data (−)
G11	AGND	Analog ground	P11	SERDOUT0−	Channel 0 outputs data (−)
G12	AGND	Analog ground	P12	DRGND	Digital drive ground
G13	AGND	Analog ground	P13	SYNCINB−	Synchronization (−)
G14	AVDD3	Analog power supply (2.5V)	P14	DVDD	Digital power supply (0.975V)

7. Recommended working conditions

Parameter	Description
Power supply voltage (AVDD1) to AGND	1V~1.02V
Power supply voltage (AVDD1_SR) to AGND	0.975V~1.0V
Power supply voltage (AVDD2) to AGND	1.9V~1.95V
Power supply voltage (AVDD3) to AGND	2.5V~2.56V
Power supply voltage (DVDD) to AGND	0.975V~1.0V
Supply voltage (DRVDD1) to AGND	0.975V~1.0V
Supply voltage (DRVDD2) to AGND	1.9V~1.95V
Supply voltage (SPIVDD) to AGND	1.9V~1.95V
Operating temperature range	-40℃ ~+ 85℃

8. Absolute maximum ratings

Parameter	Description
Power supply voltage (AVDD1) to AGND	1.05V
Power supply voltage (AVDD1_SR) to AGND	1.05V
Power supply voltage (AVDD2) to AGND	2V
Power supply voltage (AVDD3) to AGND	2.7V
Power supply voltage (DVDD) to AGND	1.05V
Supply voltage (DRVDD1) to AGND	1.05V
Supply voltage (DRVDD2) to AGND	2V
Supply voltage (SPIVDD) to AGND	2V
AGND to DRGND	-0.3V to 0.3V
AGND to DGND	-0.3V to 0.3V
DGND to DRGND	-0.3V to 0.3V
VIN to AGND	AGND-0.3V to AVDD3+ 0.3V
CLK to AGND	AGND -0.3V to AVDD1+ 0.3V
SCLK, SDIO, CSB to AGND	DGND - 0.3V to SPI - VDD + 0.3V
PDWN/STBY to AGND	DGND - 0.3V to SPI - VDD + 0.3V
SYSREF to AGND	2.5V
SYNCINB to AGND	2.5V
Storage temperature (T_{stg})	-55℃ to +125℃
Junction temperature (T_J)	120℃

9. Performance Indicators

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resolution	RES			14		Bits
Power consumption	P_W			3.2	4.0	W
Power loss	P_D			400	500	mW
Signal-to-noise ratio	SNR	f_{IN} = 255MHz, -2.0dBFS	54	58.5		dBFS
		f_{IN} = 1.6GHz, -2.0dBFS	52	55		dBFS
		f_{IN} = 1.8GHz, -2.0dBFS	52	55		dBFS
Signal-to-noise ratio	SINAD	f_{IN} = 255MHz, -2.0dBFS	53	58		dBFS
		f_{IN} = 1.6GHz, -2.0dBFS	51	54		dBFS
		f_{IN} = 1.8GHz, -2.0dBFS	51	54		dBFS
Stray dynamic range	SFDR	f_{IN} = 255MHz, -2.0dBFS	56	70		dBFS
		f_{IN} = 1.6GHz, -2.0dBFS	56	66		dBFS
		f_{IN} = 1.8GHz, -2.0dBFS	56	66		dBFS
Second harmonic	HD2	f_{IN} = 255MHz, -2.0dBFS		-70	-56	dBFS
		f_{IN} = 1.6GHz, -2.0dBFS		-66	-56	dBFS
		f_{IN} = 1.8GHz, -2.0dBFS		-66	-56	dBFS
Third harmonic	HD3	f_{IN} = 255MHz, -2.0dBFS		-70	-56	dBFS
		f_{IN} = 1.6GHz, -2.0dBFS		-66	-56	dBFS
		f_{IN} = 1.8GHz, -2.0dBFS		-66	-56	dBFS
Significant digits	ENOB	f_{IN} = 255MHz, -2.0dBFS	8.5	9.3		Bits
		f_{IN} = 1.6GHz, -2.0dBFS	8.1	8.6		Bits
		f_{IN} = 1.8GHz, -2.0dBFS	8.1	8.6		Bits
JESD204B Lane Rate	f_{SDATA}			13	13	Gbps
JESD204B Lane Number of Passages	L			8	8	Lane
CSB Logic 1 Voltage	V_{IH}, CSB		1.2	1.2		V
CSB Logic 0 Voltage	V_{IL},CSB			0.6	0.6	V
SCLK Logic 1 Voltage	V_{IH}, SCLK		1.2	1.2		V
SCLK Logic 0 Voltage	V_{IL},SCLK			0.6	0.6	V
SDIO Logic 1 Voltage	V_{IH}, SDIO		1.2	1.2		V
SDIO logic 0 voltage	V_{IL},SDIO			0.6	0.6	V
Clock input frequency	f_{clk}			2600	2600	MHz
Sampling frequency	F_S			2.6	2.6	GSPS

10. Working Sequence

Parameter	Description	Min	Typ	Max	Unit
CLK+ to SYSREF+ Timing Requirements					
t_{SU_SR}	Device clock to SYSREF + setup time		-65		ps
t_{H_SR}	Device clock to SYSREF + hold time		95		ps
SPI Timing Requirements					
t_{DS}	Setup time between data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between data and the rising edge of SCLK	2			ns
t_{CLK} is used for SPI reading.	SCLK cycle	20			ns
t_{CLK} is used for SPI writing.	SCLK cycle	10			ns
t_{S}	Establishment time between CSB and SCLK	2			ns
t_{H}	Establishment time between CSB and SCLK	2			ns
t_{HIGH} is used for SPI reading.	The shortest time that SCLK must be in a logic high state	8			ns
t_{HIGH} is used for SPI writing.	The shortest time that SCLK must be in a logic high state	4			ns
t_{LOW} is used for SPI reading.	The shortest time SCLK must be in a logic low state	8			ns
t_{LOW} is used for SPI writing.	The shortest time SCLK must be in a logic low state	4			ns
t_{ACCESS}	The maximum time delay between the falling edge of SCLK and the validity of the output data.		5	8	ns
t_{DIS_SDIO}	The time required for an SDIO pin to switch from output to input relative to the rising edge of SCLK (not shown in the diagram below).	2			ns

Time series diagram

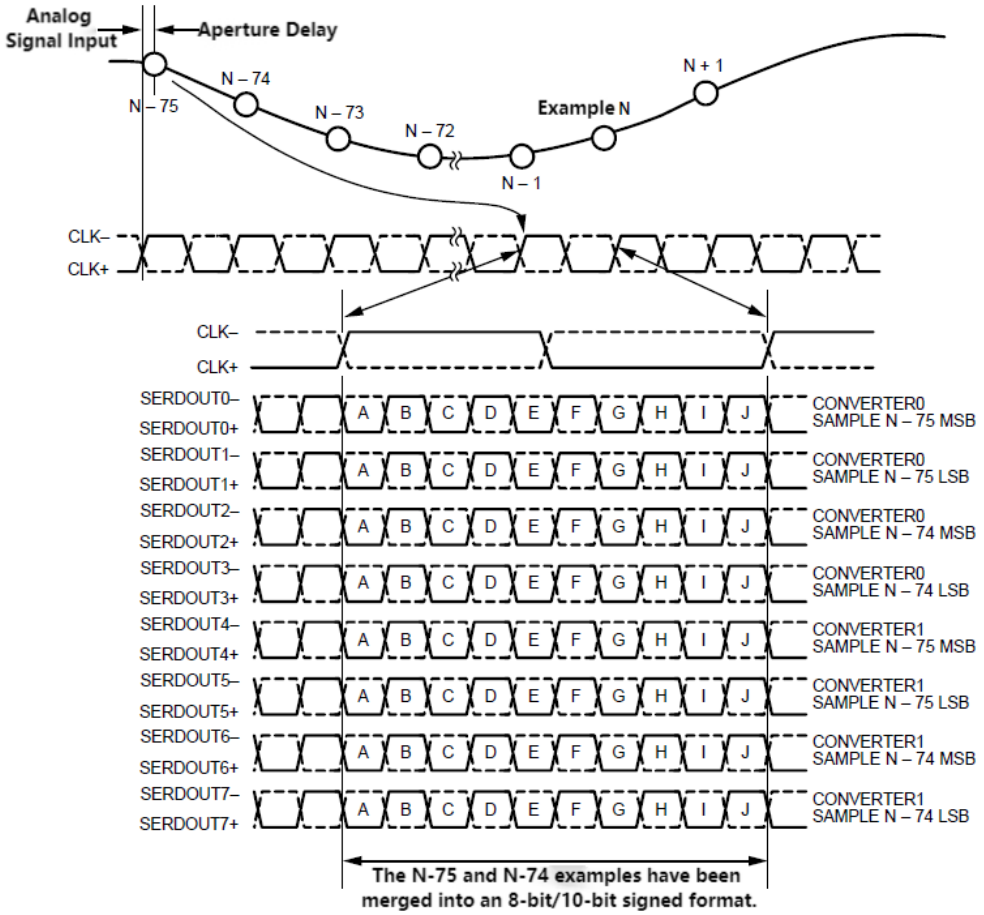


Figure 3. Data Output Timing Diagram

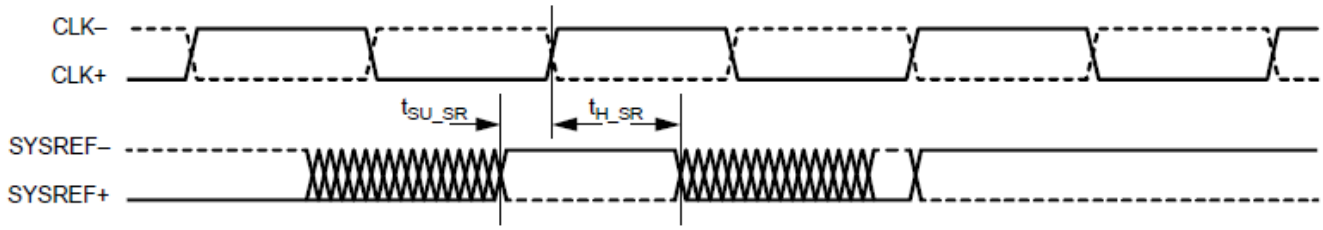


Figure 4. Timing Diagram for CLK+ to SYSREF+ Setup and Hold

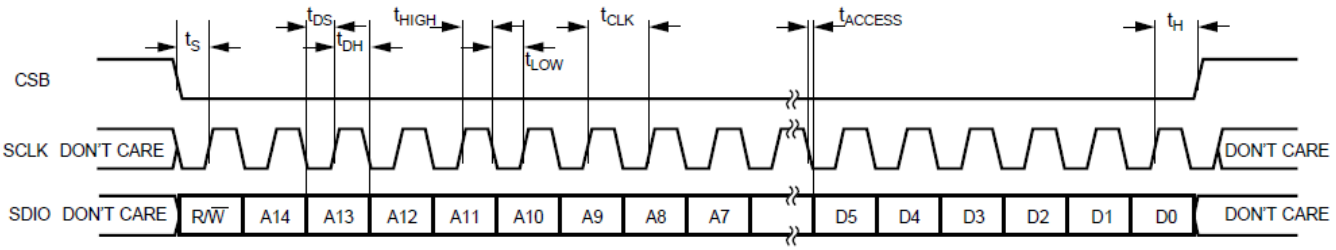


Figure 5. SPI Interface Timing Diagram

11. Differential Input Configuration

To achieve good dynamic performance, this product requires differential inputs at its analog input terminals. The recommended low-frequency and high-frequency input signal configurations are shown below.

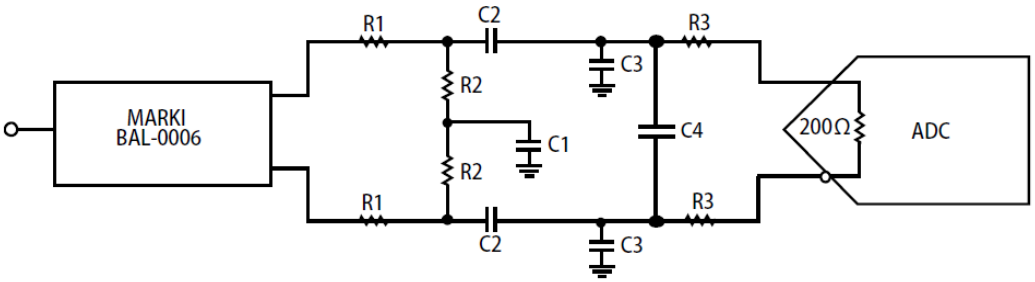


Figure 6. Low - frequency input signal configuration

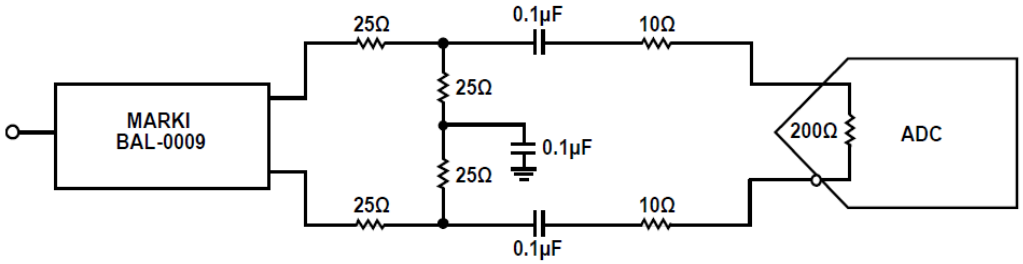


Figure 7. High -frequency input signal configuration

Input signal configuration component parameter table

Frequency range	Transformer	R1	R2	R3	C1	C2	C3	C4
<5000 MHz	BAL-0006	25 Ω	25 Ω	10 Ω	0.1 μF	0.1 μF	0.4 Pf	0.4 pF or open
>5000 MHz	BAL-0009	25 Ω	25 Ω	10 Ω	0.1 μF	0.1 μF	Open	Open

12. Clock Port

To achieve good dynamic performance, this product requires differential clock input. Below are some recommended clock input methods.

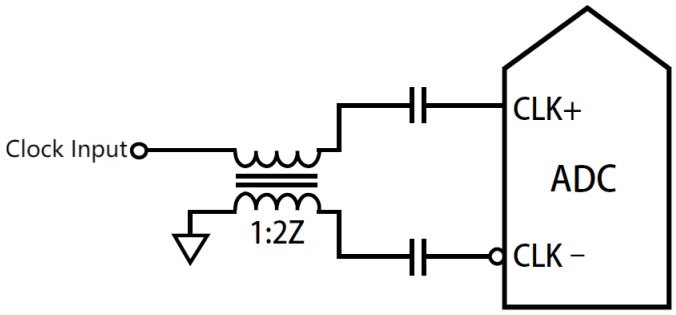


Figure 8. Transformer - coupled differential clock input

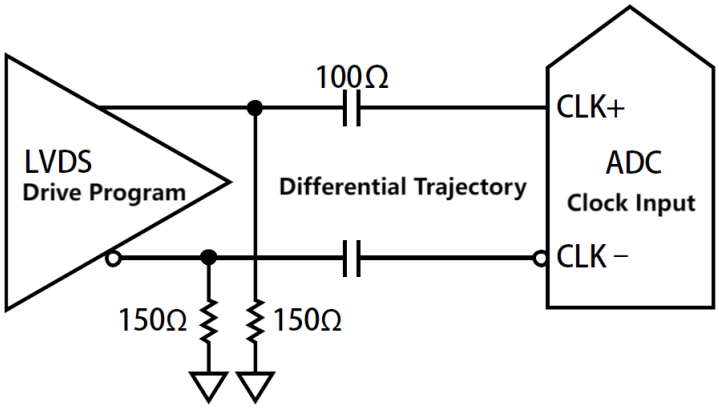


Figure 9. LVPECL Differential Clock Input

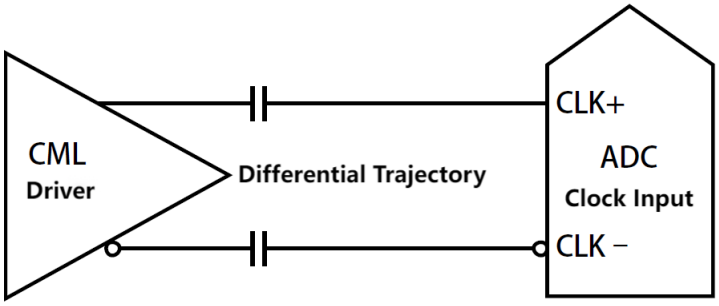


Figure 10. CML Differential Clock Input

13. ADC offset calibration

Offset calibration is disabled by default. It can be enabled by configuring registers 0x73B to 37 and registers 0x701 to 86.

14. Power- on /power - off requirements and power-on reset function

The current version offers two methods to ensure reliable power-on:

1. When the power-on sequence is controllable, the digital power supply DVDD should be powered on first, followed by other power supplies .
2. If the power-on sequence cannot be controlled, after all power supplies are powered on, reset the chip once through configuration registers 0x00 to 81.

15. Register Description

Memory Mapping

Read the memory-mapped register table

Each address in the memory-mapped register table is 8 bits. Memory mapping is divided into the following parts:

Name	Description
Analog circuit SPI register	0x0000 to 0x000F
Clock/SYSREF/Chip Power-Down Pin Control Register	0x003F to 0x01FF
Chip operating mode control register	0x0200 to 0x0201
Fast detection and signal monitoring control register	0x0245 to 0x027A
DDC Function Register	0x0300 to 0x03CD
Digital output and test mode register	0x0550 to 0x05CB and 0x1222 to 0x01262
Programmable filter control and coefficient register	0x0DF8 to 0x0F7F
VREF/Analog Input Control Register	0x18A6 to 0x1A4D and 0x0701 to 0x073B

The memory-mapped register records the hexadecimal value of each address in detail. For example, in the output sampling mode, the register address is 0x0561, and the default value is 0x01, which means that the least significant bit is 1 and the rest are 0.

Default Value

After a reset, critical registers are loaded with their default values. The default values for these registers are stored in the memory-mapped register table.

Logic Level

The logic level terminology is explained as follows:

1. " Bit set " means " the bit has been set to logic 1 " or " the bit has been written to logic 1 " .
2. " Clear bit" means "the bit has been set to logic 0" or "the bit has been written to logic 0" .
3. X represents an irrelevant bit.

Channel-Specific Registers

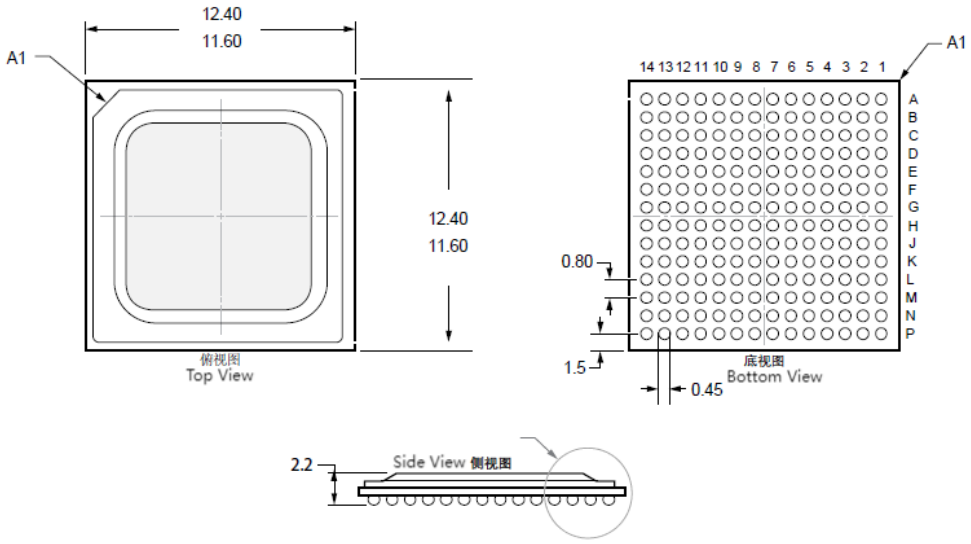
Some channel setting functions, such as the buffer control register (register 0x1A4C), can have different values for each channel. In this case, the register and bit addresses are essentially the same for each channel. These registers and bits can be accessed by setting the appropriate channel A or channel B register 0x0008. If both bits are set, subsequent writes will affect the registers for both channels. During a read cycle, only channel A or channel B is set when reading the register. If both bits are set during an SPI read cycle, the value for channel A is returned. All other registers and bits are considered global, and changes to these registers and bits affect the entire device; independent setting of channel functions is not allowed between channels. For example, settings in register 0x0005 do not affect global registers and bits.

SPI Soft Reset

After setting 0x81 to register 0x0000 and issuing a soft reset command, it takes 5ms to recover. When using this for application setup, ensure that the soft reset is programmed into the firmware with sufficient delay before starting operation.

16. Package Dimensions and Structure

BGA196 package



17. Ordering Guide

Product Model	Temperature Range	Packaging Type	Package Quantity
ADCP9689-32	-40 ℃ ~+85 ℃	BGA196	189/Tray