ADCP9656-125 4-Channel, 16-Bit, 125 MSPS, 204B Interface Synchronous

1. Characteristics

- Signal-to-noise ratio (SNR): 79 dBFS (9.7 MHz, VREF = 1.4 V)
- Signal-to-noise ratio (SNR): 77 dBFS (9.7 MHz, VREF = 1.0 V)
- Spurious-free dynamic range (SFDR): 85dBc (to the Nyquist frequency, VREF=1.4V)
- Spurious-free dynamic range (SFDR): 91 dBc (to the Nyquist frequency, VREF = 1.0 V)
- JESD204B Subclass1 encoding, serial digital output.
- Analog input range (adjustable): 2.0Vp-p/2.8Vp-p
- 1.8V power supply
- Low power consumption: ≤195mW per channel in 125MHz mode
- Differential nonlinearity (DNL): ±0.6 LSB
- Integral nonlinearity (INL): ±5.0 LSB
- 650MHz full-power analog input bandwidth
- Serial port control:
  - Full-chip, independent channel power-saving mode (Power Down)
  - Built-in and user-defined test modes
  - Multi-chip synchronization and clock division function
  - Standby mode

2. Applications

- Medical Imaging
- High-speed imaging
- Radio receiver
- Portable measuring devices

3. Overview

The ADCP9656-125 is a 4-channel, 16-bit, 125MSPS analog-to-digital converter (ADC) specifically designed for low power consumption, small size, and flexibility. This product offers a maximum conversion rate of 125MSPS, excellent dynamic performance, and ultra-low power consumption, making it suitable for a variety of applications. The ADC samples from a single 1.8V supply and uses an LVPECL/CMOS/LVDS compatible sampling clock signal. No external reference voltage source or driver is required. It supports independent shutdown of internal channels; with all channels disabled, typical power consumption is less than 14mW. The ADC incorporates various functions, including programmable clock output, data alignment, and digital test code generation. Available digital test codes include built-in fixed test codes and pseudo-random test codes, and user-defined test codes can also be created via the serial port interface (SPI).

4. Device Packaging Information

Product Model	Packaging Type	Package Size
ADCP9656-125	QFN-56	8.00mm×8.00mm

5. Functional Block Diagram

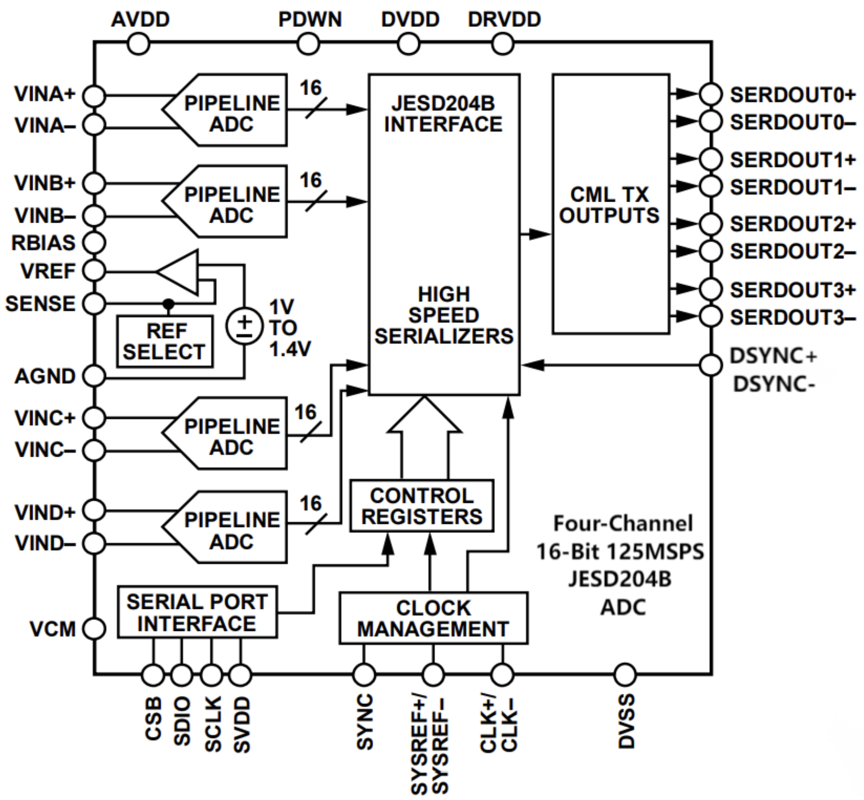

Figure 1. Functional Block Diagram

www.dsown.com
Email：info@dsown.com

6. Absolute Maximum Rating

Parameter	Values
Electrical	
AVDD to AGND	-0.3V to +2.0V
DRVDD to AGND	-0.3V to +2.0V
DVDD to DVSS	-0.3V to +2.0V
SVDD to AGND	-0.3V to +3.9V
Digital output to AGND	-0.3V to +2.0V
CLK+, CLK− to AGND	-0.3V to +2.0V
VINx +, VINx − to AGND	-0.3V to +2.0V
DSYSREF+, DSYSREF− to AGND	-0.3V to +2.0V
DSYNC−, DSYNC+ to AGND	-0.3V to +2.0V
SCLK, SDIO, CSB, PDWN to AGND	-0.3V to +3.9V
SYNC to AGND	-0.3V to +2.0V
RBIAS to AGND	-0.3V to +2.0V
VCM, VREF, SENSE to AGND	-0.3V to +2.0V
Environmental	
Operating temperature range (environment)	-40°C to +85°C
Maximum junction temperature	150°C
Pin temperature (soldering, 10 seconds)	300°C
Storage temperature range (ambient)	-65°C to +150°C

Note that exceeding the above absolute maximum ratings may result in permanent damage to the device. These are only the rated maximums and should not be used to infer whether the device will function properly under these conditions or under any other conditions beyond those shown in the Operation section of this technical specification. Prolonged operation under absolute maximum ratings conditions will affect the reliability of the device.

Thermal resistance: θ_{JA} is tested on a four-layer printed circuit board (PCB, simulation) with a solid ground plane. Exposed pads are soldered to the PCB ground.

Package type	Airflow velocity (m/s)	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} top (°C/W)	θ_{JC} bottom (°C/W)
56-pin QFN 8mm×8mm	0	22.4	7.7	7.42	2.29
	1	19.0	N/A	N/A	N/A
	2.5	17.6	N/A	N/A	N/A

www.dsown.com
Email：info@dsown.com

7. DC specification (VREF=1.4 V)

AVDD=1.8V, DRVDD=1.8V, 2.8Vp-p full-scale differential input, 1.4V reference voltage, unless otherwise specified, A_{IN} = -1.0dBFS.

Parameter	Temperature	Min	Typ	Max	Unit
Resolution			16		Bits
Accuracy					
No missing codes	25℃		Guaranteed		
Offset error	25℃		0.2		%FSR
Mismatch	25℃		0.05		%FSR
Gain error	25℃		1.2		%FSR
Gain Matching	25℃		0.95		%FSR
Differential nonlinearity (DNL)	25℃		±0.5		LSB
Integral nonlinearity (INL)	25℃		±5.0		LSB
Temperature drift					
Gain error	Full		5.2		ppm/℃
Offset error	Full		-2.5		ppm/℃
Internal reference voltage source					
Internal reference voltage source	25℃		1.4		V
Load regulation (1.0 mA)	25℃		4		mV
Input resistance	25℃		7.5		kΩ
Input equivalent noise					
V_{REF} = 1.4V	25℃		2.1		LSB rms
Analog Input					
Differential input voltage	25℃		2.8		V_{p-p}
Common mode voltage	25℃		0.9		V
Common mode range	25℃	0.7		1.1	V
Differential input resistor	25℃		2.6		kΩ
Differential input capacitor	25℃		7		pF
Power supply					
AVDD	25℃		1.8		V
DVDD, DRVDD	25℃		1.8		V
I_{AVDD} (125MSPS, 2Lanes)	25℃		288		mA
I_{DVDD} (125MSPS, 2Lanes)	25℃		67		mA
I_{DRVDD} (125MSPS, 2Lanes)	25℃		83		mA
Total power consumption					
DC input (125MSPS, 2Lanes)	25℃		706		mW
Sine wave input (125MSPS, 2Lanes)	25℃		788		mW
Power saving mode	25℃		14		mW
Standby mode	25℃		547		mW

8. DC specification (VREF=1.0 V)

AVDD=1.8V, DRVDD=1.8V, 2.0Vp-p full-scale differential input, 1.0V reference voltage, unless otherwise specified, A_{IN} = -1.0dBFS.

Parameter	Temperature	Min	Typ	Max	Unit
Resolution			16		Bits
Accuracy					
No missing codes	25℃		Guaranteed		
Offset error	25℃		0.2		%FSR
Mismatch	25℃		0.13		%FSR
Gain error	25℃		1.0		%FSR
Gain Matching	25℃		0.4		%FSR
Differential nonlinearity (DNL)	25℃		±0.5		LSB
Integral nonlinearity (INL)	25℃		±4.0		LSB
Temperature drift					
Gain error	Full		3.1		ppm/℃
Offset error	Full		-3		ppm/℃
Internal reference voltage source					
Internal reference voltage source	25℃		1.0		V
Load regulation (1.0 mA)	25℃		2		mV
Input resistance	25℃		7.5		kΩ
Input equivalent noise					
V_{REF} = 1.4V	25℃		2.7		LSB rms
Analog Input					
Differential input voltage	25℃		2.0		V_{p-p}
Common mode voltage	25℃		0.9		V
Common mode range	25℃	0.5		1.3	V
Differential input resistor	25℃		2.6		kΩ
Differential input capacitor	25℃		7		pF
Power supply					
AVDD	25℃		1.8		V
DVDD, DRVDD	25℃		1.8		V
I_{AVDD} (125MSPS, 2Lanes)	25℃		276		mA
I_{DVDD} (125MSPS, 2Lanes)	25℃		69		mA
I_{DRVDD} (125MSPS, 2Lanes)	25℃		83		mA
Total power consumption					
DC input (125MSPS, 2Lanes)	25℃		688		mW
Sine wave input (125MSPS, 2Lanes)	25℃		771		mW
Power saving mode	25℃		14		mW
Standby mode	25℃		520		mW

9. AC Specifications (VREF=1.4 V)

AVDD=1.8V, DRVDD=1.8V, 2.8Vp-p full-scale differential input, 1.4V reference voltage, unless otherwise specified, A_{IN} = -1.0dBFS.

Parameter	Temperature	Min	Typ	Max	Unit
Signal-to-noise ratio (SNR)					
f_{IN} = 9.7MHz	25℃		79.0		dBFS
f_{IN} = 16MHz	25℃		78.2		dBFS
f_{IN} = 64MHz	25℃		76.3		dBFS
f_{IN} = 128MHz	25℃		71.5		dBFS
f_{IN} = 201MHz	25℃		69.7		dBFS
f_{IN} = 301MHz	25℃		66.2		dBFS
Signal-to-noise ratio (SINAD)					
f_{IN} = 9.7MHz	25℃		78.3		dBFS
f_{IN} = 16MHz	25℃		77.7		dBFS
f_{IN} = 64MHz	25℃		75.2		dBFS
f_{IN} = 128MHz	25℃		70.9		dBFS
f_{IN} = 201MHz	25℃		68.7		dBFS
f_{IN} = 301MHz	25℃		65.9		dBFS
Significant digits (ENOB)					
f_{IN} = 9.7MHz	25℃		12.7		Bits
f_{IN} = 16MHz	25℃		12.6		Bits
f_{IN} = 64MHz	25℃		12.2		Bits
f_{IN} = 128MHz	25℃		11.5		Bits
f_{IN} = 201MHz	25℃		11.1		Bits
f_{IN} = 301MHz	25℃		10.7		Bits
Spurious-free dynamic range (SFDR)					
f_{IN} = 9.7MHz	25℃		93.2		dBc
f_{IN} = 16MHz	25℃		90.1		dBc
f_{IN} = 64MHz	25℃		82.8		dBc
f_{IN} = 128MHz	25℃		82.3		dBc
f_{IN} = 201MHz	25℃		76.1		dBc
f_{IN} = 301MHz	25℃		82.3		dBc
Worst harmonic (second or third order)					
f_{IN} = 9.7MHz	25℃		93.2		dBc
f_{IN} = 16MHz	25℃		90.1		dBc
f_{IN} = 64MHz	25℃		82.8		dBc
f_{IN} = 128MHz	25℃		82.3		dBc
f_{IN} = 201MHz	25℃		76.1		dBc
f_{IN} = 301MHz	25℃		82.3		dBc
Worst-case other harmonics (excluding second or third order)					
f_{IN} = 9.7MHz	25℃		-96		dBc
f_{IN} = 16MHz	25℃		-92		dBc
f_{IN} = 64MHz	25℃		-90		dBc
f_{IN} = 128MHz	25℃		-89		dBc
f_{IN} = 201MHz	25℃		-93		dBc
f_{IN} = 301MHz	25℃		-90		dBc
Two-tone intermodulation distortion (IMD): Input amplitude = -7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN1} = 72.5 MHz	25℃		-84		dBc
Crosstalk					
In-range crosstalk	25℃		-93		dB
Overrange crosstalk	25℃		-89		dB
Analog input bandwidth (full power)	25℃		650		MHz

10. AC Specifications (VREF=1.0 V)

AVDD=1.8V, DRVDD=1.8V, 2.0Vp-p full-scale differential input, 1.0V reference voltage, unless otherwise specified, A_{IN} = -1.0dBFS.

Parameter	Temperature	Min	Typ	Max	Unit
Signal-to-noise ratio (SNR)					
f_{IN} = 9.7MHz	25℃		77.4		dBFS
f_{IN} = 16MHz	25℃		77.1		dBFS
f_{IN} = 64MHz	25℃		75.3		dBFS
f_{IN} = 128MHz	25℃		71.9		dBFS
f_{IN} = 201MHz	25℃		69.2		dBFS
f_{IN} = 301MHz	25℃		65.8		dBFS
Signal-to-noise ratio (SINAD)					
f_{IN} = 9.7MHz	25℃		77.3		dBFS
f_{IN} = 16MHz	25℃		76.9		dBFS
f_{IN} = 64MHz	25℃		75.1		dBFS
f_{IN} = 128MHz	25℃		71.6		dBFS
f_{IN} = 201MHz	25℃		68.5		dBFS
f_{IN} = 301MHz	25℃		65.6		dBFS
Significant digits (ENOB)					
f_{IN} = 9.7MHz	25℃		12.5		Bits
f_{IN} = 16MHz	25℃		12.4		Bits
f_{IN} = 64MHz	25℃		12.2		Bits
f_{IN} = 128MHz	25℃		11.6		Bits
f_{IN} = 201MHz	25℃		11.1		Bits
f_{IN} = 301MHz	25℃		10.6		Bits
Spurious-free dynamic range (SFDR)					
f_{IN} = 9.7MHz	25℃		97.6		dBc
f_{IN} = 16MHz	25℃		94.9		dBc
f_{IN} = 64MHz	25℃		92.5		dBc
f_{IN} = 128MHz	25℃		86.0		dBc
f_{IN} = 201MHz	25℃		77.5		dBc
f_{IN} = 301MHz	25℃		80.3		dBc
Worst harmonic (second or third order)					
f_{IN} = 9.7MHz	25℃		-97.6		dBc
f_{IN} = 16MHz	25℃		-94.9		dBc
f_{IN} = 64MHz	25℃		-92.5		dBc
f_{IN} = 128MHz	25℃		-86.0		dBc
f_{IN} = 201MHz	25℃		-77.5		dBc
f_{IN} = 301MHz	25℃		-80.3		dBc
Worst-case other harmonics (excluding second or third order)					
f_{IN} = 9.7MHz	25℃		-95		dBc
f_{IN} = 16MHz	25℃		-95		dBc
f_{IN} = 64MHz	25℃		-94		dBc
f_{IN} = 128MHz	25℃		-89		dBc
f_{IN} = 201MHz	25℃		-91		dBc
f_{IN} = 301MHz	25℃		-89		dBc
Two-tone intermodulation distortion (IMD): Input amplitude = -7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN1} = 72.5 MHz	25℃		-89		dBc
Crosstalk					
In-range crosstalk	25℃		-94		dB
Overrange crosstalk	25℃		-89		dB
Analog input bandwidth (full power)	25℃		650		MHz

www.dsown.com
Email：info@dsown.com

11. Digital Specifications

AVDD=1.8V, DRVDD=1.8V, 2.8Vp-p full-scale differential input, 1.4V reference voltage, unless otherwise specified, A_{IN} = -1.0dBFS.

Parameter	Temperature	Min	Typ	Max	Unit
Clock inputs (CLK+, CLK-)					
Logical compatibility			CMOS/LVDS/LVPECL		
Differential input voltage range	Full	0.2		3.6	Vp -p
Input voltage range	Full	AGND−0.2		AVDD+0.2	V
Input common mode voltage	Full		0.9		V
Input resistance (differential)	25℃		15		kΩ
Input capacitor	25℃		4		pF
Enter DSYNC (DSYNC+ / DSYNC-)					
Logical compatibility	Full		LVDS		
Internal common-mode bias	Full		0.9		V
Differential input voltage range	Full	0.3		3.6	Vp -p
Input voltage range	Full	DGND		DVDD	V
Input common-mode voltage range	Full	0.9		1.4	V
High-level input current	Full	-5		+5	μA
Low-level input current	Full	-5		+5	μA
Input capacitor	Full		1		pF
Input resistance	Full	12	16	20	kΩ
Enter DSYSREF (DSYSREF+ / DSYSREF-)					
Logical compatibility	Full		LVDS		
Internal common-mode bias	Full		0.9		V
Differential input voltage range	Full	0.3		3.6	Vp -p
Input voltage range	Full	DGND		DVDD	V
Input common-mode voltage range	Full	0.9		1.4	V
High-level input current	Full	-5		+5	μA
Low-level input current	Full	-5		+5	μA
Input capacitor	Full		4		pF
Input resistance	Full	8	10	1 2	kΩ
Logical inputs (PDWN, SYNC, SCLK)					
Logic 1 Voltage Range	Full	1.2		AVDD+0.2	V
Logic 0 voltage range	Full	0		0.8	V
Input resistance	25℃		30		kΩ
Input capacitor	25℃		2		pF
Logical Input (CSB)					
Logic 1 Voltage Range	25℃	1.2		AVDD+0.2	V
Logic 0 voltage range	25℃	0		0.8	V
Input resistance	25℃		26		kΩ
Input capacitor	25℃		2		pF
Logical Input (SDIO)					
Logic 1 voltage range	25℃	1.2		AVDD+0.2	V
Logic 0 voltage range	25℃	0		0.8	V
Input resistance	25℃		2 6		kΩ
Input capacitor	25℃		5		pF
Digital outputs (SERDOUTx +, SERDOUTx -)					
Logical compatibility	Full		CML400		
Differential Output Voltage (VOD)	Full	400	600	750	mV
Output offset voltage (VOS)	Full	0.75	DRVDD/2	1.05	V

12. Switch Specifications

AVDD=1.8V, DRVDD=1.8V, 2.8Vp-p full-scale differential input, 1.4V reference voltage, unless otherwise specified, A_{IN} = -1.0dBFS.

Parameter	Temperature	Min	Typ	Max	Unit
Clock parameters					
Input clock rate	Full	40		1000	MHz
Conversion rate		40		125	MSPS
Width of the high-level pulse of the clock (t_{EH})			4		ns
Width of the low-level pulse of the clock (t_{EL})			4		ns
SYNC establishes time to clock				1.4	ns
SYNC hold time to clock				-0.4	ns
DSYSREF sets the time to the clock (t_{REFS})			370	600	ps
DSYSREF Hold Time to Clock (t_{REFH})			-92	0	ps
Data output parameters					
Data output period or unit interval (UI)	Full		L / (20 × M × fS)		Second
Data output duty cycle	25°C		50		%
Data validity period	25°C		0.81		UI
PLL lock time (t_{LOCK})	25°C		25		µs
Wake-up time					
Standby	25°C		250		ns
ADC (Power Saving Mode)	25°C		375		µs
Output (Power Saving Mode)	25°C		50		µs
DSYNC falling edge to the first character of K.28	Full	4			Multi-frame
Duration of K.28 character in CGS phase	Full	1			Multi-frame
Pipeline delay					
JESD204B M4, L1 mode (delay)	Full		23		cycle
JESD204B M4, L2 mode (latency)	Full		29		cycle
JESD204B M4, L2 mode (latency)	Full		44		cycle
Data rate per channel	Full			6.4	Gbps
Deterministic jitter (D_J)					
At 6.4Gbps	Full		8		Ps
Random jitter (R_J)					
At 6.4Gbps	Full		1.25		ps rms
Output rise time/fall time	Full		50		ps
Differential terminal resistor	25°C		100		Ω
Aperture parameters					
Aperture delay (t_A)	25°C		1		ns
Aperture uncertainty (jitter, t_J)	25°C		135		fs rms
Out-of-range recovery time	25°C		1		clock cycle

www.dsown.com
Email：info@dsown.com

13. Timing Specifications

Parameter	Description	Limit	Unit
t_{DS}	Setup time between data and the rising edge of SCLK	2	ns (minimum value)
t_{DH}	Hold time between data and the rising edge of SCLK	2	ns (minimum value)
t_{CLK}	SCLK cycle	40	ns (minimum value)
t_{S}	Establishment time between CSB and SCLK	2	ns (minimum value)
t_{H}	The holding time between CSB and SCLK	2	ns (minimum value)
t_{HIGH}	SCLK high-level pulse width	10	ns (minimum value)
t_{LOW}	SCLK low-level pulse width	10	ns (minimum value)
t_{EN_SDIO}	Compared to the falling edge of SCLK, it takes time for an SDIO pin to switch from the input state to the output state.	10	ns (minimum value)
t_{DIS_SDIO}	Compared to the falling edge of SCLK, it takes time for an SDIO pin to switch from an output state to an input state.	10	ns (minimum value)

Timing diagram

For SPI register settings, please refer to the "Memory Mapped Register Table" section.

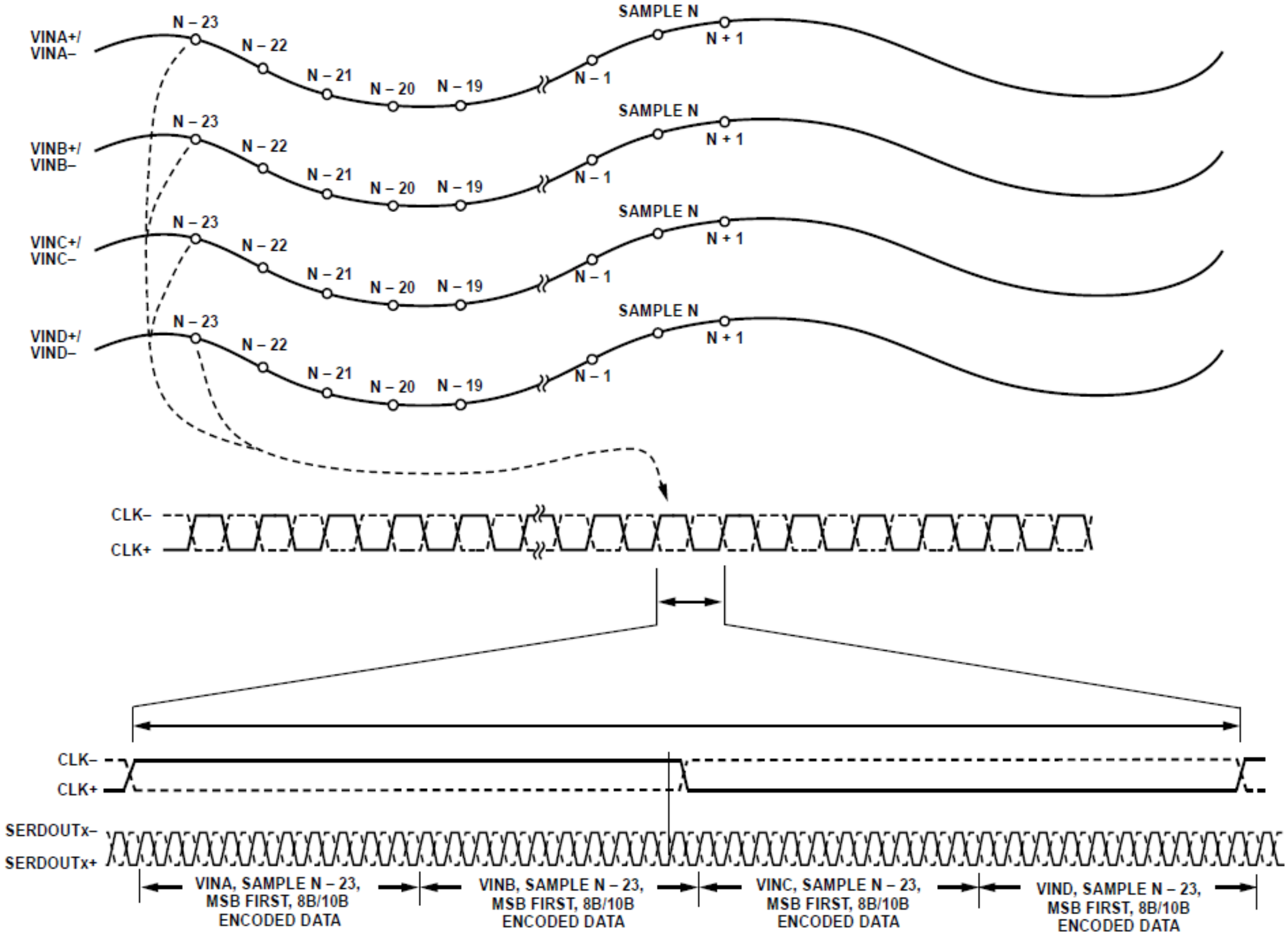

Figure 2. Data Output Timing

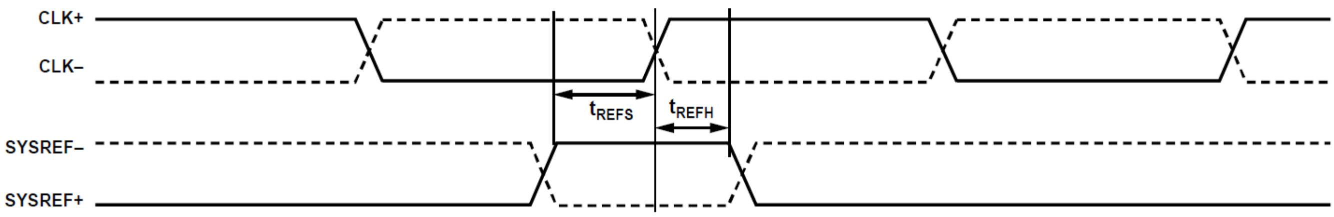

Figure 3. Setup and hold times for DSYSREF+/DSYSREF- (clock divider = 1)

14. Pin Configuration and Pin Functions

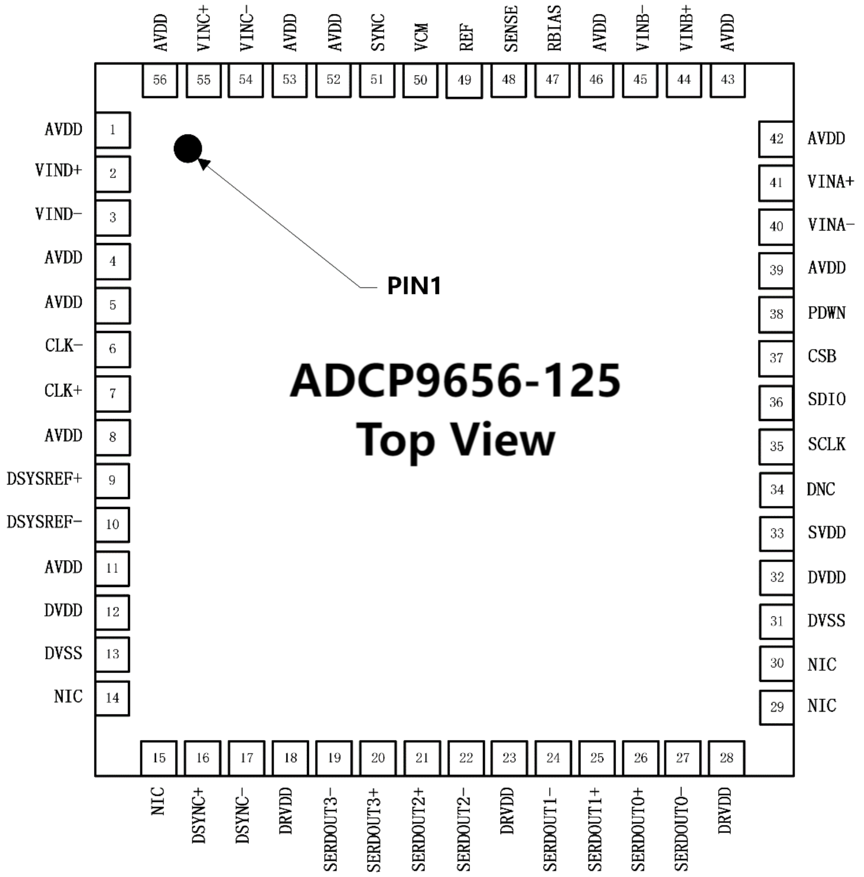

Figure 4. Pin configuration (top view)

Pin Functions

Pin Name	Pin Number	Description
AGND, exposed pad	0	Analog ground, the exposed thermal pads on the bottom of the package provide analog ground for the device.
AVDD	1, 4, 5, 8, 11, 39, 42, 43, 46, 52, 53, 56	1.8V analog power supply pin
VIND+	2	ADC D-channel analog input (+)
VIND-	3	ADC D-channel analog input (-)
CLK -,CLK +	6, 7	Differential clock, PECL, LVDS, or 1.8V CMOS input
DSYSREF+	9	JESD204B LVDS SYSREF Active Low Input (+)
DSYSREF-	10	JESD204B LVDS SYSREF Active Low Input (-)
DVDD	12, 32	Digital power pins
DVSS	13, 31	Digital ground pin
NIC	14, 15, 29, 30	Internally unconnected, grounding is possible when needed.
DSYNC+	16	JESD204B LVDS SYNC - Active low (+)
DSYNC-	17	JESD204B LVDS SYNC - Active low input (-)
DRVDD	18, 23, 28	Digital output drive power pin
SEROUT3-	19	Lane 3 Digital Output (-)
SEROUT3+	20	Lane 3 Digital Output (+)
SEROUT2+	21	Lane 2 Digital Output (+)
SEROUT2-	22	Lane 2 Digital Output (-)
SEROUT1-	24	Lane 1 Digital Output (-)
SEROUT1+	25	Lane 1 Digital Output (+)

Pin Functions (Continued)

Pin Name	Pin Number	Description
SEROUT0+	26	Lane0 Digital Output (+)
SEROUT0-	27	Lane0 Digital Output (-)
SVDD	33	SPI power pin
DNC	34	Do not connect this pin if it is not connected.
SCLK	35	SPI clock input
SDIO	36	SPI data input and output
CSB	37	SPI chip select signal, active low to enable, with built-in 30kΩ pull-up resistor.
PDWN	38	Digital input: High level = Off; Low level = On
VINA-	40	ADC A-channel analog input (-)
VINA+	41	ADC A-channel analog input (+)
VINB+	44	ADC B channel analog input (+)
VINB-	45	ADC B channel analog input (-)
RBIAS	47	Set the analog circuit bias, and connect the pin to a 10kΩ resistor to ground.
SENSE	48	Reference voltage mode selection
VREF	49	Reference voltage input and output pins
VCM	50	Analog input common-mode voltage
SYNC	51	Digital input, synchronous input of clock divider
VINC-	54	ADC C-channel analog input (-)
VINC+	55	ADC C-channel analog input (+)

15. Equivalent Circuit

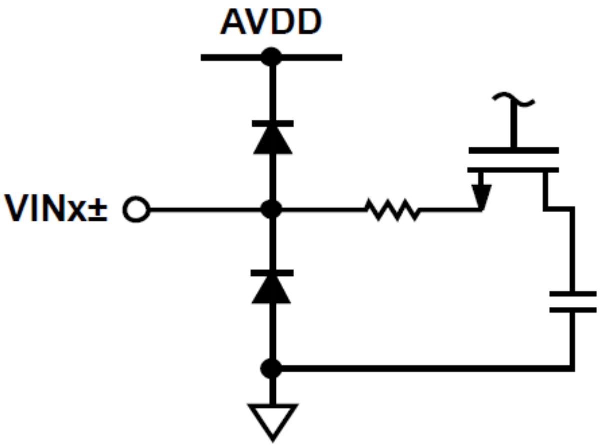

Figure 5. Equivalent analog input circuit diagram

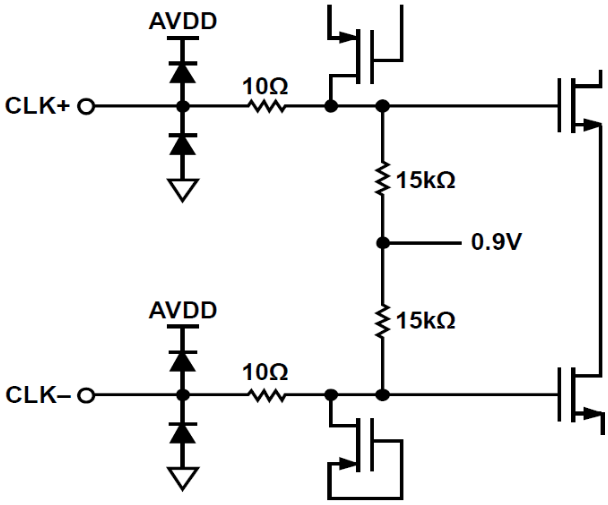

Figure 6. Equivalent clock input circuit

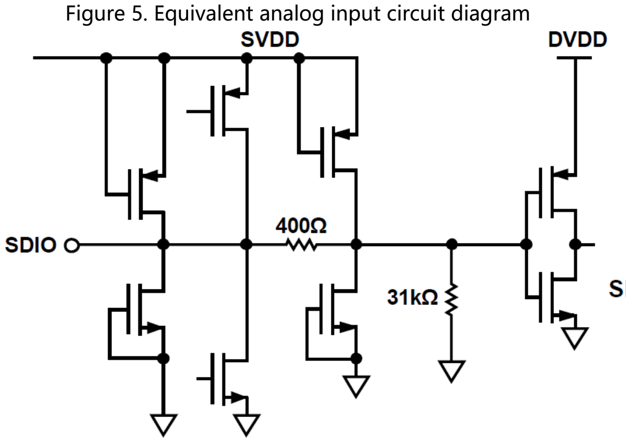

Figure 7. Equivalent SDIO input circuit diagram

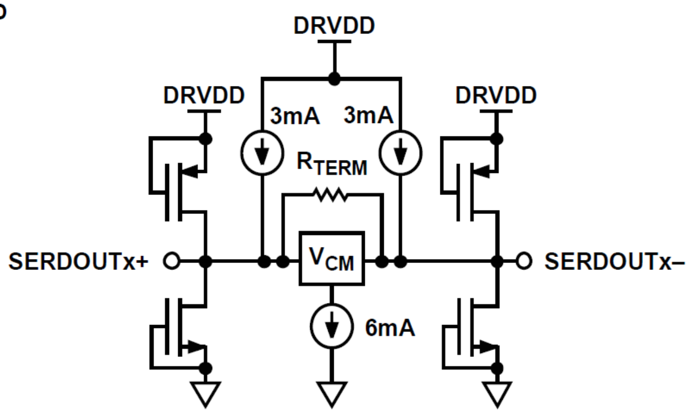

Figure 8. Equivalent SERDOUT ± circuit.

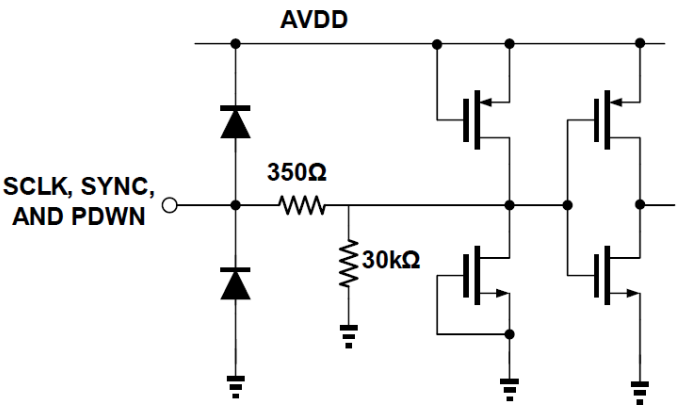

Figure 9. Equivalent SCLK , SYNC , and PDWN input circuits

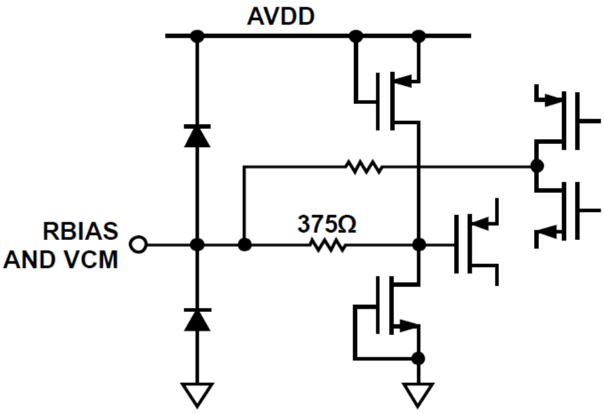

Figure 10. Equivalent RBIAS and VCM circuits

www.dsown.com
Email：info@dsown.com

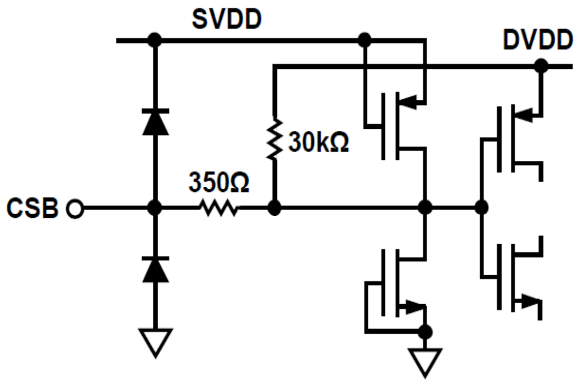

Figure 11. Equivalent CSB Input Circuit

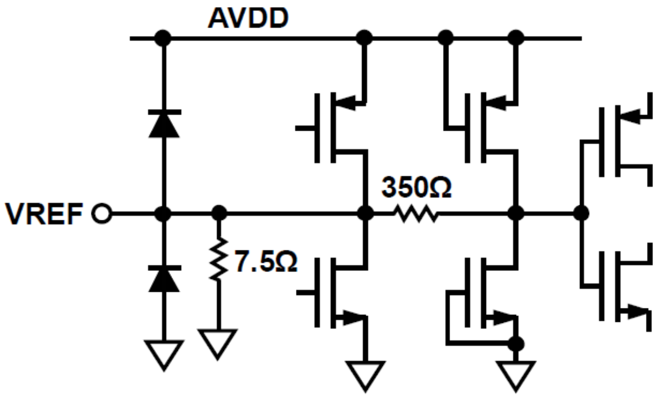

Figure 12. Equivalent VREF circuit

16. Working Principle

The product core uses a multi-stage pipelined ADC architecture, with each stage providing one redundant bit to eliminate offset errors from the coarse quantization comparator. Each stage's pipelined quantization structure is reconstructed in the digital domain by shift-adders to form a 16-bit conversion result. A serializer sends this conversion result in a 16-bit output format. Except for the last stage, each pipeline stage consists of a low-resolution Flash ADC, a connected switched-capacitor DAC, and an interstage margin amplifier (e.g., a multiplicative digital-to-analog converter [MDAC]). The margin amplifier amplifies the difference between the reconstructed DAC output and the Flash input to provide power to the next stage of the pipeline. To aid in digital correction of Flash errors, each stage provides one bit of redundancy. The final stage consists of only one Flash ADC.

- **Analog input terminal**

This product features a differential switched-capacitor circuit at its analog input, designed to handle differential input signals. This circuit supports a wide common-mode range while maintaining excellent performance. Signal correlation error is minimized and optimal performance is achieved when the input common-mode voltage is at the intermediate supply voltage.

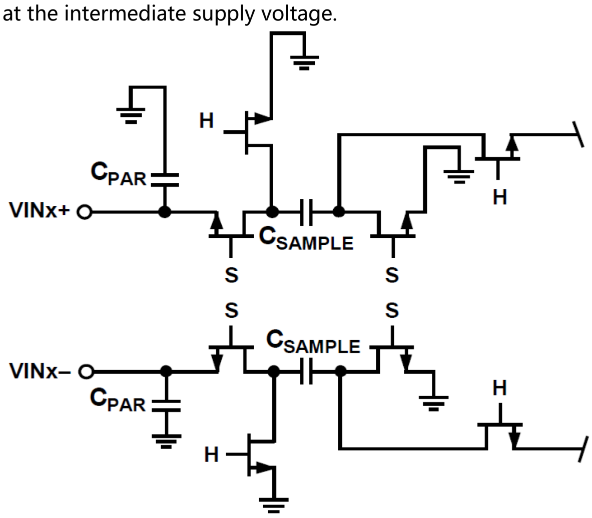

Figure 13. Switched Capacitor Input Circuit

The input circuitry switches between sample and hold modes based on the clock signal (see Figure 13). When the input circuitry switches to sample mode, the signal source must be able to charge the sampling capacitor and complete the build-up within half a clock cycle. A small resistor is connected in series at each input to help reduce peak transient current injected from the driver output stage. Furthermore, low-Q inductors or ferrite beads can be used on each side of the inputs to reduce the high differential capacitance at the analog inputs, thereby maximizing the ADC's bandwidth. Low-Q inductors or ferrite beads must be used when driving the converter front end at high-frequency (IF). A differential capacitor or two single-ended capacitors can be used at the inputs to provide a matched passive network. This ultimately forms a low-pass filter at the inputs to limit unwanted broadband noise.

- **Input common-mode level**

This product has no internal DC bias at the analog inputs; in AC-coupled applications, the user must provide an external bias. For optimal dynamic performance, the user must configure the device so that the input common-mode level VCM = AVDD/2. This device achieves reasonable performance over a wider input common-mode range, as shown in Figures 14 and 15.

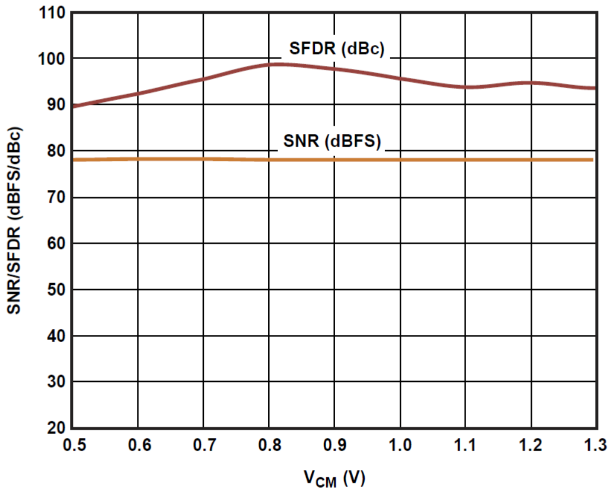

Figure 14. Relationship between SNR/SFDR and input common-mode level (V_{CM})
(f_{IN} =9.7MHz, f_{SAMPLE} =125MSPS, V_{REF} =1.0V)

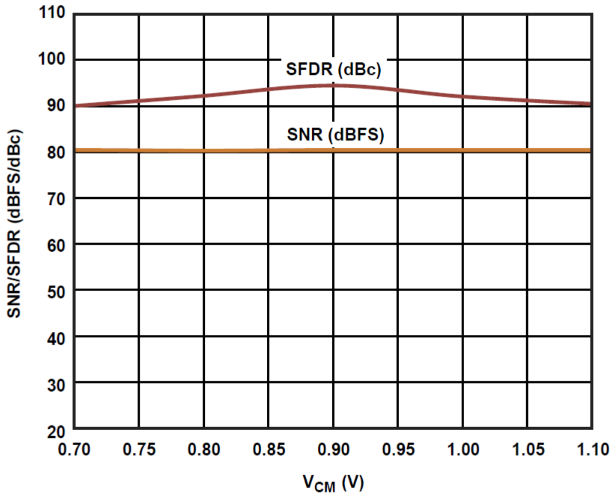

Figure 15. Relationship between SNR/SFDR and input common-mode level (V_{CM})
(f_{IN} =9.7MHz, f_{SAMPLE} =125MSPS, V_{REF} =1.4V)

This product provides an on-chip reference voltage via the VCM pin, which must be bypassed to ground using a 0.1F capacitor. In a differential configuration, setting the device input to its maximum range achieves the highest signal-to-noise ratio (SNR) performance. For this product, the input range depends on the reference voltage; performance deteriorates drastically beyond the input range.

- **Differential input configuration**

There are various active and passive methods to effectively drive this product. Differential driving can suppress even-order harmonics and achieve optimal performance. In baseband applications, using a differential balun configuration to drive this product provides excellent performance and a flexible interface for the ADC (see Figure 16). In applications where SNR is a critical parameter, because the noise performance of most amplifiers is insufficient to meet the true performance requirements of this product, a differential transformer coupling is required for the input configuration (see Figure 17) . In both of these applications, the value of capacitor C needs to be considered in conjunction with the input spectrum. It is recommended to reduce the capacitance or remove the capacitor when converting high-frequency analog input signals . Driving this product with a single-ended input is not recommended.

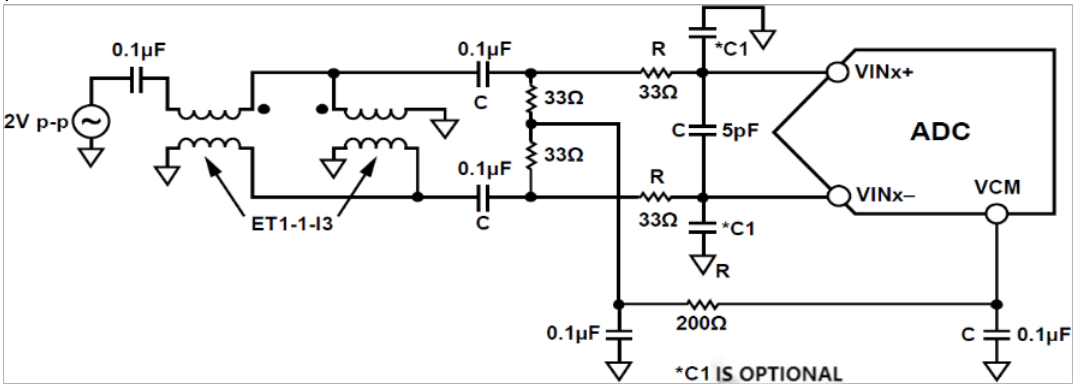

Figure 16. Differential double balun configuration

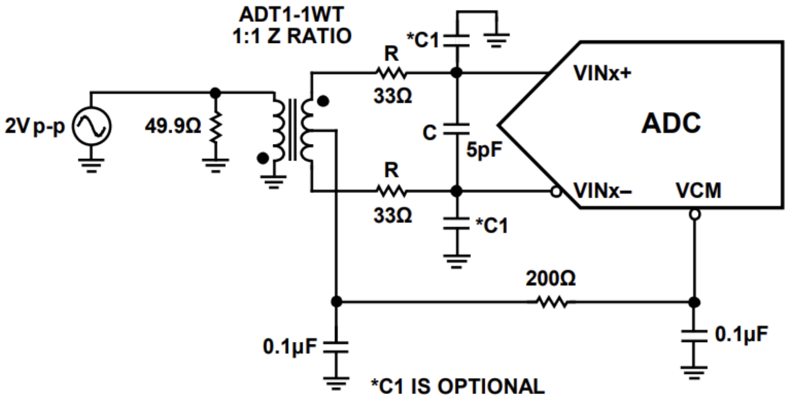

Figure 17. Differential transformer coupling

- **Reference voltage**

This product incorporates a stable and accurate reference voltage source. V_{REF} can be configured to generate a user-selectable reference voltage using an internal 1.0V reference voltage, an externally applied 1.0V to 1.4V reference voltage, or an external resistor divider acting on the internal reference voltage. See the "Internal Reference Voltage Connection" and "External Reference Voltage" sections for reference voltage source mode descriptions. The V_{REF} pin should be bypassed to ground through a parallel connection of an external 1.0µF capacitor with low equivalent series resistance (ESR) and a 0.1µF ceramic capacitor with low ESR. The product's built-in comparator detects the voltage at the SENSE pin, thus configuring the reference voltage to one of three possible modes. If the SENSE pin is grounded, the reference voltage amplifier switch is connected to the internal resistor divider (see Figure 18), thus setting the V_{REF} pin voltage V to 1.0V. If the SENSE pin is connected to an external resistor divider (see Figure 19), V_{REF} is defined as: $V_{REF} = 0.5\ x\left(1+\frac{R2}{R1}\right)$

Where 7kΩ≤(R1+R2)≤10kΩ

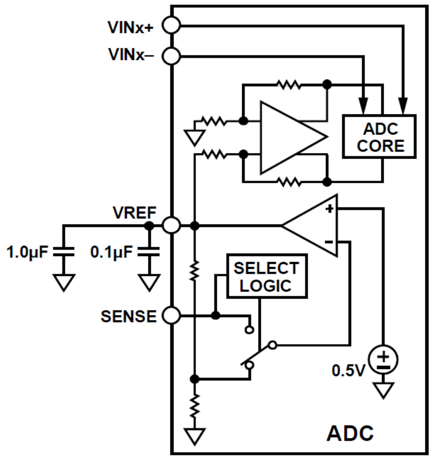

Figure 18. Reference Voltage Configuration 1

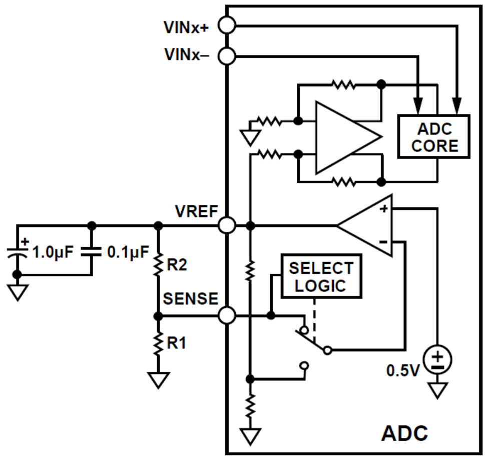

Figure 19. Reference Voltage Configuration 2

To utilize the product's internal reference voltage to drive multiple converters and improve gain matching, the load of other converters on the reference voltage must be considered. Figures 20 and 21 show how the load affects the internal reference voltage.

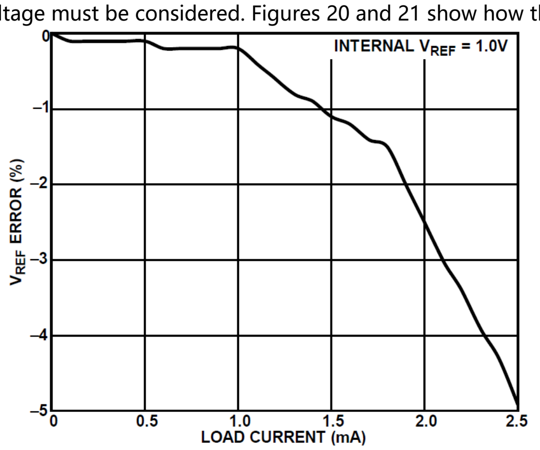

Figure 20. V_{REF} Error (Internal V_{REF} = 1.0V) vs. Load Current Graph

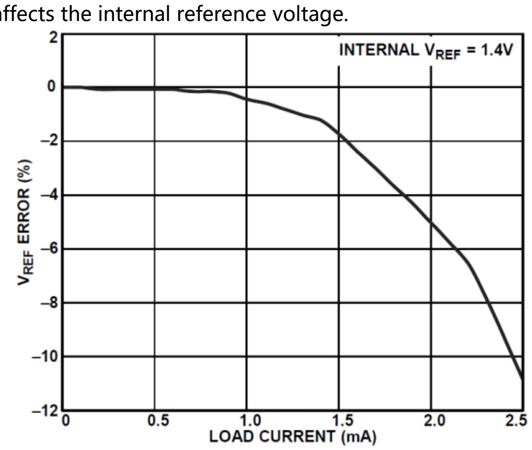

Figure 21. V_{REF} Error (Internal V_{REF} = 1.4V) vs. Load Current Graph

- **External reference voltage**

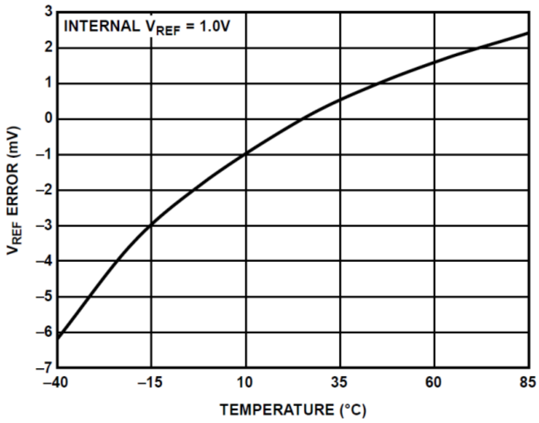

Figure 22. V_{REF} error and temperature relationship (V_{REF}=1.0V typical drift)

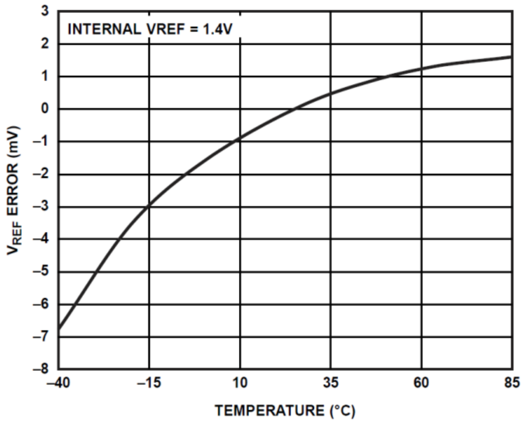

Figure 23. V_{REF} error and temperature relationship (V_{REF}=1.4V typical drift)

An external reference voltage is required to further improve ADC gain accuracy and thermal drift characteristics. Figures 22 and 23 show typical drift characteristics of the internal reference voltage source in 1.0V and 1.4V modes, respectively. Connecting the SENSE pin to AVDD disables the internal reference voltage source, allowing the use of an external reference voltage source. The internal reference voltage buffer provides a load equivalent to 7.5kΩ for an external reference voltage source. The internal buffer generates positive and negative full-scale reference voltages for the ADC core. Floating the SENSE pin is not recommended.

- **Clock input considerations**

To fully utilize the chip's performance, a differential signal should be used as the clock signal for the product's sampling clock inputs (CLK+ and CLK−). This signal is typically AC-coupled to the CLK+ and CLK− pins using a transformer or capacitor. These two pins have internal bias and require no external bias.

- **Clock input option**

This product features a flexible clock input configuration. CMOS, LVDS, LVPECL, or sine wave signals can all be used as its clock input. Regardless of the signal used, clock source jitter must be considered. Figures 24 and 25 show two preferred methods for providing the clock signal to this product (clock rates up to 1GHz before internal clock division). Using an RF transformer or RF balun, a single-ended signal from a low-jitter clock source can be converted to a differential signal. For clock frequencies from 125MHz to 1GHz, an RF balun configuration is recommended; for clock frequencies from 40MHz to 200MHz, an RF transformer configuration is recommended. A Schottky diode connected across the secondary winding of the transformer/balun limits the clock signal input to this product to approximately a differential peak-to- peak value of 0.8V (see Figures 24 and 25). This prevents large voltage swings from feeding into other parts of the product and preserves the fast rise and fall times of the signal, which is crucial for achieving low-jitter performance. However, at frequencies above 500MHz, diode capacitance can have an impact. Careful selection of an appropriate signal limiting diode is essential.

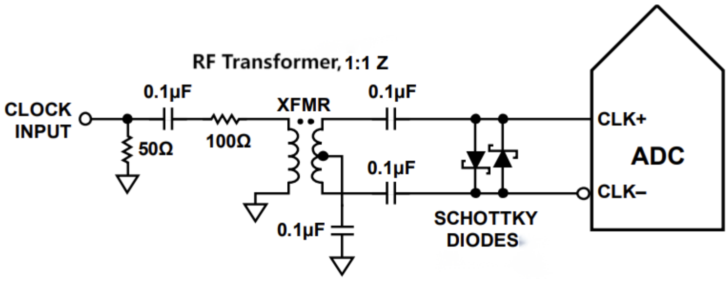

Figure 24. Transformer - coupled differential clock (frequency up to 200MHz)

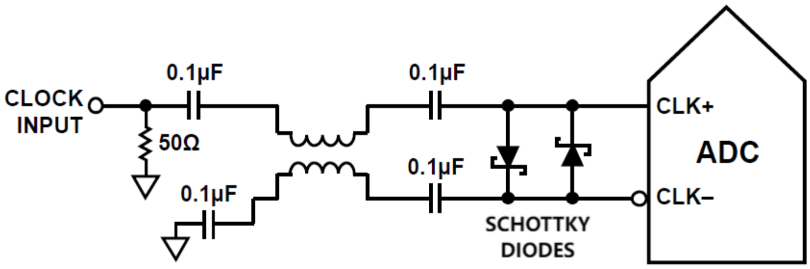

Figure 25. Balun-coupled differential clock (frequency up to 1 GHz)

If a low-jitter clock source is unavailable, an alternative is to AC couple the differential PECL signal to the sampling clock input pin, as shown in Figure 26.

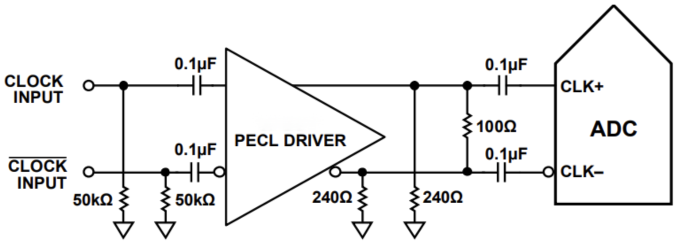

Figure 26. Differential PECL sampling clock (frequency up to 1GHz)

Another option is to AC couple the differential LVDS signal to the sampling clock input pin, as shown in Figure 27.

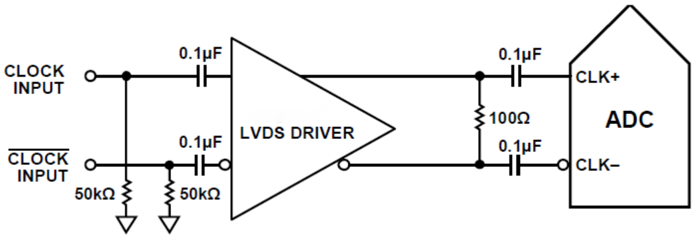

Figure 27. Differential LVDS sampling clock (frequency up to 1GHz)

In some applications, the sampling clock input can be driven by a single-ended 1.8V CMOS signal. In such applications, the CLK+ pin is driven directly from the CMOS gate, and the CLK- pin is bypassed to ground using a 0.1µF capacitor (see Figure 28).

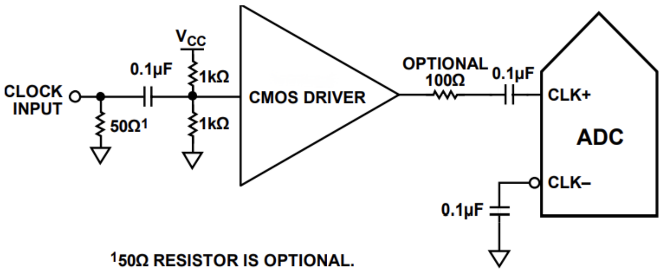

Figure 28. Single -ended 1.8V CMOS input clock (frequency up to 200MHz)

- **Input clock divider**

This product incorporates an input clock divider, capable of dividing the input clock by integer multiples from 1 to 8. The clock divider can be synchronized using an external SYNC input signal. By writing to bits 0 and 1 of register 0x109, the clock divider can be resynchronized upon each SYNC signal received, or only upon the first SYNC signal received. A valid SYNC resets the divider to its initial state. This synchronization feature allows the clock dividers of multiple devices to be aligned, ensuring simultaneous input sampling.

- **Clock duty cycle**

Typical high-speed ADCs utilize two clock edges to generate different internal timing signals, making them highly sensitive to clock duty cycle. Generally, to maintain the dynamic performance of an ADC, the clock duty cycle tolerance should be ±5%. This product incorporates a duty cycle stabilizer (DCS) that retims non-sampling edges (falling edges) and provides an internal clock signal with a nominal duty cycle of 50%. This feature minimizes performance degradation when the clock input duty cycle deviates from the nominal 50% duty cycle by more than ±5%. Enabling the DCS function significantly improves noise and distortion performance at clock input duty cycles of 30% to 45% and 55% to 70%. Input rising edge jitter remains a concern and cannot be easily reduced using internal stabilization circuitry. In applications with dynamically changing clock rates, the time constant associated with this loop must be considered. A waiting time of 1.5µs to 5µs is required before the DCS loop relocks the input signal.

- **Jitter consideration**

High-speed, high-resolution ADCs are highly sensitive to the quality of the clock input signal. Intermediate-frequency undersampling applications are particularly sensitive to jitter (see Figure 29). When aperture jitter could affect the dynamic range of the product, the clock input signal should be treated as an analog signal. Separate the clock driver power supply from the ADC output driver power supply to avoid introducing digital noise into the clock signal. A low-jitter crystal-controlled oscillator provides the optimal clock source. If the clock signal comes from other types of clock sources (via gating, frequency division, or other methods), retiming using the original clock is required in the final step.

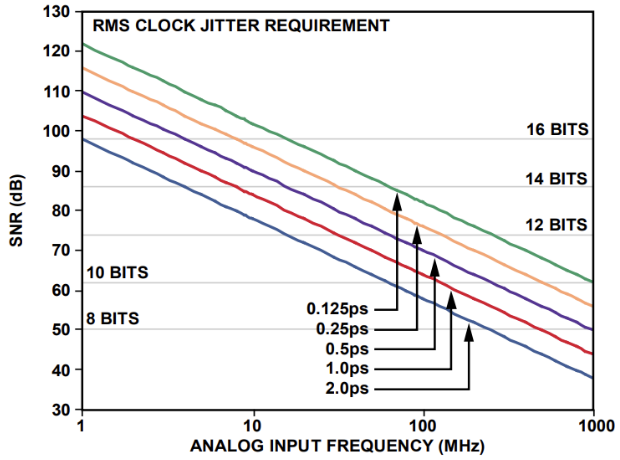

Figure 29. Relationship between ideal signal-to-noise ratio and analog input frequency and jitter

- **Power consumption and power saving mode**

As shown in Figures 30 and 31, the power consumption of this product is proportional to its sampling rate. This product can enter power-saving mode via the SPI port or by setting the PDWN pin high. In power-saving mode, the typical power consumption of the ADC is 14mW. In power-saving mode, the output driver is in a high-impedance state. Setting the PDWN pin low returns the product to normal operating mode. Note that PDWN is referenced to the data output driver supply voltage (DRVDD) and must not exceed this supply voltage. In power-saving mode, low power consumption is achieved by disabling the reference voltage source, reference voltage buffer, bias network, and clock. Internal capacitors discharge when entering power-saving mode; they must be recharged when returning to normal operating mode. Therefore, the wake-up time is related to the time spent in power-saving mode; the shorter the time spent in power-saving mode, the shorter the corresponding wake-up time. When using the SPI port interface, the user can place the ADC in power-saving mode or standby mode. For a shorter wake-up time, standby mode can be used, in which the internal reference voltage circuit is powered on. For more information on using these functions, see the "Memory Mapping" section.

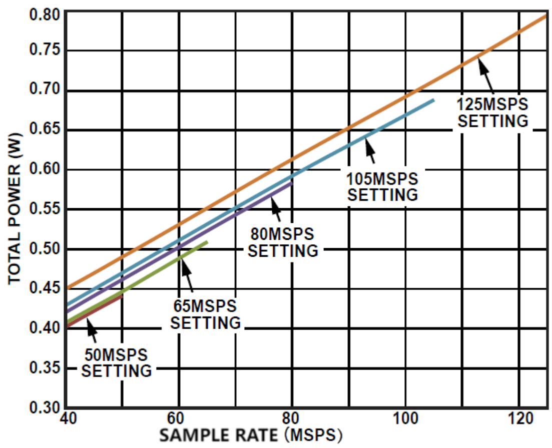

Figure30.Relationship between total power consumption and f_{SAMPLE} 9.7MHz, 4 channels, V_{REF} = 1.4V)

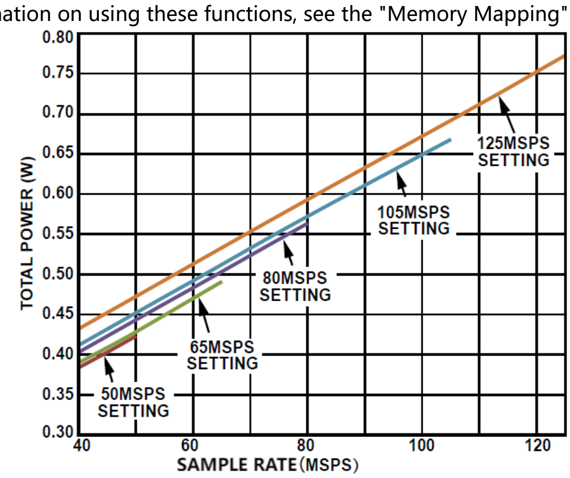

Figure31.Relationship between total power consumption and f_{SAMPLE} (f_{IN} = (f_{IN} = 9.7MHz , 4 channels, V_{REF} = 1.0V)

- **Digital output**

JESD204B Top-Level Description - This product's digital outputs adopt the JEDEC standard (standard number: JESD204B, Serial Interface for Data Converters). JESD204B is the protocol by which this product connects to digital processing devices via a serial interface (up to 6.4Gbps link speed). Advantages of the JESD204B interface include: less board space required for data interface routing, and smaller packages for converters and logic devices. This product supports single-channel, dual-channel, and quad-channel interfaces.

JESD204B Overview - The JESD204B data transmission module JTX combines parallel data from ADCs into data frames and outputs serial data using 8b/10b encoding and optional data scrambling. Channel synchronization is supported using special characters during initial link establishment; additional synchronization is implemented in subsequent data streams. A matched external receiver needs to be locked onto the serial data stream to restore data and clock. For more information on the JESD204B interface, please refer to the JESD204B standard. This product's JESD204B transmission module maps the outputs of four ADCs onto a link. The link can be configured to use single, dual, or quad serial differential outputs, referred to as channels. The JESD204B specification defines the link using several parameters that must match between the JESD204B transmitter (the output of this product) and the receiver.

The JESD204B link can be described by the following parameters:

1. S = Number of samples transmitted / Number of converters per frame (value is 1 for this product)
2. M = Number of converters / Number of converters (the value for this product is 4)
3. L = Number of channels / Converter (The value for this product is 1, 2, or 4)
4. N = Converter resolution (16 for this product)
5. N ' = The total number of digits in each sample (16 for this product)
6. CF = Control Words / Frame Clock Cycle / Converter (Value for this product is 0)
7. CS = Control bits / Transformed sample (value is 0 for this product)
8. K = Number of frames per multi-frame module (configurable on this product)
9. HD = High-density mode (the value for this product is 0)
10. F = 8 bits per frame (the value for this product is 2, 4, or 8, depending on the corresponding L value of 4, 2, or 1)
11. C = Control bit (over-range, overflow, under-flow; this feature is not provided in the default mode of this product)
12. T = End bit (This feature is not provided in the default mode of this product)
13. SCR = Scrambler Enable/Disable (configurable on this product)
14. The checksum of the FCHK=JESD204B parameter (automatically calculated and stored in the register map)

Figure 32 shows a simplified block diagram of the JESD204B link of this product. The default configuration of this product uses four converters and one channel. Other configurations are supported, such as combining the outputs of two or four converters into a single channel, allowing data from four converters to be output through two channels. The mapping of the 0, 1, 2, and 3 digital output paths can be changed. These modes can be set via the quick configuration register in the SPI register map, and additional customization options are provided. By default, the 16-bit word of each converter is divided into two 8-bit words (8 data bits). The first 8-bit word includes bits 0 (MSB) to 7, and the second 8-bit word includes bits 8 to 15 (LSB). The two resulting 8-bit words can be scrambled. Scrambling is optional; this option avoids spectral spikes when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by equation $1 + x^{14} + x^{15.}$ The descrambler in the receiver must also use the self-synchronizing version of the scrambler polynomial . The two 8-bit words are then encoded by an 8b/10b encoder. An 8b/10b encoder encodes 8 data bits (one 8-bit word) into a 10-bit symbol. Figure 34 shows how 16-bit data is output from the ADC, how two 8-bit words are scrambled, and how the 8-bit words are encoded into two 10-bit symbols. Figure 34 shows the default data format. At the data link layer, in addition to 8b/10b encoding, character substitution is used so that the receiver can monitor frame alignment. Character substitution occurs at the boundaries between frames and multiframes, and its implementation depends on which boundary the process occurs at and whether scrambling is enabled. If scrambling is disabled, the following measures are taken: If the last scrambled 8-bit word of the last frame in a multiframe is equal to the last 8-bit word of the previous frame, the transmitter replaces the last 8-bit word with the control character /A/=/K28.3/. For other frames in a multiframe , if the last 8-bit word within the frame is equal to the last 8-bit word of the previous frame, the transmitter replaces the last 8-bit word with the control character /F/=/K28.7/. If scrambling is enabled, the following measures are taken: If the last 8-bit word of the last frame in a multiframe is equal to 0x7C, the transmitter replaces the last 8-bit word with the control character /A/=/K28.3/. For other frames in the multiframe , if the last 8-bit word is equal to 0xFC, the transmitter replaces the last 8-bit word with the control character /F/=/K28.7/. For more information on the JESD204B interface, please refer to the JEDEC standard (standard number: JESD204B, July 2011). Section 5.1 contains details on the transport layer and data format; Section 5.2 contains details on scrambling and descrambling.

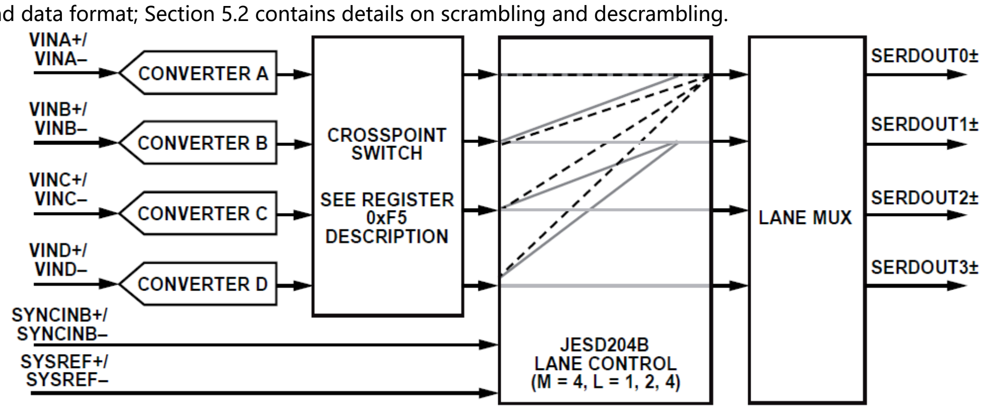

Figure 32. Simplified conceptual block diagram of transmission link

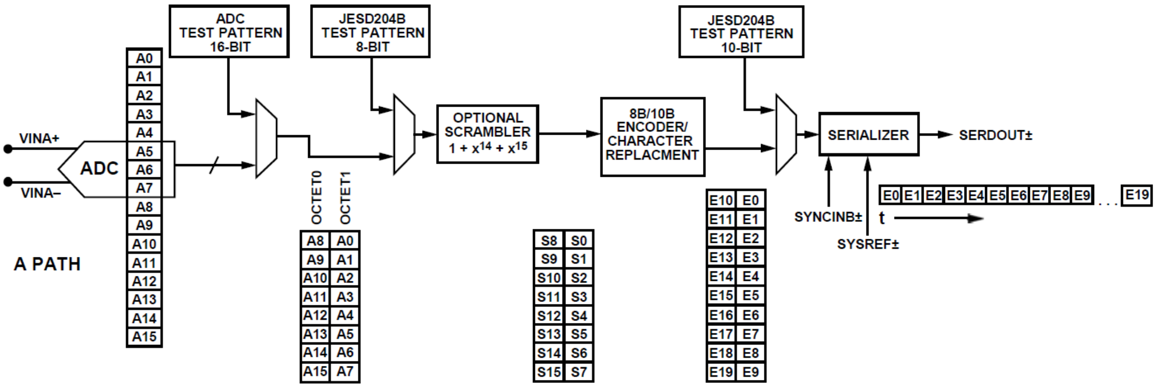

Figure 33. JESD204B tunnel ADC digital processing

JESD204B Synchronization Explained - This product is a JESD204B Subclass 1 device that achieves link synchronization via two control signals (SYSREF and DSYNC). At the system level, multiple conversion devices are aligned using the common DSYSREF and the device clock (CLK). The synchronization process is completed in three phases: Code Group Synchronization (CGS), Initial Channel Alignment Sequence (ILAS), and data transmission. If scrambling is enabled, data bits will not be actually scrambled before the data transmission phase; scrambling is not performed in the CGS and ILAS phases.

CGS Phase - During the CGS phase, the JESD204B's transmit module will transmit the /K28.5/ character. The receiver (external logic device) must use Clock and Data Recovery (CDR) technology to locate the K28.5 character in the input data stream. Once a certain number of consecutive K28.5 characters are detected on the link channel, the receiver generates a DSYSREF edge signal to establish the internal Local Multiframe Clock (LMFC) signal for the product's transmitted data. The DSYSREF edge can also reset any sampling edge of the ADC to synchronize the sampling instance with the LMFC. This is crucial for maintaining synchronization between multiple devices. The receiver or logic device de-sets the SYNC~ signal applied to DSYNC, and the transmitter module begins the ILAS phase.

ILAS Phase - In the ILAS phase, the transmitter sends a known pattern, and the receiver aligns all channel links and verifies the link parameters. After SYNC~ is de-set (goes high), the ILAS phase begins. The transmitting module starts sending four multiframes. Pseudo-samples are inserted into the required characters to transmit the complete multiframes. The four multiframes include:

Multiframe 1: Begins with the character /R/ [K28.0] and ends with the character /A/ [K28.3].

Multiframe 2: Begins with the /R/ character, followed by the /Q/[K28.4] character, then 14 8-bit link configuration parameters (see Table 1), and ends with the /A/ character.

Multi-frame 3: Same as Multi-frame 1.

Multi-frame 4: Same as Multi-frame 1.

Table 1. The 14 Configuration Octets in the ILAS Phase

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS [2:0]			N '[4:0]				
9	JESDV[2:0]			S[4:0]				
10				CF[4:0]				
11	Retained, irrelevant (RES1)							
12	Retained, irrelevant (RES2)							
13	FCHK [7:0]							

Data Transmission Phase - During the data transmission phase, frame alignment is monitored via control characters. Character substitution is performed at the end of the frame . Character substitution is performed on the transmitter under the following conditions:

1. If scrambling is disabled, and the last 8-bit word of one or more frames is equal to the 8-bit word of the previous frame.
2. If scrambling is enabled, and the last 8-bit word of the multiframe is equal to 0x7C, or the last 8-bit word of the frame is equal to 0xFC.

Link Configuration Parameters - The following content demonstrates how to configure the JESD204B interface of this product. The configuration output steps include:

1. Disable the channel before changing the configuration.
2. Choose a quick configuration option.
3. Configure detailed options.
4. Check the JESD204B interface parameter checksum and FCHK.
5. Configure other digital output options.
6. Enable the channel again.

Disable the channel before making any configuration changes. Before changing the link parameters of the JESD204B, disable the link and hold it in the reset register. This can be done by writing a logic 1 to register 0x5F (bit 0).

Select the quick configuration option - write to register 0x5E (JESD204B quick configuration register) to select the configuration option. See Table 2 for the configuration options and their corresponding JESD204B parameter values.

0x41 = 4 converters, 1 channel
0x42 = 4 converters, 2 channels
0x44 = 4 converters, 4 channels
0x21 = 2 converters, 1 channel
0x22 = 2 converters, 2 channels
0x11 = 1 converter, 1 channel

Table 2. Quick Configuration

JESD204B Quick Configuration (register 0x5E)	M(number of converters, register x71, [7:0])	L(number of channels, register 0x6E, [4:0])	F (8-bit word/frame, register 0x6F, [7:0])	S(sample/ADC/ frame, register 0x74, [4:0])	HD (high-density mode, register 0x75, [7])
0x41	4	1	8	1	0
0x42	4	2	4	1	0
0x44	4	4	2	1	0
0x22	2	2	2	1	0
0x21	2	1	4	1	0
0x11	1	1	2	1	0

Configure detailed options - configure end bit and control bit.

1. Since N ' = 16 and N = 14 (non-default configuration), each sample has 2 data bits available for transmitting additional information over the JESD204B link. A stop bit or control bits can be selected. The default stop bit is 0b00.
2. The stop bit is a pseudo-data bit sent over the link to complete the two 8-bit words; it does not convey any information about the input signal. The stop bit can be a fixed value of zero (default) or a pseudo-random number (bit 6 of register 0x5F).
3. One or two control bits can be selected to replace the end bit via bits [7:6] of register 0x72. The meaning of the control bits can be set via bits [7:5] of register 0x14.
4. Set the channel identifier value.
5. The JESD204B supports identifying devices and channels by parameters. These parameters are transmitted during the ILAS phase and can be accessed through internal registers.
6. The three identifier values are Device Identifier (DID), Module Identifier (BID), and Channel Identifier (LID). DID and BID are device-specific identifiers and can therefore be used to identify circuits.
7. Set the number of frames K for each multi-frame.
8. According to the JESD204B specification, a multiframe is defined as a group of K consecutive frames, where K ranges from 1 to 32, and the number of 8-bit words must be between 17 and 1024. Register 0x70 (bits [4:0]) defaults to setting K to 32. Note that K is the register value plus 1.
9. The K value can be changed, but certain conditions must be met. Based on the settings in JESD204B quick configuration, this product uses a fixed 8-bit word value for each frame [F]. K must also be a multiple of 4 and satisfy the following equation: $32 \geq K \geq Ceil(17/F)$
10. The JESD204B specification also specifies the number of 8-bit words per multiframe, i.e., (KxF), ranging from 17 to 1024. The F value is set to a fixed value through quick configuration to ensure that this relationship is true.

Table 3. Configurable Identifier Values for JESD204B

DID value	Register, bit	Range of values
LID (Channel 0)	0x66, [4:0]	0…31
LID (Channel 1)	0x67, [4:0]	0…31
DID	0x64, [7:0]	0…255
BID	0x65, [3:0]	0…15

Scrambling, SCR-

1. Scrambling can be enabled or disabled via bit 7 of register 0x6E. Scrambling is enabled by default. According to the JESD204B protocol, scrambling is only effective after the channel has been synchronized.
2. Select the channel synchronization option.
3. Most JESD204B interface synchronization functions are enabled by default for typical applications. These features can be disabled or changed in certain situations using the following methods:
4. Register 0x5F (bits [3:2]) enables ILAS, which is enabled by default. Additionally, to support certain specific interfaces (such as NMCDA-SL), the JESD204B interface can be programmed to disable ILAS sequences or allow continuous repeating ILAS sequences.
5. This product has some fixed JESD204B interface parameter values, as follows:

[N ']=16: The number of bits per sample is 16 (register 0x73, bits [4:0]).

[CF]=0: Control word/frame clock cycle/converter number is 0 (register 0x75, bits [4:0])

6. Verify the read-only values: number of channels per link (L), number of 8-bit words per frame (F), number of converters (M), and number of samples per converter per frame (S). This product calculates certain JESD204B parameter values based on other settings, particularly the options for the fast configuration register. The following read-only values in the register map are used for verification.
7. [L] = The number of channels per link can be 1, 2, or 4, and this value is read from register 0x6E (bits [4:0]).
8. [F] = The number of 8-bit words per frame can be 2, 4, or 8, from register 0x6F (bit 1).
9. [7:0]) Read this value
10. [HD] = High-density mode is 0, read from register 0x75 (bit 7).
11. [M] = Number of converters per link, defaults to 4, but can be 1, 2 or 4; read from register 0x71 (bits [7:0]).
12. [S] = 1 sample per converter per frame; this value is read from address 0x74 (bits [4:0]).

Checking the JESD204B interface parameter checksum FCHK - JESD204B parameters can be verified through the JESD204B interface parameter checksum [FCHK]. Each link has its own corresponding FCHK value. The FCHK value is transmitted in the second multiframe of ILAS and can be read through internal registers. The checksum is the modulo 256 sum of the parameters listed in the "Number" column of Table 4. The checksum is calculated by adding the parameters before they are encapsulated into 8-bit words as shown in Table 4. The FCHK for channel configuration when outputting data from channel 0 can be read from register 0x78. Similarly, the FCHK for channel configuration when outputting data from channel 1 can be read from register 0x79, the FCHK for channel configuration when outputting data from channel 2 can be read from register 0x7A, and the FCHK for channel configuration when outputting data from channel 3 can be read from register 0x7B.

Table 4. JESD204B Configuration Table for ILAS and Checksum Calculation

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS [2:0]			N '[4:0]				
9	JESDV[2:0]			S[4:0]				
1 0				CF[4:0]				

Configure other digital output options - other data format controls include:

1. Serial output data polarity inversion: bit 1 of register 0x60
2. ADC data format (offset binary or two's complement): bits [1:0] of register 0x14
3. Deciphering the options for signals on DSYSREF and DSYNC: Bits [4:3] of register 0x3A
4. Remapping converters (logical channels) and SERDOUTx ± (physical channels) allocation: registers 0x82 and 0x83. Figure 33 shows a simplified functional block diagram.

Configure and then enable the channel - After changing the JESD204B link parameters, the link channel should be enabled to begin synchronization. This can be done by writing a logic 0 to register 0x5F (bit 0).

Frame and Channel Alignment Monitoring and Correction – Frame alignment monitoring and correction are both part of the JESD204B specification. A 16-bit word requires two 8-bit words to transmit all data. Two 8-bit words (MSB and LSB, F=2) constitute a frame. Under normal operating conditions, frame alignment is monitored by arranging characters; under certain conditions, characters can be inserted at the end of a frame. Table 5 summarizes the conditions for character insertion and the expected characters in various operating modes. If channel synchronization is enabled, the replacement character value depends on whether the 8-bit word is at the end of a single frame or multiple frames. By correctly receiving the replacement character, the receiver can ensure synchronization with frame boundaries in different operating modes.

Table 5. Frame and Channel Arrangement Monitoring and Correction Replacement Character Table

Scrambling	Channel synchronization	Characters to be replaced	Whether it is the last 8 characters in multiple frames	Replacement character
Close	Open	The last 8 characters repeat the content of the previous frame.	No	K28.7
Close	Open	The last 8 characters repeat the content of the previous frame.	Yes	K28.3
Close	Close	The last 8 characters repeat the content of the previous frame.	N/A	K28.7
Open	Open	The last 8 bits equal D28.7	No	K28.7
Open	Open	The last 8 bits equal D28.3	Yes	K28.3
Open	Close	The last 8 bits equal D28.7	N/A	K28.7

Digital Outputs and Timing - This product features differential digital outputs by default upon power-up. Driver current is derived from the chip, setting the output current at each terminal to the nominal value of 4mA. Each output has a 100K dynamic internal termination resistor to reduce reflection interference. Placing a 100K differential termination resistor at the input of each receiver enables a nominal 600mVp-p receiver differential swing (see Figure 33). A single-ended 50K termination resistor can also be used. When using a single-ended termination resistor, the termination voltage must be DRVDD/2; additionally, AC coupling capacitors terminated to any single-ended voltage can be used.

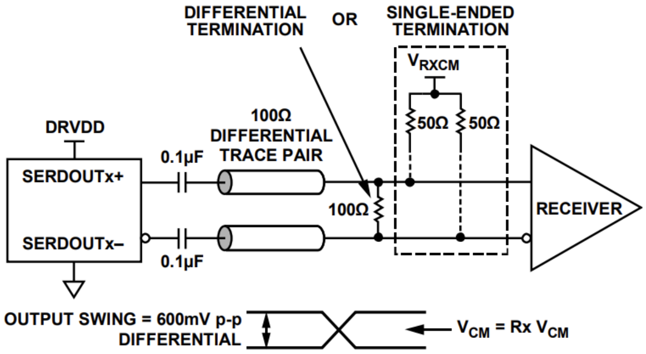

Figure 33. Example of AC - coupled digital output termination

This product's digital outputs interface with custom ASIC and FPGA receivers, enabling excellent switching performance in high-noise environments. A single point-to-point network topology is recommended, with the single 100K differential termination resistor placed as close to the receiver as possible. If a DC-coupled connection is used (as shown in Figure 34), the common-mode digital output will automatically bias itself to the middle of the receiver's power supply (i.e., 0.9V common-mode voltage when the receiver power supply is 1.8V). For receivers with logic levels outside the DRVDD power supply boundary, an AC-coupled connection should be used. Place a 0.1µF capacitor on each output pin and use a 100K differential termination resistor close to the receiver.

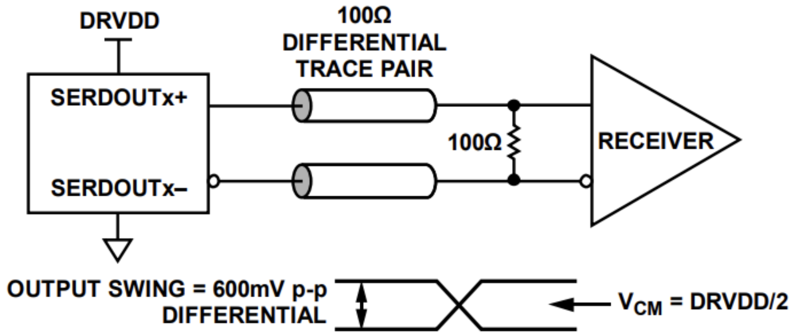

Figure 34. Example of DC-coupled digital output terminal connection

The absence of remote receiver termination resistors or poor differential trace routing can lead to timing errors. To avoid timing errors, it is recommended that trace lengths not exceed 6 inches, and differential output traces be kept as close to each other as possible and of equal length. Figure 35 shows an example of the digital output data eye diagram, time interval error (TIE) jitter histogram, and bathtub curve when the product channel is operating at 6.4Gbps. An additional SPI option allows users to further increase the output driver voltage swing of all four outputs, thereby driving longer traces. Using this option will increase the power consumption of the DRVDD power supply. See the Memory Mapping section for more information. The output data format is two's complement by default. To change the output data format to offset binary, see the Memory Mapping section and Register 0x14 in Table 16.

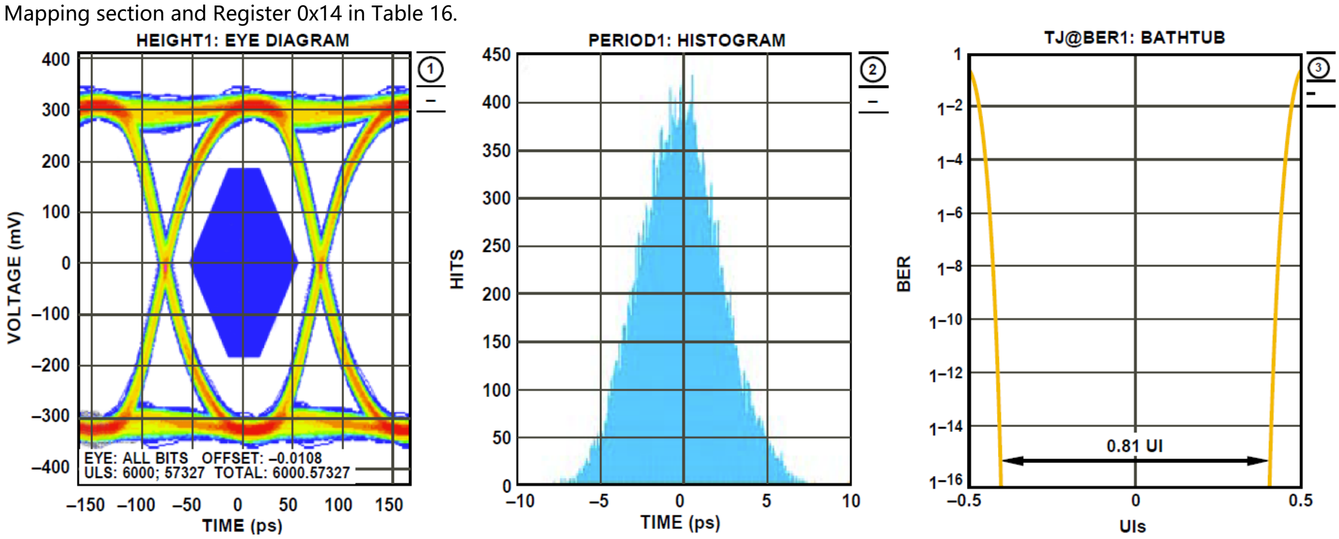

Figure 35. The digital output data eye diagram, histogram and bathtub graph of this product
(with an external termination resistor of 100K at 6.4 Gbps)

17. Memory Mapping

- **Read the memory-mapped register table**

Each row of the memory-mapped register table has 8 bits. The memory map is roughly divided into three parts: chip configuration registers (addresses 0x00 to 0x02), channel index and transfer registers (addresses 0x05 and 0xFF), and ADC function registers, including setup, control, and test registers (addresses 0x08 to 0x10A). The memory-mapped register table (see Table 6) records each hexadecimal address and its hexadecimal default value. The 7th bit (MSB) column is the starting bit of the given hexadecimal default value. For example, the hexadecimal default value for the output mode register (address 0x14) is 0x01. This indicates that bit 0 = 1, and the remaining bits are 0. This setting is the default output format value (two's complement).

- **Disabled and reserved locations**

This device does not support all addresses and bits not included in Table 6. Unused bits at valid address locations should be written with 0. Write operations can only be performed on these locations if only some bits of the address (e.g., address 0x18) are disabled. If the entire address (e.g., address 0x13) is disabled, no write operations should be performed on that address.

- **Default value**

After this product is reset, the critical registers will be loaded with their default values. The memory-image register table (see Table 6) lists the default values for each register.

- **Logic Level**

The following is a definition of logic levels:

1. "Setting" means "set a bit to logic 1" or "write logic 1 to a bit".
2. "Clear bit" means "set a bit to logic 0" or "write a bit to logic 0".

- **Specific channel register**

Different values can be set for certain functions of each channel through programming. In these cases, the channel address location can be copied internally for each channel. These registers and their corresponding bits are referred to as local registers in Table 6. These local registers and their corresponding bits can be accessed by setting the channel 0, channel 1, channel 2, or channel 3 bit in register 0x05. If all four bits are set, subsequent write operations will affect the registers of all four channels. In a read cycle, only one channel is set, and a read operation is performed on one of the four registers. If all bits are set in an SPI read cycle, the device returns the value of channel 0. The global registers and their corresponding bits given in Table 6 affect the characteristics of the entire device and channels, and individual settings for each channel are not allowed. Settings in register 0x05 do not affect the values of the global registers and their corresponding bits.

- **Memory Mapped Register Table**

This product uses a 3-wire interface and 16-bit addressing. Bits 0 and 7 of register 0x00 are set to 0, and bits 3 and 4 are set to 1. When bit 5 of register 0x00 is set to 1, SPI enters a soft reset, all user registers are restored to their default values, and bit 2 is automatically cleared to 0.

Table 6. Memory -mapped registers (SPI registers/bits not marked as "local" are "global" registers/bits)

Address	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default value	Remark
Chip configuration register											
0x00	SPI port configuration	0	LSB priority	Soft reset	1	1	Soft reset	LSB priority	0	0x18	
0x01	Chip ID	8-bit chip ID [7:0]; This product = 0xC0 (quad-channel, 16-bit, 125 MSPS, JESD204B)								0xC0	Read-only
0x02	Chip level	Disable	Speed Class ID [6:4]; 110 = 125 MSPS			Disable	Disable	Disable	Disable	0x60	Read-only
Channel Index and Transfer Register											
0x05	Device Index	Disable	Disable	Disable	Disable	Data Channel 3	Data Channel 2	Data Channel 1	Data Channel 0	0x0F	
0xFF	Transmission	Disable	Disable	Disable	Disable	Disable	Disable	Disable	Overwrite (self-clear) the boot register 0x100.	0x00	
ADC function											
0x08	Power consumption mode	Disable	Disable	PDWN pin function: 0 = Complete	JTX Standby Mode: 0 = Ignore	Reserve		Power consumption mode: 00 = Normal operation		0x00	

				power down, 1 = Standby	standby , 1 = Do not ignore standby			01 = Complete power outage 10 = Standby 11 = Digital Reset			
0x09	Clock	Disable	0	Disable	Disable	Disable	Disable	Disable	Duty cycle stabilizer: 0 = Off 1 = Open	0x00	
0x0A	PLL_STATUS	PLL lock status bit: 0 = PLL not locked 1 = PLL Lock	Disable	Disable	Disable	Disable	Disable	Disable	JTX link state: 0 = Not ready 1 = Ready		Read-only
0x0B	Clock divider	Disable	Disable	Disable	Disable	Disable	Clock division ratio [2:0]: 000 = 1 divider, 001 = 2 dividers , 010 = 3 dividers, 011 = 4 dividers, 100 = 5 dividers, 101 = 6 dividers, 110 = 7 dividers, 111 = 8 divider			0x00	
0x0C	Enhanced control	Disable	Disable	Disable	Disable	Disable	Chopper Mode 0 = Off, 1 = On	Disable	Disable	0x00	
0x0D	Test mode (Local, Pseudo-random number (PN)) (Except for sequence reset)	User input test mode: 00 = Single 01 = Alternate 10 = Single time 11 = alternating once (Only affects user input test pattern [3:0]=1000)		Reset PN length Sequence generator	Reset PN length Sequence generator	Output test mode [3:0] (local): 0000 = Off (Default) 0001 = Short intermediate level 0010 = Full Scale (FS) 0011 = Negative FS 0100 = Alternating chessboard pattern 0101=PN23 sequence 0110 = PN9 sequence 0111 = 1/0 (reversed) 1000 = User input 1001 = 1/0 bit reversal 1010 = 1 × Synchronization 1011 = 1 high level 1100 = Mixed bit frequency				0x00	When set to 1, test data will be placed on the output pin instead of normal data.
0x10	Disorder adjustment (Partial)	8-bit device offset adjustment [7:0] (local); offset adjustment in LSB units, from +127 to -128 (two's complement format).								0x00	Device offset adjustment
0x14	Output mode	JTXCS mode: 000 = {Over-range||Under-range, Valid Flag} 001 = {Over-range, Under-range} 010 = {Overrange||Underrange, empty} 011 = {empty, valid flag} 100={empty, empty} Other = {Overrange||Underrange, Valid Flag}			ADC output Valid mark: 0 = Output valid 1 = Invalid output (partial)	Disable	Disable	Output format: 0 = offset binary 1 = two's complement		0x01	
0x15	Output adjustment	Disable	Disable	Disable	Disable	Disable	Typical CML differential output drive level: 000 = 473mVp-p			0x03	

							001=524mVp-p 010 = 574mVp-p 011 = 621mVp-p (default) 100 = 667mVp-p 101=716mVp-p 110 = 763mVp-p 111=811mVp-p				
0x16	Clock phase control	Disable	Input clock phase adjustment [2:0] (Value is the number of input clock cycles with phase delay)			Disable	Disable	Disable	Disable	0x00	
0x18	Input range selection	Internal VREF adjustment [1:0]: 00 = 1.0V 01 = 1.2V 10 = 1.3V 11 = 1.4V		Disable	Disable	Disable	Differential range adjustment: 000 = 50% of normal value 001 = 57% of normal value 010 = 67% of normal value 011 = 80% of normal value 100 = Normal value			0x04	
0x19	User test code 1LSB	User test code 1 [7:0]								0x00	
0x1A	User test code 1MSB	User test code 1 [15:8]								0x00	
0x1B	User test code 2LSB	User test code 2 [7:0]								0x00	
0x1C	User test code 2MSB	User test code 2 [15:8]								0x00	
0x21	FLEX_ SERIAL_ CONTROL	Disable	Disable	Disable	Disable	PLL low-rate mode: 0 = Channel speed Rate ≥ 2Gbps 1 = Channel speed Rate < 2Gbps	Disable	Disable	Disable	0x00	
0x22	FLEX_ SERIAL_ CH_STAT	Disable	Disable	Disable	Disable	Disable	Disable	Disable	Channel power failure (Partial)	0x00	
0x3A	SYSREF_ CTRL	Disable	Disable	Disable	0 = Normal Mode 1 = Each activation DSYNC± Realign channels	0 = only when SYSREF ± Realign channels when counter resynchronization is triggered 1 = per DSYNC± Upper Realign Channel	Disable	Disable	Disable	0x00	
0x3B	REALIGN_ PATTERN_ CTRL	When aligning a channel, write this mode code into the FIFO: 00 = channel output all 0s; 55 = channel output alternating mode code.								0x55	

www.dsown.com
Email：info@dsown.com

0x5E	JESD204B Quick Configuration	0x41 = 4 converters, 1 channel; 0x42 = 4 converters, 2 channels; 0x44 = 4 converters, 4 channels 0x22 = 2 converters, 2 channels; 0x21 = 2 converters, 1 channel; 0x11 = 1 converter, 1 channel								0x00	Self-clearing, always reads 0x00.
0x5F	JESD204B Link Control 1	Disable	End bit pattern: 0 = fill with 0 1 = Fill 9 PN sequence	JTX Transmission Layer testing: 0 = Not enabled 1 = Long transport layer test Enable	Multi-frame aligned character insertion: 0 = Disabled 1 = Enable	ILAS mode: 00 = ILAS disabled 01 = ILAS Enabled (Normal Mode) 11 = ILAS is always enabled (test mode)		Frame - aligned words Symbol Insertion: 0 = Enable 1 = Disabled	0=JTX link enabled 1=JTX link disabled	0x14	
0x60	JESD204B Link Control 2	Reserve		DSYNC± Pin reversal: 0 = No reversal 1 = Reverse	DSYNC± Foot input bias: 0 = Disabled 1 = Enable	Disable	Disable	JTX output Reversal: 0 = Normal 1 = Reverse	Reserve	0x10	
0x61	JESD204B Link Control 3	Reserve	Reserve	Test data injection point: 01=8b/10b encoder Inject 10 bits of data during output. 10 = 8 bits of data when scrambling input		JTX Test Mode Code: 0000 = Normal operation (Test mode disabled) 0001 = Alternating chessboard pattern 0010 = 1/0 alternation 0011=PN sequence is PN23 0100=PN sequence is PN9 0101 = Continuous/Repeated User Testing Mode 0110 = Single-user test mode 0111 = Reserved 1000 = Modified RPAT test sequence (8 bits of data only) 1100=PN sequence is PN7 1101=PN sequence is PN15 Other settings are not used.				0x00	
0x62	JESD204B Link Control 4	Reserve								0x00	
0x64	JESD204B DID Configuration	Device Identifier (DID) = C0								0xC0	Read-only
0x65	JESD204B BID Configuration	Disable	Disable	Disable	Disable	JTX Module Identifier (BID)				0x00	
0x66	JESD204B LID Configuration 0	Disable	Disable	Disable	JTX Channel Identifier (LID) Number for Channel 0					0x00	

Address	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default value	Remark
0x67	JESD204B LID Configuration 1	Disable	Disable	Disable	JTX Channel Identifier (LID) Number of Channel 1					0x01	
0x68	JESD204B LID Configuration 2	Disable	Disable	Disable	JTX Channel Identifier (LID) Number of Channel 1					0x02	
0x69	JESD204B LID Configuration 3	Disable	Disable	Disable	Channel 3 JTX Channel Identifier (LID)					0x03	
0x6E	JESD204B Parameter SCR/L	JESD204B Scrambling (SCR) : 0 = Disabled 1 = Enable	Disable	Disable	JESD204B Serial Channel Control: 0 = 1 channel per link (L=1) 1 = 2 channels per link (L=2) 2 = Not used 3 = 4 channels per link (L=4) 4 to 31 = Unused					0x80	
0x6F	JESD204B parameter F	The number of 8-bit words per frame in JESD204B (F); calculated value, F=(2×M)/L								0x00	Read-only
0x70	JESD204B parameter K	Disable	Disable	Disable	Number of frames (K) per multiframe in JESD204B; K = register content + 1, and K must be a multiple of 48-bit words.					0x1F	
0x71	JESD204B parameter M	JESD204B converter count (M): 0 = 1 converter (M=1), 1 = 2 converters (M=2), 3 = 4 converters (M=4, default value)								0x03	
0x72	JESD204B Parameters CS/N	00 = 0 samples sent per sample Control bits (CS=0)		Disable	JTX converter resolution (N): 0x0F = 16 bits 0x0D = 14 bits 0x0B = 12 bits 0x09 = 10 bits					0x0F	
0x73	JESD204B parameter subclass/Np	JESD204B subclasses: 0x0 = subclass 0 0x1 = Subclass 1 (default)			The number of bits per sample in JESD204B (N '); N ' = register content + 1					0x2F	
0x74	JESD204B Parameter S	Reserve			JESD204B converter sample count per frame (S); S = register content + 1					0x20	Read-only
0x75	JESD204B Parameters HD and CF	JESD204B HD value = 0	Disable	Disable	Frame clock cycle on each link.					0x00	Read-only
0x76	JESD204B RESV1	The JESD204B serial reserved field 1 in the link configuration is shown in Table 1 (RES1).								0x00	
0x77	JESD204B RESV2	JESD204B serial reserved field 2 in the link configuration, see Table 1 (RES2).								0x00	
0x78	JESD204B CHKSUM0	For the JESD204B serial checksum value in the link configuration, please refer to Channel 0 (FCHK) in Table 1.									Read-only
0x79	JESD204B CHKSUM1	For the JESD204B serial checksum values in the link configuration, please refer to Channel 1 (FCHK) in Table 1.									Read-only
0x7A	JESD204B CHKSUM2	For the JESD204B serial checksum values in the link configuration, please refer to Channel 2 (FCHK) in Table 1.									Read-only
0x7B	JESD204B CHKSUM3	For the JESD204B serial checksum values in the link configuration, please refer to Channel 3 (FCHK) in Table 1.									Read-only
0x80	JTX physical channel disabled	Disable	Disable	Disable	Disable	Channel 3: 0 = Enable 1 = Disabled	Channel 2: 0 = Enable 1 = Disabled	Channel 1: 0 = Enable 1 =	Channel 0: 0 = Enable 1 =	0x00	Channel serializa-tion, output driver off

								Disabled	Disabled		
0x82	JESD204B Channel Alignment 1	Disable	Physical Channel 1 Alignment: 000 = Logical Channel 0 001 = Logical Channel 1 010 = Logical Channel 2 011 = Logical Channel 3				Physical channel 0 alignment: 000 = Logical Channel 0 001 = Logical Channel 1 010 = Logical Channel 2 011 = Logical Channel 3			0x10	
0x82	JESD204B Channel Alignment 1	Disable	Physical Channel 1 Alignment: 000 = Logical Channel 0 001 = Logical Channel 1 010 = Logical Channel 2 011 = Logical Channel 3			Disable	Physical channel 0 alignment: 000 = Logical Channel 0 001 = Logical Channel 1 010 = Logical Channel 2 011 = Logical Channel 3			0x10	
0x83	JESD204B Channel Alignment 2	Disable	Physical Channel 3 Alignment: 000 = Logical Channel 0 001 = Logical Channel 1 010 = Logical Channel 2 011 = Logical Channel 3			Disable	Physical Channel 2 Alignment: 000 = Logical Channel 0 001 = Logical Channel 1 010 = Logical Channel 2 011 = Logical Channel 3			0x32	
0x86	JESD204B Channel Reversal	Disable	Disable	Disable	Disable	Channel 3: 0 = No reversal 1 = Reverse	Channel 2: 0 = No reversal 1 = Reverse	Channel 1 : 0 = No reversal 1 = Reverse	Channel 0 : 0 = No reversal 1 = Reverse	0x00	
0x8B	JESD204B LMFC offset	Disable	Disable	Disable	Local Multi-Frame Clock (LMFC) phase offset value; LMFC when DSYSREF is set The reset value of the phase counter; used for deterministic delay applications.					0x00	
0xA0	JTX User Mode 8 -bit byte 0, LSB	The least significant byte of the user test code is an 8-bit word 0								0x00	
0xA1	JTX User Mode 8 -bit byte 0, MSB	Significant byte in the user test code is an 8-bit word 0								0x00	
0xA2	JTX User Mode 8 -bit byte 1, LSB	User test code: minimum valid byte, 8-bit word								0x00	
0xA3	JTX User Mode 8 -bit byte 1, MSB	The user test code, 8 bits								0x00	
0xA4	JTX User Mode 8 -bit byte 2, LSB	User test code minimum valid bytes, 8-bit word 2								0x00	
0xA5	JTX User Mode 8 -bit byte 2, MSB	The user test code, 8 bits								0x00	
0xA6	JTX User Mode 8 -bit byte 3, LSB	User test code minimum valid bytes, 8-bit word 3								0x00	
0xA7	JTX User Mode 8 -bit byte 3, MSB	The user test code, 8 bits								0x00	
0xF5	JTX converter Mapping	JTX Converter 3: 0=ADCA		JTX Converter 2: 0=ADCA		JTX Converter 1: 0=ADCA		JTX converter 0: 0=ADCA		0xE4	

		1=ADCB 2=ADCC 3=ADCD		1=ADCB 2=ADCC 3=ADCD		1=ADCB 2=ADCC 3=ADCD		1=ADCB 2=ADCC 3=ADCD			
0x100	Resolution/sampling rate coverage	Disable	Coverage Enable	Resolution 0=16 bits 1=14 bits 2=12 bits 3= 10 bits	Disable	Sampling rate: 001 = 40 MSPS 010 = 50 MSPS 011 = 65 MSPS 100 = 80 MSPS 101 = 105 MSPS 110 = 125 MSPS				0x00	Sampling rate coverage (requires transfer register 0xFF)
0x101	User I/O Control 2	Disable	Disable	Disable	Disable	Disable	Disable	Disable	SDIO pulldown	0x00	Disable SDIO pull-down resistors
0x102	User I/O Control 3	Disable	Disable	Disable	Disable	VCM power failure	Disable	Disable	Disable	0x00	VCM control
0x109	Clock divider Synchronization control	Clock divider synchroni-zation mode: 0 = using the SYNC pin; 1 = using the DSYSREF± pin.	reserve					Received reset Clock division Device Synchron-izer	Synchron-ous clock divider enable: 0= Disabled 1 = Enable	0x00	
0x10A	Received clock Frequency divider synchronization	Disable	Disable	Disable	Disable	Disable	Disable	Disable	Received clock minutes Frequency converter synchron-ization	0x00	Read-only

- **Device Index (Register 0x05)**

For certain characteristics specified as local in the mapping, each channel can be set independently, while other characteristics are globally applicable (depending on the context), regardless of which channel is selected. Bits [3:0] of register 0x05 can be used to select which data channels are affected.

- **Transfer (register 0xFF)**

Except for register 0x100, all other registers are updated immediately upon being written. When bit 0 of the transfer register is set to 1, the resolution/sampling rate override register (address 0x100) is initialized.

- **Power consumption mode (register 0x08)**

1. Bit 5—PDWN pin function
   When set to 1, the PDWN pin enters standby mode. When set to 0 (cleared), the PDWN pin enters full power-down mode.
2. Bit 4—JTX Standby Mode
   When set to 1, if the chip's standby function is enabled, the JTX module enters standby mode. In standby mode, only the PLL continues to operate. When cleared to 0, if the chip's standby function is enabled, the JTX module continues to operate.
3. Bits [1:0] — Power consumption mode
   When operating normally (bits [1:0]=00), all ADC channels and JTX modules are enabled.
   In full power-down mode (bits [1:0]=01), all ADC channels and JTX modules are powered down, the digital data path clock is disabled,

and the digital data path is reset. Outputs are disabled.

In standby mode (bits [1:0]=10), all ADC channels are partially powered down, and the digital data path clock is disabled. If JTX standby mode is set, the outputs are also disabled.

During a digital reset (bits [1:0]=11), all other digital data path clocks and outputs (where applicable) of the chip, except for the SPI port, are reset. Note that the SPI is always under user control and is never automatically disabled or reset (unless powered on). If the digital reset is ineffective, a foreground calibration sequence is initiated.

- **Enhanced control (register 0x0C)**

1. Position 2 - Chopper Mode

   Some applications are sensitive to offset voltage and other low-frequency noise, such as null-difference or direct-conversion receivers. For these applications, bit 2 can be set to enable the chopping characteristics of the first stage of this product. In the frequency domain, chopping converts offset and other low-frequency noise into $f_{CLK}/2$, which can be filtered out by a filter.

- **Output mode (register 0x14)**

1. Bit [7:5] — JTX CS mode

Specify the meaning of the JTX control bit.

2. Bits [1:0] — Output Format

By default, this field is set to 1, and the data is output in two's complement format. When this field is cleared to 0, the output mode changes to offset binary.

- **Clock phase control (register 0x16)**

1. Bit [6:4] — Input clock phase adjustment

When using the clock driver (register 0x0B), the applied clock frequency is higher than the internal sampling clock. Bits [6:4] determine which phase of the external clock is sampled on. This only applies when using a clock divider. Bits [6:4] cannot be set to values greater than bits [2:0] of register 0x0B.

- **JTX User Mode Code (Registers 0xA0 to 0xA7)**

When bits [3:0] of register 0x61 are set to 5 or 6, the pattern codes in these registers are output on all valid channels. When bits [5:4] of register 0x61 are set to 2, a 32-bit pattern code consisting of registers 0xA0, 0xA2, 0xA4, and 0xA6 is inserted before the scrambler. When bits [5:4] of register 0x61 are set to 1 (40-bit pattern code), a pattern code consisting of the following is inserted before the 8b10b encoder: bits [1:0] of register 0xA1 and bits [7:0] of register 0xA0; bits [1:0] of register 0xA3 and bits [7:0] of register 0xA2; bits [1:0] of register 0xA5 and bits [7:0] of register 0xA4; bits [1:0] of register 0xA7 and bits [7:0] of register 0xA6.

- **Resolution/sampling rate coverage (register 0x100)**

In applications where the highest resolution and/or sampling rate is not required, users can use this register to reduce the resolution and/or maximum sampling rate (in order to reduce power consumption). This register is initialized after bit 0 of the transfer register (register 0xFF) is written high.

Bits [2:0] do not affect the sampling rate, but rather the maximum sampling rate of the ADC.

User I/O control 2 (register 0x101)

1. Bit 0 - SDIO pull-down

   Bit 0 can be set to disable the built-in 30kK pull-down resistor on the SDIO pin. This setting can be used to limit the load when many devices are connected to the SPI bus.

User I/O control 3 (register 0x102)

1. Position 3—VCM power failure

   The internal VCM generator can be turned off by setting bit 3 high. Use this function when using an external reference voltage source.

18. Application Information

- **Design Guidelines**

Before performing system-level design and layout for this product, designers are advised to familiarize themselves with the following design guidelines, which discuss the special circuit connections and layout routing requirements for certain pins.

- **Power supply and grounding recommendations**

When connecting power to this product, it is recommended to use two separate 1.8V power supplies: one for analog outputs (AVDD) and the other for digital outputs (DRVDD and DVDD). Designers can use several different decoupling capacitors to suit both high and low frequencies. Decoupling capacitors should be placed close to the PCB entry point and near the device pins, with trace lengths kept as short as possible.
This product requires only one PCB ground plane. Optimal performance can be easily achieved by properly decoupling and cleverly separating the PCB analog, digital, and clock modules.

- **Clock stability considerations**

Upon power-up, this product enters the initial phase, and the internal state machine sets the bias and registers to ensure proper operation. A stable clock is required during initialization. If the ADC clock source is absent or unstable during ADC power-up, the state machine will be interrupted, leading to an unknown state. To correct this, the initial sequence must be called back after the ADC clock stabilizes. This can be accomplished by initiating a digital reset via register 0x08. In the default configuration (internal V_{REF}, AC-coupled input), V_{REF} and V_{CM} are provided by the ADC itself, thus providing a sufficiently stable clock upon power-up. When V_{REF} and /or V_{CM} are provided by an external source, they must also be stable upon power-up; otherwise, a digital reset via register 0x08 is required. The pseudocode sequence for the digital reset is shown below:

```
SPI_Write (0x08, 0x03); # Digital Reset
SPI_Write (0x08, 0x00); # Normal Operation
```

- **Recommendations for exposed pad heat sinks**

To achieve optimal electrical and thermal performance, the exposed pads on the bottom of the ADC must be connected to analog ground (AGND). The exposed (without solder mask) continuous copper plane on the PCB must match the exposed pads (pin 0) of this product. Multiple vias must be present on the copper plane to provide the lowest possible thermal resistance path for heat dissipation through the bottom of the PCB. These vias should be filled or sealed with insulating epoxy. To maximize coverage and connection between the ADC and the PCB, a silkscreen layer should be applied to the PCB to divide the continuous plane into multiple equal sections. This prevents solder buildup during reflow soldering and provides multiple connection points between the ADC and the PCB. A continuous, undivided plane would only guarantee one connection point between the ADC and the PCB.

- **VCM**

Use a 0.1μF capacitor to decouple the VCM pin to ground.

- **Reference voltage source decoupling**

The VREF pin should be decoupled to ground through a parallel connection of an external low-ESR 0.1μF ceramic capacitor and a low-ESR 1.0μF capacitor.

- **SPI port**

The SPI port should be disabled when the converter needs to fully utilize its dynamic performance. Typically, the SCLK, CSB, and SDIO signals are asynchronous with the ADC clock; therefore, noise in these signals can degrade converter performance. If other devices use the on-board SPI bus, a buffer may be needed between that bus and this product to prevent these signals from changing at the converter's input pins during critical sampling periods.

19. Precautions

- **Product installation precautions:**

1. The application circuit board must have a clean and intact ground plane.
2. The application must be a multi-layer cabling board containing an independent ground plane.
3. The digital ground and analog ground of the application circuit board should be separated as much as possible, and digital lines should not be routed next to analog lines or under the ADC.
4. VCC, VDD, and CL should be connected to high-quality ceramic bypass capacitors, and the bypass capacitors should be as close to the pins as possible. The connection between the pins and the bypass capacitors should be as short and wide as possible.
5. It is recommended to reset the circuit after power-on before use. For reset methods, see "Reset Operation and Clock Stability Considerations" and operate on register 0x08.

- **Product usage precautions:**

1. Differential inputs should be as close as possible to each other and parallel to each other.
2. Input connections should be kept as short as possible to minimize parasitic capacitance and noise introduction.
3. To achieve better heat dissipation and electrical performance, the chip's baseplate should be soldered to a large ground terminal on the PCB board to maximize the thermal performance of the package.
4. It is important that the chip's ground plane be connected to the PCB's ground plane through as many channels as possible and with a sufficient area.

- **Product protection precautions:**

1. Electrostatic charges can easily accumulate on the human body and testing equipment and may discharge imperceptibly. Although this product has dedicated ESD protection circuitry, permanent device damage may occur upon exposure to high-energy electrostatic discharges. Therefore, appropriate ESD precautions are recommended to avoid device performance degradation or malfunction.
2. Exceeding the absolute maximum ratings may result in permanent damage to the device. These are only the maximum ratings and do not indicate that the device will function properly under these conditions or under any other conditions beyond those shown in this datasheet. Prolonged operation at the absolute maximum ratings will affect the reliability of the device.
3. Plastic-encapsulated circuits are prone to moisture absorption, which can lead to delamination. When using them, care should be taken to keep the surrounding environment dry. When storing them, they should be vacuum-packed and stored in a dry environment at room temperature.

- **Denso requirements**

1. This product has a moisture sensitivity rating of MSL3. The permissible time for the product to be exposed to the external environment after being removed from the moisture-proof bag, dried, or baked, until reflow soldering is: ≤30℃/60RH%, 168h.
2. If the storage conditions of the device cannot be controlled or traced, please strictly follow the baking process of 125℃ for 8 hours before electrical assembly.
3. If the ambient temperature and humidity of the electrical installation environment cannot be guaranteed to be ≤30℃/60RH%, please complete the soldering within 12 hours after baking.
4. After the product is baked, it is very easy to generate static electricity, so ESD protection should be taken into account during all operations.
5. When using leaded reflow soldering (Sn63Pb37) for board-level assembly, the recommended peak temperature range is 210℃~220℃, and the maximum peak temperature should not exceed 235℃. The dwell time within ±5℃ of the peak temperature should be ≤20s, and the dwell time above the liquidus line should be 60~90s. The heating rate is 2~4℃/s, and the cooling rate is ≤2℃~6℃.
6. When using lead-free reflow soldering (SAC305) for board-level assembly, the recommended peak temperature range is 230℃~245℃, and the maximum peak temperature should not exceed 260℃. The dwell time within ±5℃ of the peak temperature should be ≤20s, and the dwell time above the liquidus line should be 60~90s. The heating rate should be 2~4℃/s, and the cooling rate should be ≤2℃~6℃.
7. If the hybrid assembly process requires increased temperature, the device body temperature should be ensured not to exceed 260°C. (The device body temperature measurement point is located on the upper surface of the device during reflow soldering .)
8. The solder joints of this product are plated with tin.

- **Common Faults and Troubleshooting**

1. No signal output: Check if the power supply voltage, input signal, and clock are correctly applied.
2. An overflow signal occurs: Check if the reference is working properly and if the input signal amplitude is correct.
3. Device malfunction: Check the power supply and ensure the power supply voltage is stable.

www.dsown.com
Email：info@dsown.com

20. Package Information

External dimensions

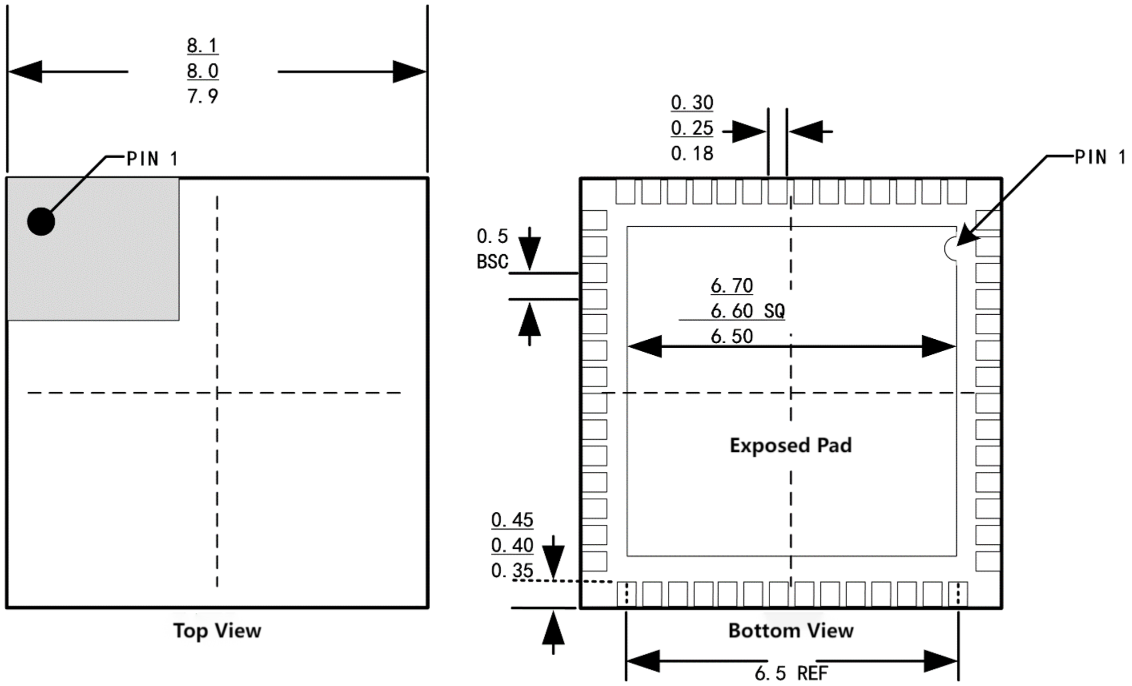

Figure 36. QFN56 package dimensions

21. Ordering Guide

Model	Temperature range	Package Type	Package Quantity
ADCP9656-125	-40 °C to +85°C	QFN56	260/Reel