ADCP9434-500, 12-Bit, 500MSPS, High-Speed ADC

1. Features

- Resolution: 12-bit
- Sampling rate: 500 MSPS
- SFDR: > 65dBFS
- Variable input range 1.18Vp-p to 1.6Vp-p
- PIN compatible with AD9434 series
- Circuit interface: LVDS
- Operating temperature range: -40℃ to +85℃
- QFN56 package

2. Applications

- Wireless and broadband communications
- Receiver
- Communication testing equipment
- Radar and satellite subsystems
- Linearization of power amplifiers

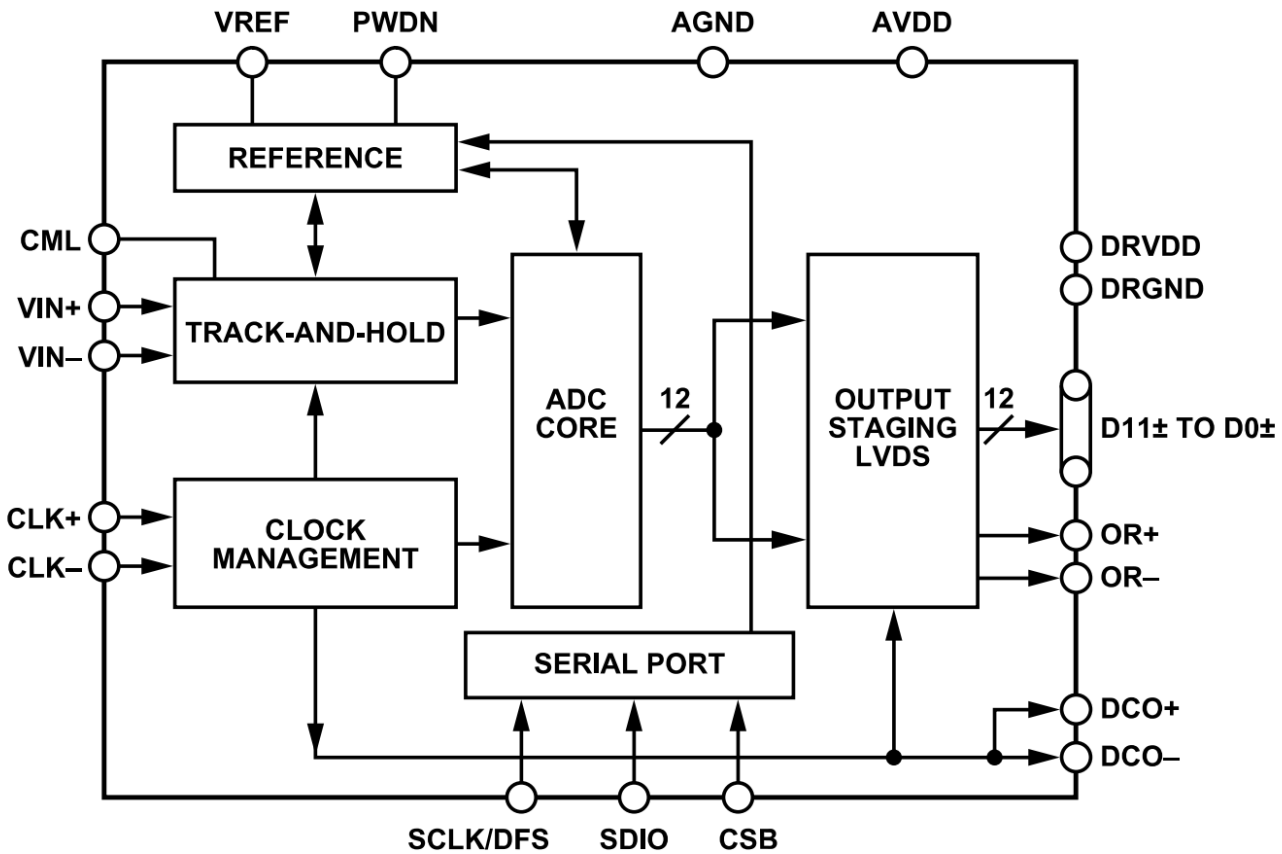
3. Overview

The ADCP9434-500 is a 12-bit single-edge sampling analog-to-digital converter (ADC) optimized for high performance, low power consumption, and ease of use. It achieves a conversion rate of 500 MSPS and exhibits excellent dynamic performance in broadband applications. All necessary functions are integrated on-chip, including a sample-and-hold amplifier (SHA) and an on-chip reference voltage source, providing a complete signal conversion solution. The VREF pin can be used to change the internal reference voltage or accept an external reference voltage (external reference mode requires enabling via the SPI port). This ADC requires a 1.8V analog supply and a differential clock to maintain excellent overall ADC performance. The digital output is LVDS (ANSI-644) compliant, with data formats of two's complement, Gray code, or offset binary. A data output clock ensures correct timing for the corresponding data outputs. This product is packaged in a 56-lead plastic package (QFN56).

4. Device Packaging Information

Product Model	Package Type	Package size
ADCP9434-500	QFN56	8mm×8mm

5. Functional Block Diagram



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6. Pin Configuration and Functions

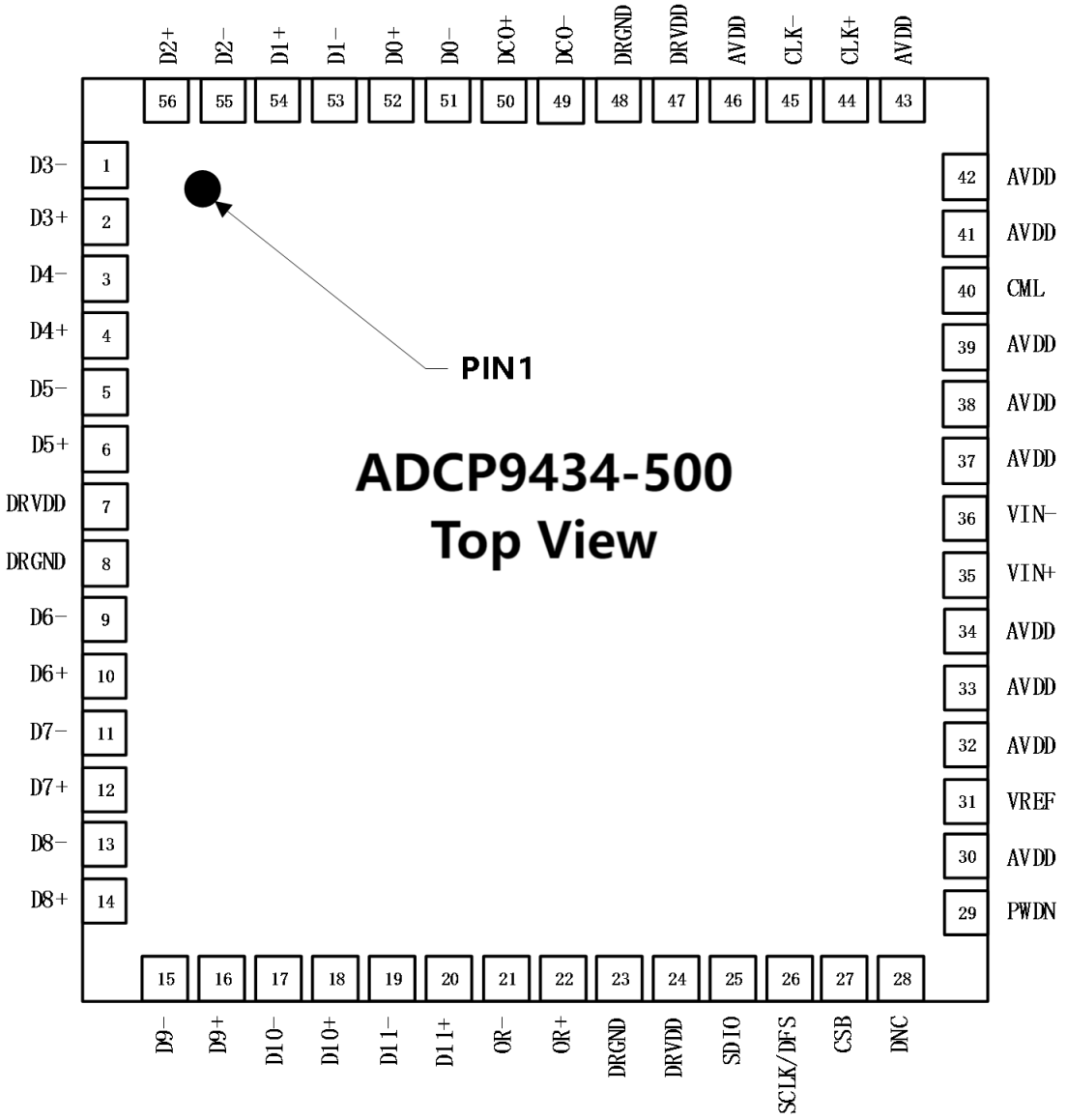


Figure 1. QFN56 Pin Diagram

Pin Functions

Pin No.	Pin Name	Pin Function	Pin No.	Pin Name	Pin Function
1	D3-	D3 Differential Output, Negative Terminal	29	PWDN	Shutdown mode selection
2	D3+	D3 Differential Output, Positive Terminal	30	AVDD	1.8V analog power supply
3	D4-	D4 Differential Output, Negative Terminal	31	VREF	Reference voltage input/output
4	D4+	D4 Differential Output, Positive Terminal	32	AVDD	1.8V analog power supply
5	D5-	D5 Differential Output, Negative Terminal	33	AVDD	1.8V analog power supply
6	D 5+	D5 Differential Output, Positive Terminal	34	AVDD	1.8V analog power supply
7	DRVDD	1.8V digital power supply	35	VIN+	Analog differential input positive terminal
8	DRGND	Digital	36	VIN-	Analog differential input negative terminal
9	D6-	D6 Differential Output, Negative Terminal	37	AVDD	1.8V analog power supply
10	D6+	D6 Differential Output, Positive Terminal	38	AVDD	1.8V analog power supply
11	D7-	D7 Differential Output, Negative Terminal	39	AVDD	1.8V analog power supply
12	D7+	D7 Differential Output, Positive Terminal	40	CML	Common-mode voltage bias output
13	D8-	D8 Differential Output, Negative Terminal	41	AVDD	1.8V analog power supply
14	D8+	D8 Differential Output, Positive Terminal	42	AVDD	1.8V analog power supply
15	D9-	D9 Differential Output, Negative Terminal	43	AVDD	1.8V analog power supply
16	D9+	D9 Differential Output, Positive Terminal	44	CLK+	Clock differential input, positive terminal
17	D10-	D10 Differential Output, Negative Terminal	45	CLK–	Clock differential input, negative terminal
18	D10+	D10 Differential Output, Positive Terminal	46	AVDD	1.8V analog power supply
19	D11-	D11 Differential Output, Negative Terminal	47	DRVDD	1.8V analog power supply
20	D11+	D11 Differential Output, Positive Terminal	48	DRGND	Digital
21	OR-	Overflow check bit, negative end	49	DCO–	Data clock, negative end
22	OR+	Overflow check bit, positive terminal	50	DCO+	Data clock, positive terminal
23	DRGND	Digital	51	D0–	D0 Differential output, negative terminal
24	DRVDD	1.8V digital power supply	52	D0+	D0 Differential output, positive terminal
25	SDIO	SPI data input/output (serial mode)	53	D1-	D1 Differential Output, Negative Terminal
26	SCLK/DFS	SPI Clock (Serial Mode) / Output Data Format Selection (External Pin Mode)	54	D1+	D1 Differential Output, Positive Terminal
27	CSB	SPI chip select (active low)	55	D2-	D2 Differential Output, Negative Terminal
28	DNC	------	56	D2+	D2 Differential Output, Positive Terminal

7. Electrical Characteristics

Unless otherwise specified, AVDD=1.8V, DRVDD=1.8V, GND=DRGND=0V, $V_{IN(P-P)}$ ≤1.5V, -40℃≤T_A ≤85 ℃.

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Resolution	RES				12		bits
Offset error	E_O			-5.0	-1.17	5.0	mV
Gain error	E_G			-9	1.73	9	%FS
Differential linearity error	E_{DL}			-1.5	0.61	1.5	LSB
Integral linearity error	E_L			-4.5	1.60	4.5	LSB
Internal reference voltage	V_{REF}			0.7	0.739	0.8	V
Power supply current (1)	I				348.18	500	mA
LVDS differential output voltage	V_{OD}			200	286.47	500	mV
LVDS common-mode output voltage	V_{OS}			1.0	1.19	1.45	V
Power consumption	P_W				626.73	900	mW
Standby power consumption	P_{SDB}				14.94	60	mW
Sleep power consumption	P_{PDN}				1.32	12	mW
Signal-to-noise ratio	SNR	f_{CLK} = 500MHz	T_A = 25℃, f_{IN} = 30.3MHz	63	65.61		dBFS
			T_A = 25℃, f_{IN} = 450.3MHz	61	63.7		dBFS
			T_A = -55℃, 85℃, f_{IN} = 30.3MHz	58	64.54		dBFS
Signal-to-noise ratio	SINAD	f_{CLK} = 500MHz	T_A = 25℃, f_{IN} = 30.3MHz	62	65.41		dBFS
			T_A = 25℃, f_{IN} = 450.3MHz	60	62.46		dBFS
			T_A = -55℃, 85℃, f_{IN} = 30.3MHz	57	64.02		dBFS
Valid bits	ENOB	f_{CLK} = 500MHz	T_A = 25℃, f_{IN} = 30.3MHz	10.0	10.49		bits
			T_A = 25℃, f_{IN} = 450.3MHz	9.5	10.03		bits
			T_A = -55℃, 85℃, f_{IN} = 30.3MHz	9.2	10.45		bits
Stray dynamic range	SFDR	f_{CLK} = 500MHz	T_A = 25℃, f_{IN} = 30.3MHz	72	81.79		dBFS
			T_A = 25℃, f_{IN} = 450.3MHz	66	71.88		dBFS
			T_A =-55℃, 85℃, f_{IN} = 30.3MHz	65	80.75		dBFS
Data latency	tPD				4.52	10	ns

Note (1): The power supply current is the sum of the analog power supply current (I_{CC}) and the digital power supply current (I_{DD}).

8. Absolute Maximum Ratings

Parameter	Value
Analog power supply voltage	2V
Digital power supply voltage	2V
Storage temperature range	-65°C to +150°C
Junction temperature	175°C

9. Recommended Working Conditions

Parameter	Value
Operating frequency	≤500MHz
Analog power supply voltage	1.75V to 1.9V
Digital power supply voltage	1.75V to 1.9V
Analog input common-mode voltage	1.6V to 1.8V
Operating ambient temperature	-40°C to +85°C
Input signal amplitude range	($V_{IN(P-P)}$) ≤ 1.5V

10. Timing Specifications

Unless otherwise specified, AVDD = 1.8V, DRVDD = 1.8V. T_{MIN} = -40°C, T_{MAX} = +85°C, f_{IN} = -1.0dBFS, full scale = 1.5V.

Parameter	Condition	Min	Typ	Max	Unit
Maximum conversion rate	Full	500			MSPS
Minimum conversion rate	Full			50	MSPS
CLK+ pulse width is high (t_{CH}) [1, 2]	Full	0.9		11	ns
CLK+ has a low pulse width (t_{CL})	Full	0.9		11	ns
Output (LVDS-SDR mode) [1]					
Data propagation delay (t_{PD})	Full		3.55		ns
Rise time (t_R) (20% to 80%)	25°C		0.15		ns
Fall time (t_F) (20% to 80%)	25°C		0.15		ns
DCO propagation delay (t_{CPD})	Full		3.3		ns
DCO skew data (t_{SKEW})	Full	0.15		0.38	ns
Delay time	Full		15		Cycles
Output (LVDS-DDR mode) [2]					
Data propagation delay (t_{PD})	Full		3.3		ns
Rise time (t_R) (20% to 80%)	25°C		0.15		ns
Fall time (t_F) (20% to 80%)	25°C		0.15		ns
DCO propagation delay (t_{CPD})	Full		3.3		ns
DCO skew data (t_{SKEW})	Full	-0.07		+0.07	ns
Delay time	Full		15		Cycles
Aperture time (t_A)	25°C		0.85		ns
Aperture uncertainty (jitter,t_J)	25°C		80		fs rms

Note: [1] See Figure 2

[2] See Figure 3

Timing Diagram

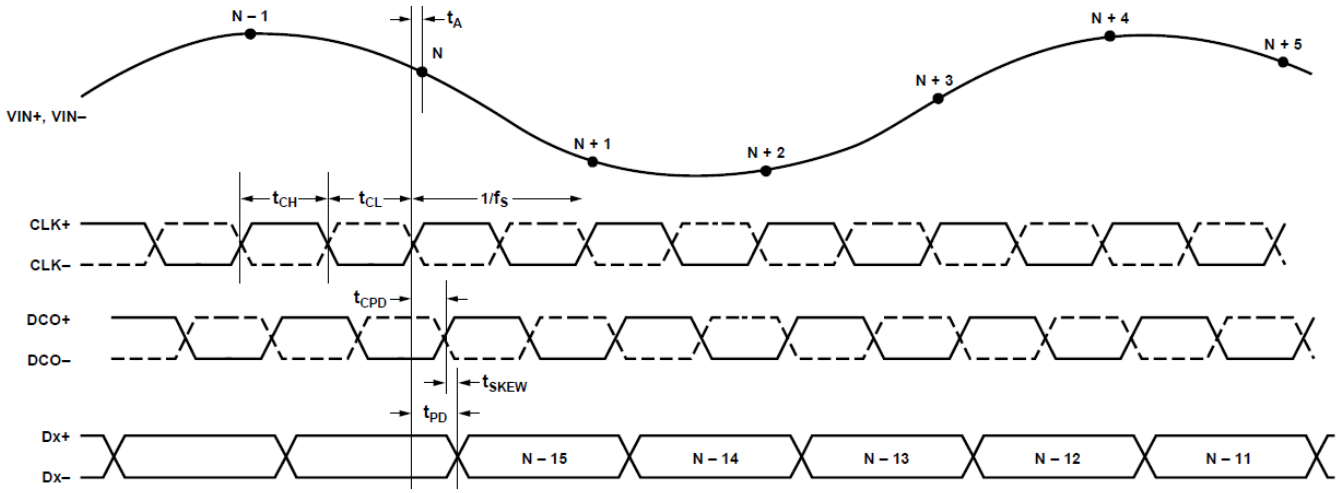


Figure 2. Single Data Rate Mode

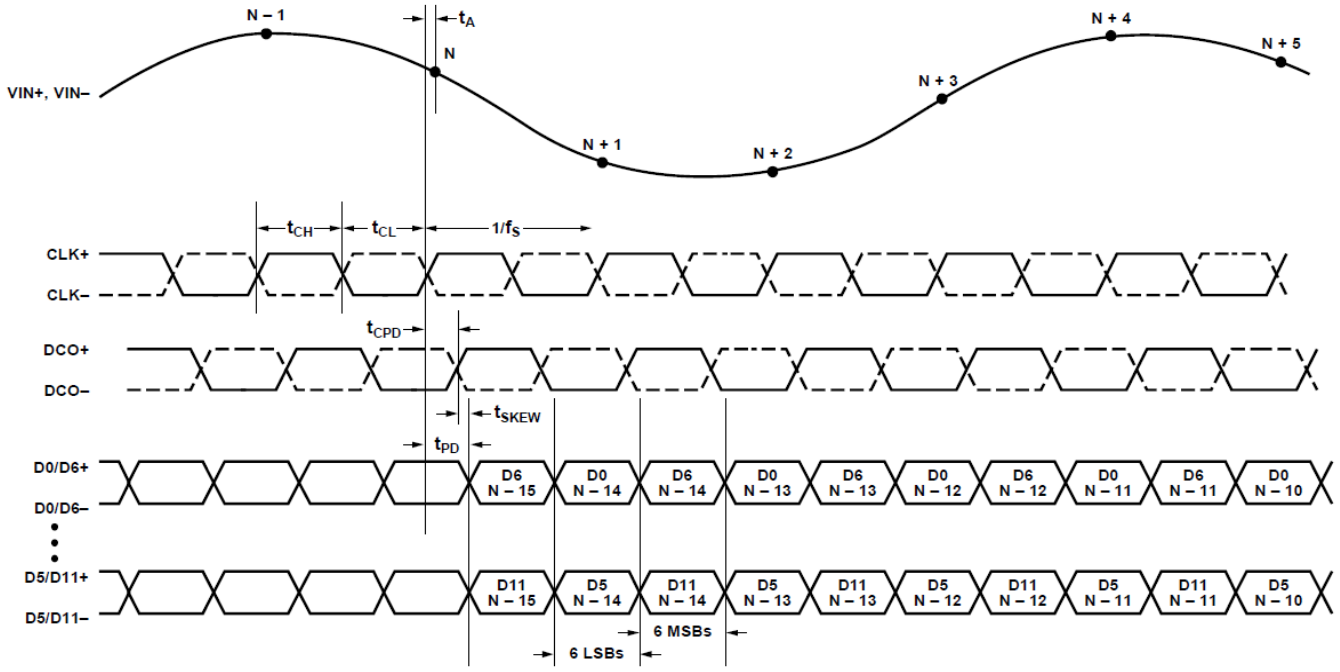


Figure 3. Double Data Rate Mode

11. Typical Application Circuit Diagram

11.1 Analog Input Circuit

Optimal chip performance can be achieved when the ADCP9434-500 is driven via differential input configuration. In baseband applications, differential drivers (e.g., 8138) provide excellent performance and flexible interface for the ADC. The differential driver output common-mode voltage is easily set to AVDD/2+0.5V, and this driver can be configured as a Sallen-Key filter topology for bandwidth limiting of the input signal.

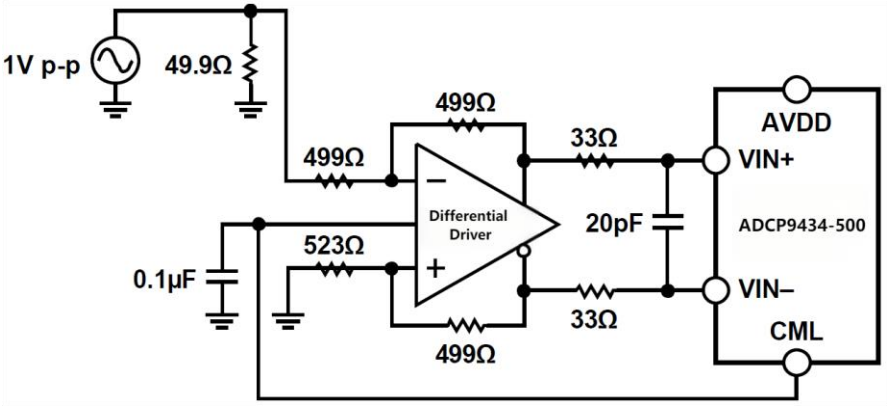


Figure 4. Differential input configuration using a differential driver (e.g., 8138)

When the input frequency is in the second or higher Nyquist region, the noise performance of most amplifiers is insufficient to achieve the true SNR performance of the ADCP9434-500. This phenomenon is particularly pronounced in IF undersampling applications with frequencies between 70MHz and 100MHz. For such applications, a differential double balun-coupled input configuration is recommended. The signal characteristics of the transformer must be considered when selecting it. Most RF transformers saturate below a few megahertz; excessive signal power can also cause core saturation, leading to distortion. In any configuration, the parallel capacitor value C depends on the input frequency and source impedance, and may need to be reduced or the parallel capacitor removed.

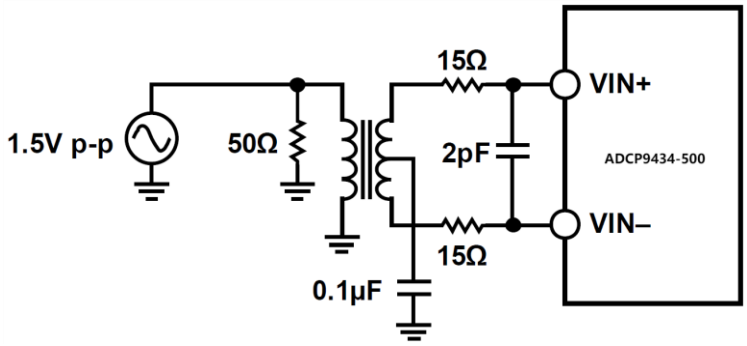


Figure 5. Differential transformer coupling configuration

When the frequency is in the second Nyquist region, in addition to using a transformer-coupled input, a differential driver (e.g., 8352) can also be used , as shown in Figure 6.

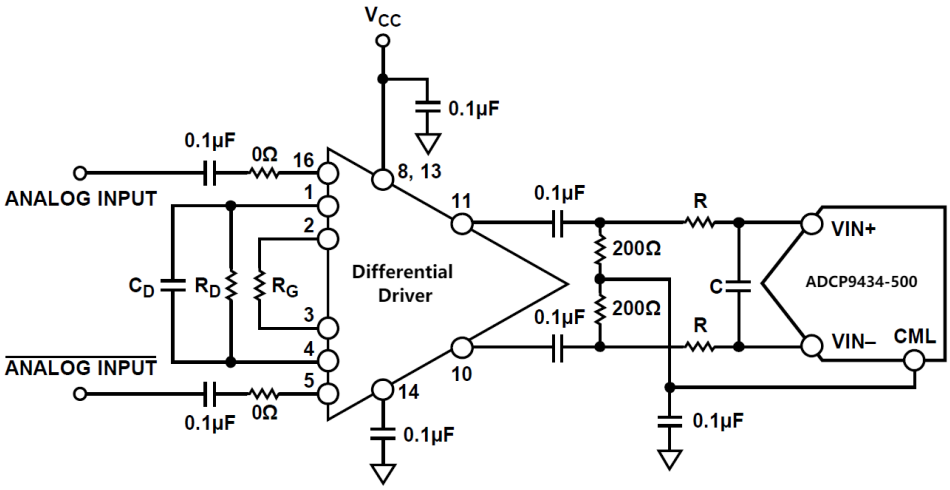


Figure 6. Differential input configuration using a differential driver (e.g., 8352)

11.2 Clock Input Circuit

To fully utilize the chip's performance, a differential signal should be used as the clock signal for the ADCP9434-500 sampling clock inputs (CLK+ and CLK-). Typically, a transformer or two capacitors should be used to AC couple this signal to the CLK+ and CLK- pins. The CLK+ and CLK- pins have an internal bias of approximately 0.9V, requiring no external bias. If the clock signal is DC-coupled, then the common-mode voltage should be maintained within the 0.9V range.

Figure 7 illustrates a preferred method for providing a clock signal to the ADCP9434-500 . Using an RF transformer, the single-ended signal of the low-jitter clock source is converted into a differential signal. Back-to-back Schottky diodes connected across the transformer's secondary winding limit the clock signal input to the ADCP9434-500 to a differential peak-to-peak value of approximately 0.8V. This preserves the signal's fast rise and fall times while preventing large voltage swings from feeding into other parts of the ADCP9434-500 , which is crucial for low-jitter performance.

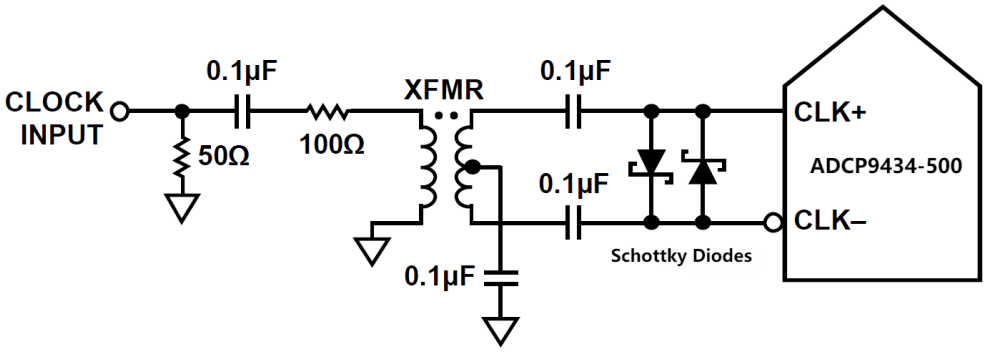


Figure 7. Transformer - coupled differential clock configuration

If a low-jitter clock source is unavailable, another approach is to AC couple the differential PECL signal and transmit it to the sampling clock input pin (as shown in Figure 8).

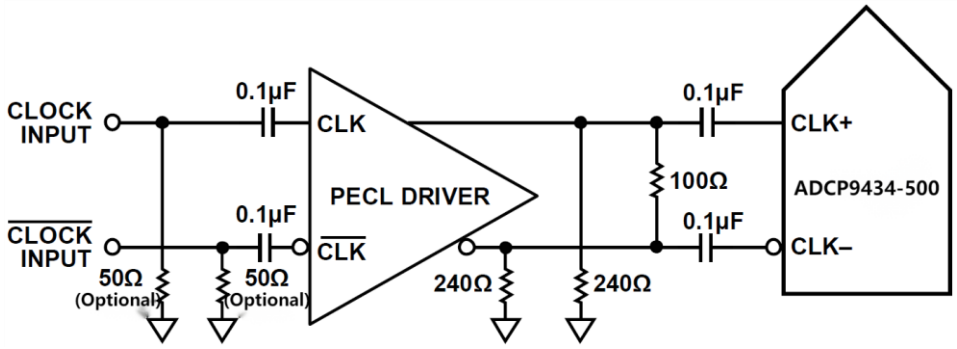


Figure 8. Differential PECL sampling clock

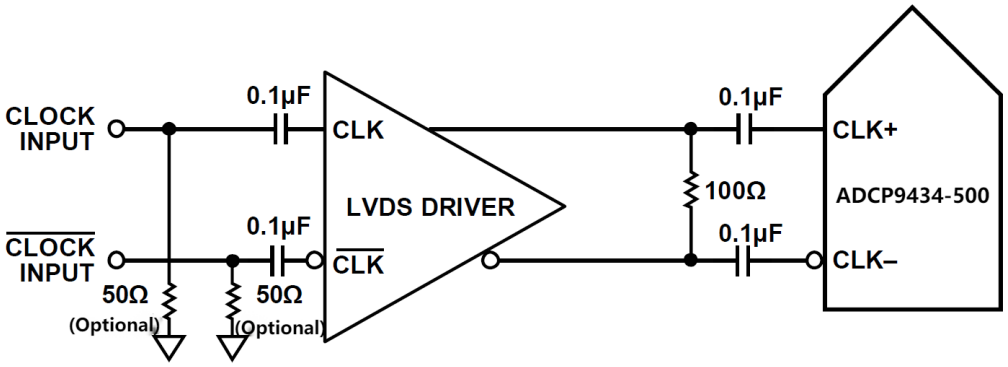


Figure 9. Differential LVDS sampling clock

In some applications, a single-ended CMOS signal can be used to drive the sampling clock input. In such applications, the CLK+ pin is directly driven by a CMOS gate, while the CLK- pin is bypassed to ground through a 0.1F capacitor. When driving CLK+ with a 1.8V CMOS signal, the CLK- pin is biased through a parallel connection of a 0.1F capacitor and a 39k resistor (as shown in Figure 10).

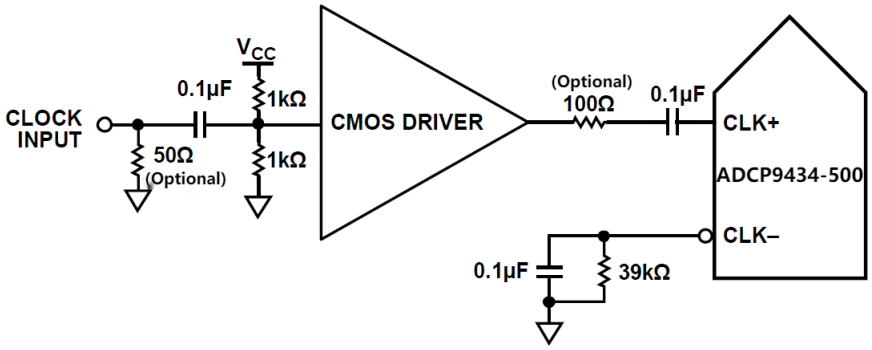


Figure 10. Single -ended 1.8V CMOS input clock

11.3 Digital Output

The ADCP9434-500 differential outputs conform to the ANSI-644 LVDS standard by default power-on. This can be changed using SPI to a low-power, low-signal option similar to the IEEE 1596.3 standard. This LVDS standard can further reduce the overall power consumption of the device, resulting in a power reduction of approximately 39mW. See the Memory Mapping section for more information. The LVDS driver current is derived on-chip, setting the output current at each output terminal to a nominal 3.5mA. A 100Ω differential terminating resistor placed at the LVDS receiver input causes the receiver to swing by a nominal 350mV.

The ADCP9434-500 LVDS output facilitates interface connections with LVDS receivers in custom ASICs and FPGAs that feature LVDS capabilities for superior switching performance in noisy environments. A single-point-to-point network topology is recommended, with the 100Ω terminating resistor placed as close to the receiver as possible. Poor termination at the remote receiver or inadequate differential tracking routing will not cause timing errors. Trace lengths should not exceed 24 inches, and differential output traces should be kept close together and of equal length.

- **Timing**

The ADCP9434-500 provides latched data outputs with a pipelined delay of seven clock cycles. The data output is available after a propagation delay (tPD) following the rising edge of the clock signal. Minimize the length of the output data lines and the load applied to them to reduce transients within the ADCP9434-500 . These transients degrade the converter's dynamic performance. The ADCP9434-500 also provides a Data Clock Output (DCO) for capturing data from external registers. The data output is valid on the rising edge of the DCO. The ADCP9434-500 has a minimum conversion rate of 50 MSPS. When the clock frequency drops below 1 MSPS, the ADCP9434-500 enters standby mode.

- **Reference voltage**

of the ADCP9434-500 allows the user to monitor the onboard voltage reference or provide an external reference (configurable via SPI). Three optional settings are internal VREF（pin connected to 20kΩ ground), output VREF，and input VREF．Do not connect bypass capacitors to this pin. VREF is internally compensated; additional loads may affect performance.

- **ADCP9434-500 using SPI**

The ADCP9434-500 SPI allows users to configure the converter for specific functions or operations via the structured register space within the ADC. This provides users with additional flexibility to customize device operation according to their application. Addresses are accessed serially in 1-byte words (programmed or read back). Each byte can be further divided into fields, which are recorded in the memory-mapped portion. Three pins define the Serial Port Interface (SPI) for this particular ADC: SCLK/DFS, SDIO, and CSB. SCLK/DFS (Serial Clock) is used to synchronize read and write data presented to the ADC. SDIO (Serial Data Input/Output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory-mapped registers. CSB is a low-level control that activates or disables read/write cycles (as shown in Table 1).

Name	Function
SCLK	SCLK (Serial Clock) is the serial shift clock in the system. SCLK is used for synchronizing serial interface read and write operations.
SDIO	SDIO (Serial Data Input/Output) is a dual-purpose pin. Its typical function is both input and output, depending on the command being sent and its relative position within the timing frame.
CSB	CSB (Chip Select) is an active low-level control that gates the read/write cycles.

Table 1. Serial Port Pins

The falling edge of CSB and the rising edge of SCLK together determine the start of a frame. Examples of serial timing and its definition can be found in Figure 11 and Table 2.

Name	Minimum value (unit: ns)	Description
t_{DS}	5	Set time between data and the rising edge of SCLK
t_{DH}	2	Hold time between data and the rising edge of SCLK
t_{CLK}	40	Clock cycle
t_S	5	Set time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HIGH}	16	The shortest time SCLK should be in a logical high state
t_{LOW}	16	The shortest time SCLK should be in a logical low state
t_{EN_SDIO}	1	The shortest time for the SDIO pin to switch from input to output relative to the falling edge of SCLK (not shown in Figure 11).
t_{DIS_SDIO}	5	The shortest time for the SDIO pin to switch from output to input relative to the rising edge of SCLK (not shown in Figure 11).

Table 2. Serial Timing Definition

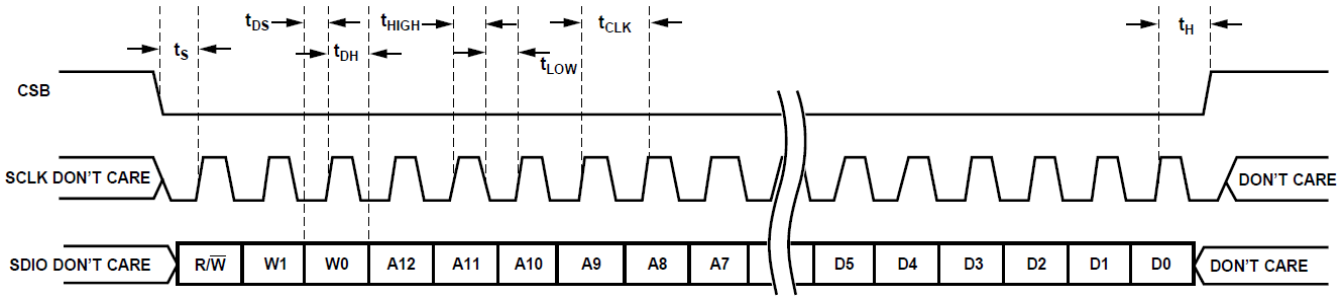


Figure 11. Serial Port Interface Timing Diagram

- **Configuration without SPI**

In applications that do not interface with the SPI control register, the SCLK/DFS pins can be used alternatively as independent CMOS-compatible control pins. In this mode, connecting the CSB pin to AVDD disables the serial port interface.

Name	External voltage	Configuration
SCLK/DFS	AVDD	Twos complementary functionality is enabled.
	AGND	Offset binary is enabled

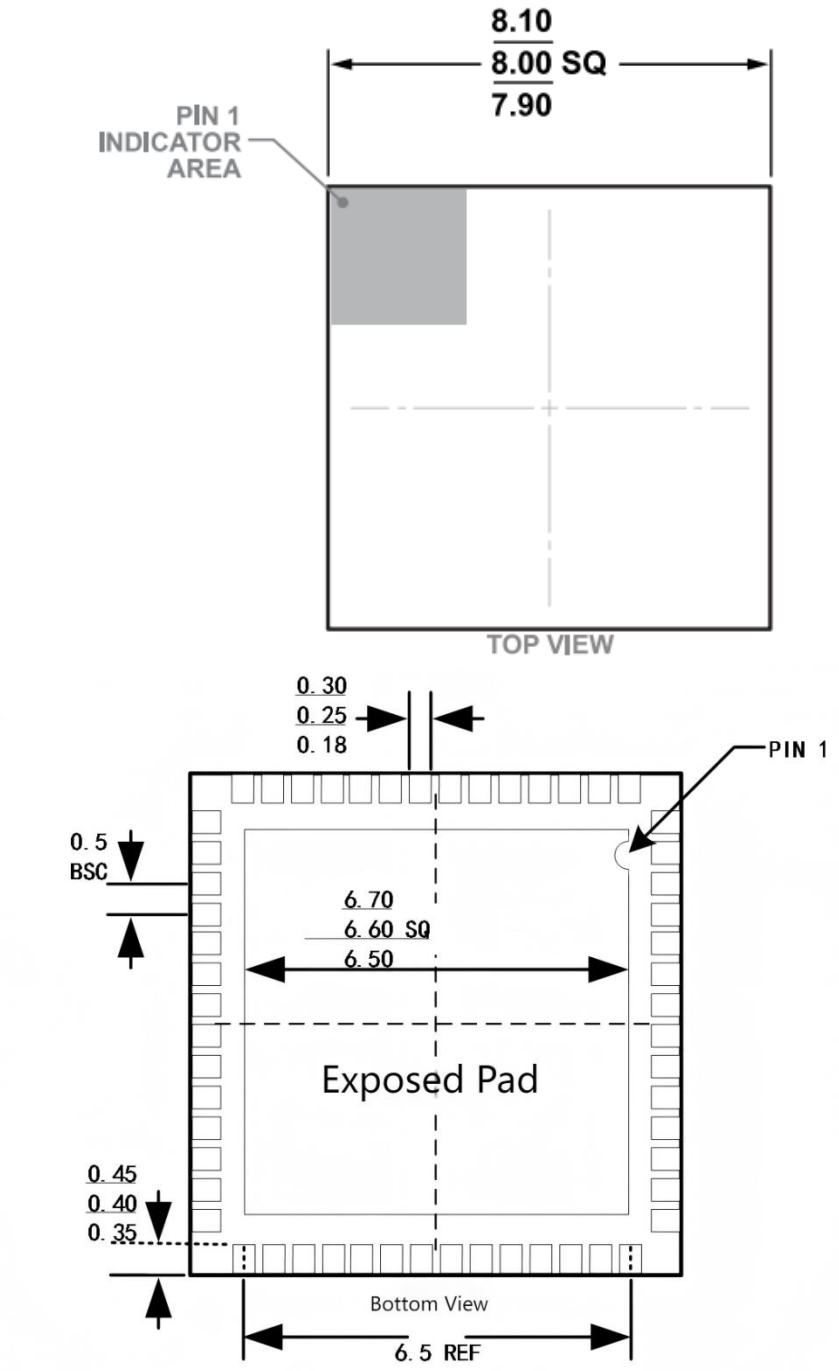
Table 3. Mode Selection

Input	Condition	Offset binary mode, D11 to D0	Binary two's complement mode, D11 to D0	OR±
VIN+ − VIN−	< 0.75 − 0.5 LSB	0000 0000 0000	1000 0000 0000	1
VIN+ − VIN−	= −0.75	0000 0000 0000	1000 0000 0000	0
VIN+ − VIN−	= 0	1000 0000 0000	0000 0000 0000	0
VIN+ − VIN−	= 0.75	1111 1111 1111	0111 1111 1111	0
VIN+ − VIN−	> 0.75 + 0.5 LSB	1111 1111 1111	0111 1111 1111	1

Table 4. Output Data Format

12. Packaging Dimensions and Structure

QFN56 package



13. Device Ordering Information

Model	Temperature Range	Packaging Type	Package
ADCP9434-500	-40 ℃ ~85 ℃	QFN56	260/reel