1. Features

- Low power consumption : 495mW (125MSPS)
- 1.8V analog power supply
- 1.8V CMOS or LVDS output power supply
- Signal-to-noise ratio (SNR) = 76.6 dBFS (Fin=30.5MHz@125MSPS)
- Spurious-free dynamic range (SFDR) = 88 dBc (Fin=30.5MHz@125MSPS)
- On-chip reference voltage source and sample-and-hold circuit
- QFN-64 package , 9mm x 9mm

2. Applications

- Communication
- Diversity radio system
- Multi-mode digital receiver (3G)
- I/O demodulation system
- Smart antenna system
- Battery-powered meters
- Battery-powered meters
- Portable medical imaging
- Ultrasonic equipment
- Radar /LIDAR

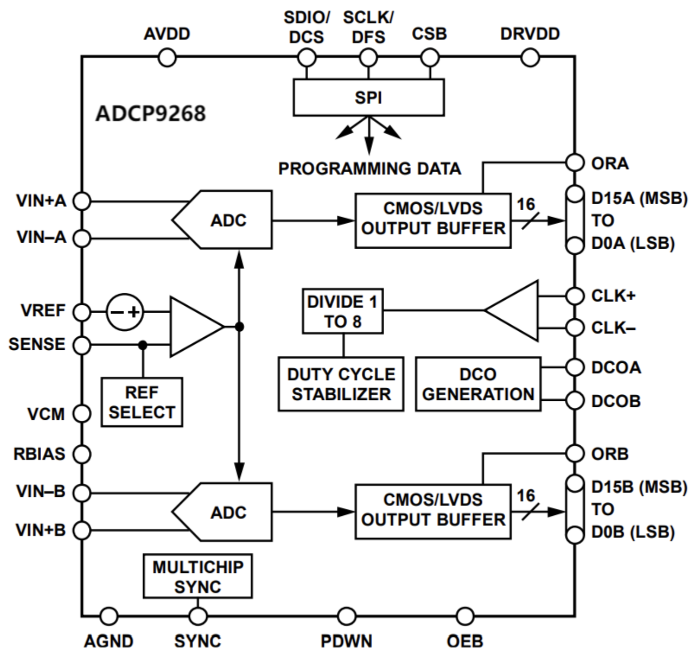
3. Overview

The ADCP9268-80/105/125 is a dual-channel, 16-bit, 80/105/125MSPS analog-to-digital converter (ADC) powered by a 1.8V supply. It features integrated high-performance sample-and-hold circuitry and an on-chip reference voltage source. Employing a multi-stage differential pipelined architecture with built-in output error correction logic, it provides 16 -bit accuracy at a 125MSPS data rate and guarantees no missing codes across the entire operating temperature range. This ADC incorporates various features to optimize device flexibility and minimize system cost, such as generating programmable digital test codes. Available digital test codes include built-in fixed codes and pseudo-random codes, as well as user-defined test codes input via a serial port interface (SPI) . A single differential clock input controls all internal conversion cycles. The digital output data format is offset binary, Gray code, or two's complement. Each ADC channel has a data output clock (DCO) to ensure correct latching timing for the receive logic. This device supports 1.8V CMOS output and LVDS output, and the output data can be multiplexed on a single output bus. It uses a RoHS- compliant 64-pin QFN.

4. Device Information

Device Model	Packaging Type	Package Size (nominal value)
ADCP9268	QFN64	9mm*9mm

5. Functional Block Diagram



www.dsown.com
Email：info@dsown.com

6. Technical Specifications

6.1 ADC DC Specifications

Unless otherwise specified, AVDD=1.8V, DRVDD=1.8V, VIN= −1.0dBFS differential input, 1.0V internal reference voltage.

Table 1.

Parameter	Condition	ADCP9268-80			ADCP9268-105			ADCP9268-125			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution			16			16			16		Bit
No missing codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset error	Full		±0.1	±0.7		±0.1	±0.7		± 0.1	±0.7	%FSR
Gain error	Full		-1.5			-1.5			-1.5		%FSR
Differential nonlinearity[1] (DNL)	Full 25 ℃	-0.75	±0.45	0.75	-0.75	±0.45	0.75	-0.75	± 0.45	0.75	LSB
Integral Nonlinearity[1] (INL)	Full 25 ℃	-2.5	±1.0	2.5	-2.5	±1.0	2.5	-2.5	± 1.0	2.5	LSB
Internal reference voltage error	Full		± 5			± 5			± 5		mV
Input reference noise (VREF=1V)	25 ℃		0.98			0.98			0.98		LSB rms
Analog input range (VREF=1V)	Full		2			2			2		Vpp
Input capacitor[2]	Full		4			4			4		pF
Input common mode voltage	Full		0.95			0.95			0.95		V
AVDD power supply voltage	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD power supply voltage	Full	1.7		1.8	1.7		1.8	1.7		1.8	V
I_{AVDD} power supply current	Full		194.9	200		200.8	210		210	220	mA
I_{DRVDD1} Power Supply Current (CMOS)	Full		76.2			81			85		mA
I_{DRVDD2} Supply Current (LVDS)	Full		66.9			69.7			71		mA
DC input power consumption	25 ℃		475	490		485	500		495	510	mW
Sine wave input power consumption [1] (CMOS)	Full		488			507			522		mW
Sine wave input power consumption [1] (LVDS)	Full		471			487			597		mW
Shutdown power consumption	25 ℃		2			2			2		mW

1. The measurement conditions were: 5MHz input frequency, full-scale sine wave, and approximately 5pF load per output bit.
2. Input capacitance refers to the effective capacitance between a differential input pin and AGND.

www.dsown.com
Email：info@dsown.com

6.2 ADC AC Specifications

Unless otherwise specified, AVDD = 1.8V, DRVDD = 1.8V, VIN = −1.0dBFS differential input, 1.0V internal reference voltage.

Table 2.

Parameter	Condition	ADCP9268-80			ADCP9268-105			ADCP9268-125			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Signal-to-noise ratio (SNR)											
fin=30.5MHz	25 ℃		78.7			77.2			76.5		dBFS
	Full	78.2			76.8			76.1			dBFS
fin=60MHz	25 ℃		77.6			76.5			75.4		dBFS
SinNabi (SNDR)											
fin=30.5MHz	25 ℃		77.7			76.9			75.3		dBFS
	Full	77.2			76.5			75.1			dBFS
fin=60MHz	25 ℃		76.1			74.4			71.6		dBFS
Significant digits (ENOB)											
fin=30.5MHz	25 ℃		12.6			12.5			12.2		B it
	Full	12.5			12.4			12.1			B it
fin=60MHz	25 ℃		12.3			12.1			11.6		B it
Stray-free dynamic range (third harmonic)											
fin=30.5MHz	25 ℃		92			92			92		dBc
	Full	88			88			88			dBc
fin=60MHz	25 ℃		8 2			8 2			77.3		dBc
Stray-free dynamic range (second harmonic)											
fin=30.5MHz	25 ℃		93			9 3			9 3		dBc
	Full	8 7			8 7			8 7			dBc
fin=60MHz	25 ℃		95			8 5			8 5		dBc
Crosstalk 1	Complete		-92			-92			-92		dB
Analog input bandwidth	25 ℃		700			700			700		MHz

1. Crosstalk measurement conditions: One channel has an input parameter of -1dBFS , a 60MHz signal, and there are no input signals on adjacent channels.

www.dsown.com
Email：info@dsown.com

6.3 Digital Specifications

Unless otherwise specified, AVDD = 1.8V, DRVDD = 1.8V, VIN = −1.0dBFS differential input, 1.0V internal reference voltage.

Table 3.

Parameter	Condition	Min	Typ	Max	Unit
Differential clock inputs (CLK+ , CLK-)					
Logical compatibility	Full	CMOS/LVDS/LVPECL			
Internal common-mode bias	Full		0.9		V
Differential input voltage	Full	0.2		3.6	Vp -p
Input voltage range	Full	GND-0.3		AVDD+0.2	V
Input capacitor	Full		3.5		pF
Input resistance	Full		8		kΩ
Logical inputs (PDWN, SYNC, SCLK, CSB, SDIO)					
Logic 1 voltage	Full	1.2		DRVDD+0.3	V
Logic 0 voltage	Full	0		0.8	V
Input resistance	Full		2 6		μA
Input capacitor	Full		2		μA
Digital output DRVDD=1.8V					
Logic 1 voltage	Full	1.79			V
Logic 0 voltage	Full			0.2	V
Encoding format (default)	Full		Offset binary		μA

6.4 Switch Specifications

Unless otherwise specified, AVDD = 1.8 V, DRVDD = 1.8 V, VIN = −1.0dBFS differential input, 1.0V internal reference voltage.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
Clock input parameters					
Clock input rate	Full			625	MHz
Conversion rate 1					
DCS Enable	Full	20		125	MSPS
DCS disabled	Full	10		125	MSPS
Clock cycle - divider mode (t_{CLK})		8			ns
Clock pulse width high level (t_{CH})					
One- division mode, DCS enabled	Full	2.5	4.3	5.7	ns
One-divide-off mode, DCS disabled	Full	3.7	4.2	4.3	ns
Frequency divider to octave divider mode		0.85			ns
Aperture delay (t_A)	Full	1			ns
Aperture uncertainty (jitter , t_J)	Full	0.07			ps rms
Data output parameters					
CMOS mode					
Data propagation delay (t_{PD})	Full	2.9	3.7	4.4	ns
DCO propagation delay (t_{DCO}) [2]	Full		3.3		ns
DCO to data skew (t_{SKEW})	Full	-0.63	-0.45	0	ns

1. The conversion rate refers to the clock rate after frequency division.
2. Additional DCO delay time can be added by configuring the corresponding value in the lower 4 bits of register 0x17 via SPI.
3. Wake-up time refers to the time required to return from power-down mode to normal operating mode.

www.dsown.com
Email：info@dsown.com

6.5 Timing Specifications

Unless otherwise specified, AVDD = 1.8 V , DRVDD = 1.8 V , VIN = −1.0 dBFS Differential input, 1.0 V internal reference voltage.

Table 5.

Parameter	Condition	ADCP9268-80			ADCP9268-105			ADCP9268-125			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock parameters											
Input clock rate	Full			625			625			625	MHz
Conversion speed	Full			80			105			125	MHz
Aperture delay (tA)	Full		1			1			1		ns
Aperture jitter	Full		0.1			0.1			0.1		ps rms
Data output parameters											
t_A	Full		1			1			1		ns
t_{CH}	Full		6.25			6.25			6.25		ns
t_{CLK}	Full		12.5			12.5			12.5		ns
t_{DCO}	Full		3			3			3		ns
t_{PD}	Full		3			3			3		ns
t_{SKEW}	Full		0.1			0.1			0.1		ns

6.6 Timing Diagram

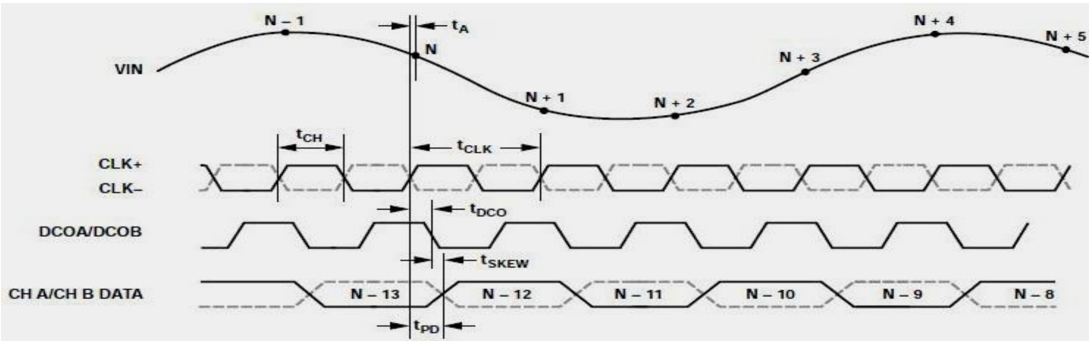


Figure 2. CMOS output timing

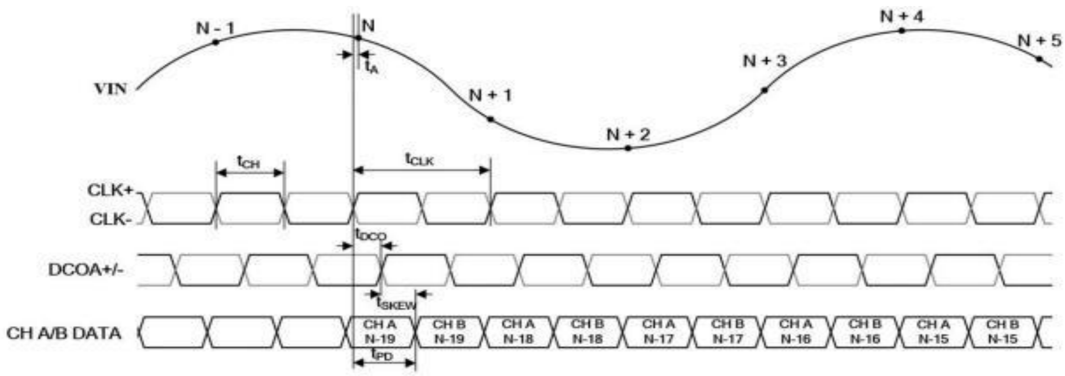


Figure 3. LVDS output timing

6.7 Switch Specifications

Unless otherwise specified, AVDD=1.8V, DRVDD=1.8V, typical sampling rate, VIN=−1.0dBFS differential input, 1.0V internal reference voltage.

Switching parameters

Parameter	Temperature	Min	Typ	Max	Unit
Clock input parameters					
Input clock rate	Full		120		MHz
Aperture delay (t_A)	Full		1	125	ns
Aperture jitter	Full		0.07		ps rms
Data output parameters					
Data transmission delay (tPD)	Full		3.5		ns
	Full		3.1		ns
DCO propagation delay (tDCO)	Full		-0.4		ns
DCO to data skew (tSKEW)					

6.8 Timing Specifications

Parameter	Condition	Limit
SPI Timing Requirements		
tDS	Setup time between data and the rising edge of SCLK	2ns, minimum value
tDH	Hold time between data and the rising edge of SCLK	2ns, minimum value
tCLK	SCLK cycle	40ns, minimum value
tS	Establishment time between CSB and SCLK	2ns, minimum value
tH	Hold time between CSB and SCLK	2ns, minimum value
tHIGH	SCLK high-level pulse width	10ns, minimum value
tLOW	SCLK low-level pulse width	10ns, minimum value

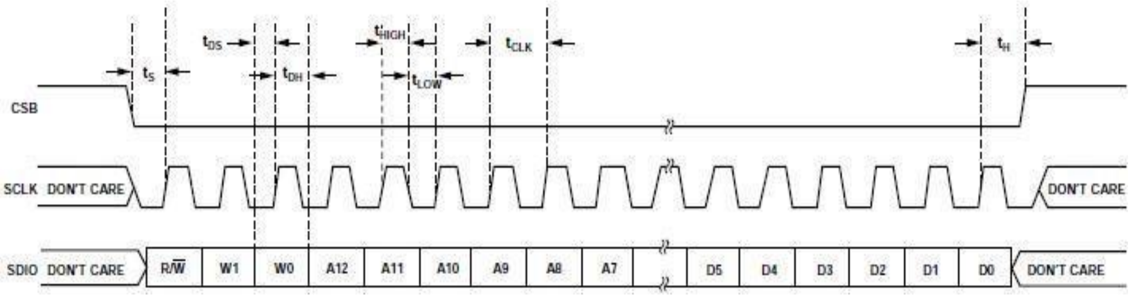


Figure 4. Serial port interface timings

6.9 Limiting Parameters

Parameter	Value
AVDD to AGND	-0.3V to 2V
DRVDD to AGND	-0.3V to 3.9V
Input voltages (VIN+/-, CLK+/-, VREF, SENSE, VCM, RBIAS)	-0.3V to AVDD+0.2V
Input voltages (CSB, SCLK, SDIO, PDWN)	-0.3V to DRVDD+0.3V
Output voltages (DCOA, DCOB, D0A/D0B to D13A/D13B)	-0.3V to DRVDD+0.3V
Maximum junction temperature $T_{J,MAX}$	150°C
Operating temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C
ESD (Human Body Model)	2000V

www.dsown.com
Email：info@dsown.com

7. Pin Configuration and Function Description

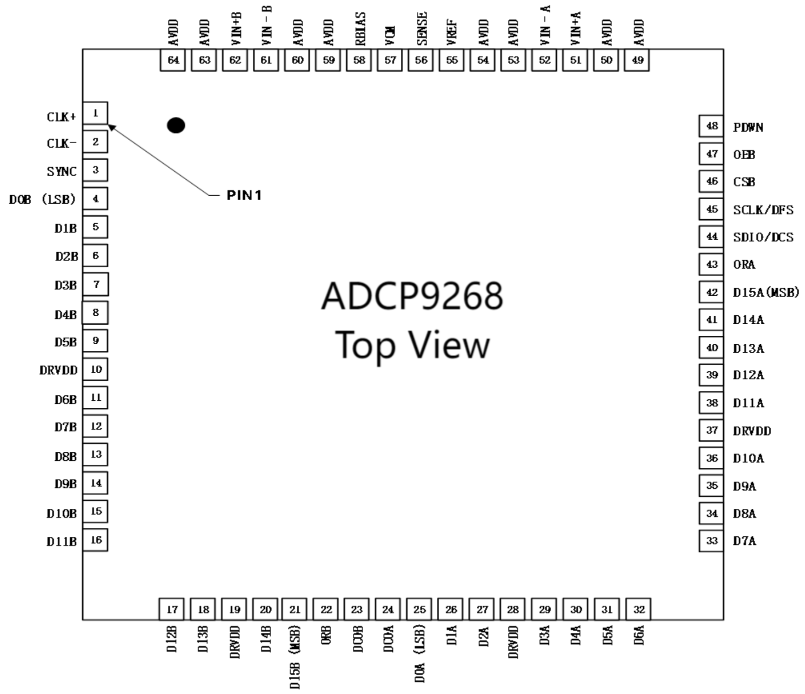


Figure 5. CMOS pin configuration (top view)

Table 6. Pin Function Descriptions (CMOS Mode)

Pin No.	Pin Name	Type	Description
0	AGND	G	The exposed thermal pad on the bottom of the package provides an analog ground for the device. This pad must be connected to ground.
1	CLK+	AI	ADC clock input (+)
2	CLK-	AI	ADC clock input (−)
3	SYNC	DI	Digital input for synchronous input clock divider
4 to 9, 11 to 18, 20, 21	D0B to D15B	DO	Channel B digital output
10, 19, 28, 37	DRVDD	P	Digital output drive power supply, 1.8V
22	ORB	DO	Channel B digital output, analog input out of range prompt foot
23	DCOB	DO	Channel B data clock output
24	DCOA	DO	Channel A data clock output
25 to 27, 29 to 36, 38 to 42	D0A to D15A	DO	Channel A digital output
43	ORA	DO	Channel A digital output, analog input out of range warning pin
4 4	SDIO	DIO	SPI data input and output
4 5	SCLK	DI	SPI clock input
46	CSB	DI	SPI chip selection bar, low enable operation, 30 kΩ Internal pull-up
4 7	OEB	DI	Digital input. If low, enables digital outputs for channels A and B; if high, enables tri-state outputs. 30kΩ internal pull-down.
33	PDWN	DI	Digital input, 30kΩ internal pull-down PDWN high = Power off; PDWN low = Equipment running, normal operation.
49, 50, 53, 54, 59, 60, 63, 64	AVDD	P	Analog power supply, 1.8V
51,52	VIN+A,VIN−A	AI	Channel A Differential Analog Input
55	VREF	AIO	Reference voltage input / output
56	SENSE	AI	Reference mode selection
57	VCM	AO	The chip output is used to provide the common-mode voltage for the analog input.
58	RBIAS	AI	Analog current bias Grounded using a 10 kΩ (1%) resistor.
61,62	VIN−B, VIN+B	AI	Channel B differential analog input

www.dsown.com
Email：info@dsown.com

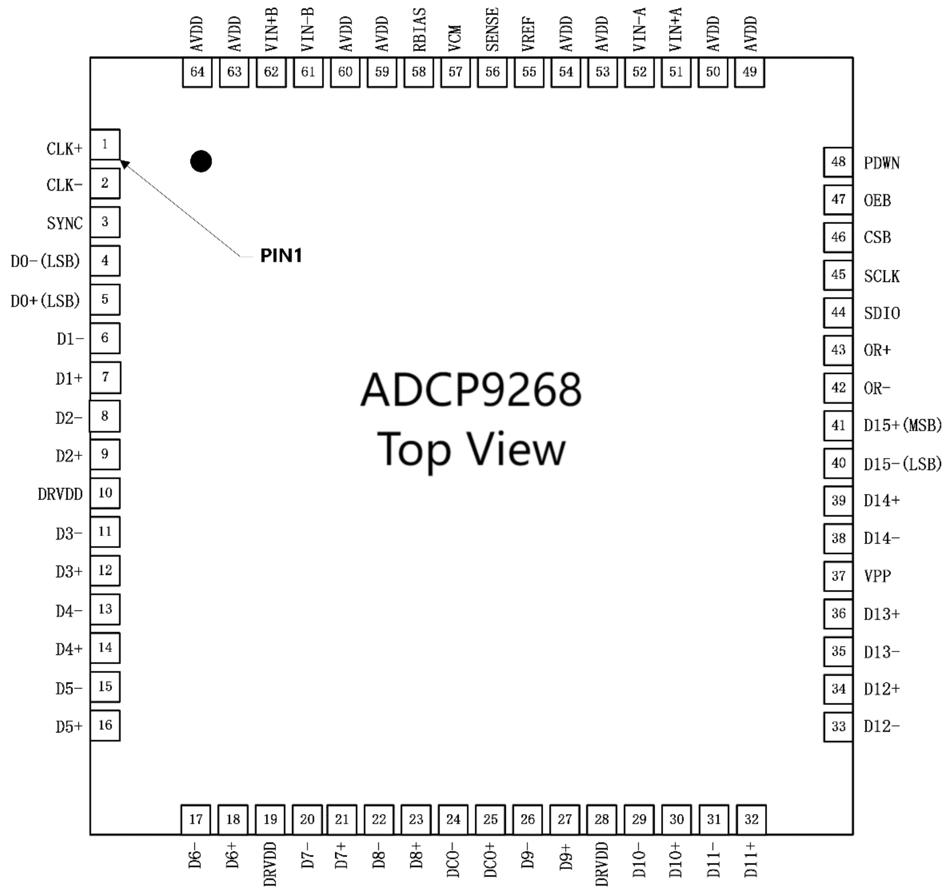


Figure 6. LVDS pin configuration (top view)

www.dsown.com
Email：info@dsown.com

Table 7. Pin Function Descriptions (LVDS Mode)

Pin No.	Pin Name	Type	Description
0	AGND	G	The exposed thermal pad on the bottom of the package provides an analog ground for the device. This pad must be connected to ground.
1	CLK+	AI	ADC clock input (+)
2	CLK-	AI	ADC clock input (−)
3	SYNC	DI	Digital input for synchronous input clock divider
4, 5, 6, 7	NC	- -	Suspended
4 to 9, 11 to 18, 20 to 23, 26, 27, 29 to 36, 38 to 41	D0-/+ to D15+/-	DO	Digital LVDS output
10, 19, 28, 37	DRVDD	P	Digital output drive power supply, 1.8V
42,43	OR-/+	DO	Channel B digital output, analog input out of range prompt foot
24,25	DCO-/+	DO	Data clock LVDS output
44	SDIO	DIO	SPI data input and output
45	SCLK	DI	SPI clock input

Pin No.	Pin Name	Type	Description
46	CSB	DI	SPI chip selection bar, low enable operation, 30 kΩ Internal pull-up
47	OEB	DO	Digital input. If low, enables digital outputs for channels A and B ; if high, enables tri-state outputs. 30kΩ internal pull-down.
33	PDWN	DI	Digital input, 30kΩ internal pull-down PDWN high = Power off; PDWN low = Equipment running, normal operation.
49, 50, 53, 54, 59, 60, 63, 64	AVDD	P	Analog power supply, 1.8V
51,52	VIN+A,VIN−A	AI	Channel A Analog Input
55	VREF	AIO	Reference voltage input / output
56	SENSE	AI	Reference mode selection
57	VCM	AO	Analog input common mode
58	RBIAS	AI	Analog current bias Grounded using a 10 kΩ (1%) resistor
61,62	VIN−B,VIN+B	AI	Channel B Analog Input

8. Typical application circuits

The typical application circuit for peripheral devices such as ADCP9268 input signal, input clock, and external DC pins is as follows.

- **Analog Input Network**

Using a fully differential mode ensures optimal ADC performance. To bias the analog input, the VCM voltage can be connected to the center tap of the transformer secondary winding. For applications above 10MHz , differential dual-balun coupling is recommended as the input configuration (see Figure 7). Alternatively, a fully differential op-amp can be used to drive the ADC. In single-ended applications, using the input network method of connecting VIN- to the common-mode voltage and VIN+ to the input signal will result in a decrease in ADC performance. Therefore, it is not recommended to drive the ADCP9268 input in a single-ended manner. In any configuration, the value of the parallel capacitor C depends on the input frequency and source impedance , and may need to be reduced or removed. Table 8 shows recommended values for setting up the RC network. However, these values depend on the input signal and are only recommended as application guidelines.

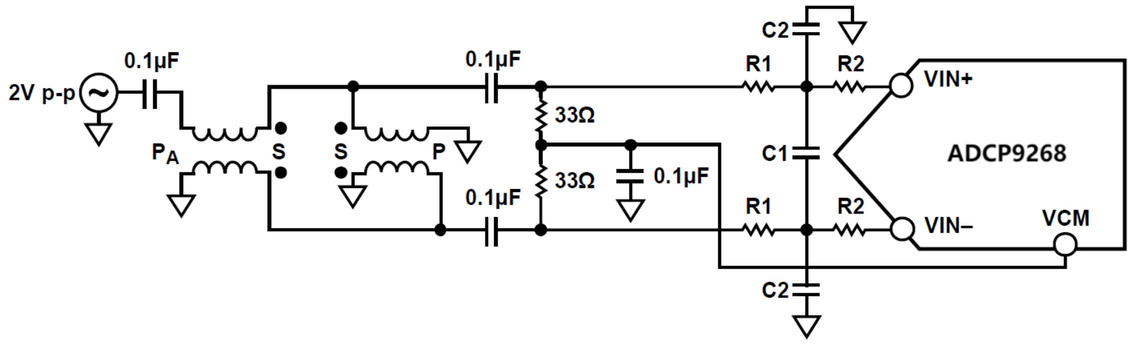


Figure 7. Differential dual balun input configuration

Table 8. Examples of RC Networks

Sampling frequency (MSPS)	Series resistor R1/Ω	Series resistance R2/Ω	Differential capacitor C1/pF	Parallel capacitor C2/pF
0-80	33	1 5	5	1 5
80-125	1 0	1 5	5	1 0

- **Clock input network**

To fully utilize the chip's performance, a differential clock should be used as the clock signal for the ADCP9268 's sampling clock input (CLK+/-). The input clock circuit has internal bias, eliminating the need for external bias. A balun- driven input is recommended, as shown in Figure 8. Back-to-back Schottky diodes connected across the transformer can limit the clock signal input to the ADCP9268 to approximately 0.8Vpp differentially . This prevents large clock voltage swings from feeding through to other parts and preserves the signal's rapid rise and fall times, resulting in less clock jitter and better ADC performance.

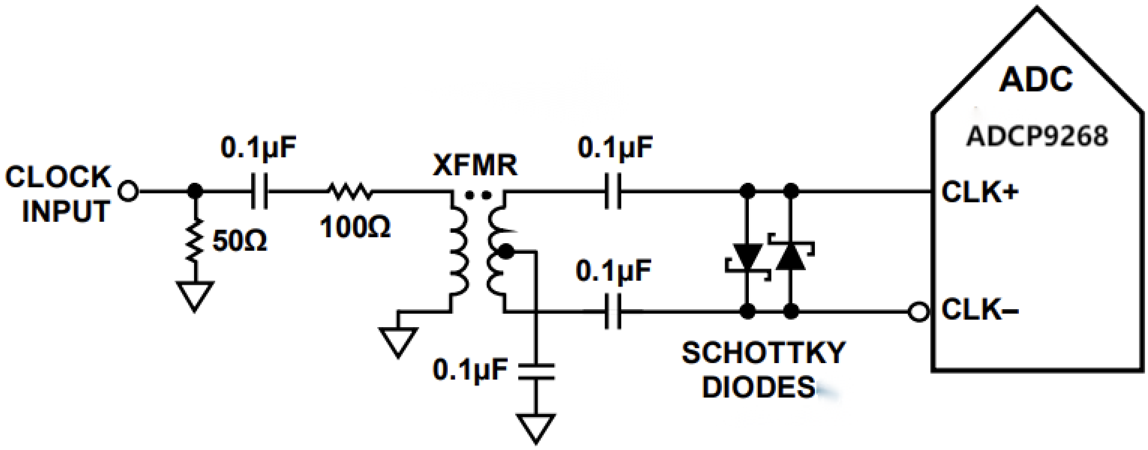


Figure 8. Clock Input Configuration

- **Baseline configuration**

The ADCP9268 's built-in comparator detects the voltage on the SENSE pin, allowing the reference voltage to be configured in two different modes (see Table 9). If the SENSE pin is grounded, the internal 1V reference voltage is used; if the SENSE pin is connected to AVDD, an external 1V reference voltage is used . It is recommended not to leave the SENSE pin floating.

Table 9. Summary of Reference Voltage Configurations

Selected mode	SENSE voltage	The corresponding VREF (V)	The corresponding differential range (Vpp)
External reference voltage	AVDD	1.0 (Applied to external VREF pin)	2.0
Internal reference voltage	AGND to 0.2	1.0 (Internal)	2.0

- **Digital output format**

The ADCP9268 output driver provides a 1.8V CMOS logic and LVDS output interface. CMOS output data can also be multiplexed onto a single output bus to reduce the total number of channels required to connect to the digital processing unit. Timing parameters are shown in Figures 2 and 3. The output driver should provide sufficient output current to drive various logic circuits; the drive force can be adjusted via a register. However, a large drive current may cause glitches in the power supply signal, affecting the converter's performance. Therefore, in applications requiring the ADC to drive large capacitive loads or have a large fan-out, an external buffer or latch may be necessary.

Table 10. Data Output Format

Input (V)	condition	Offset binary mode	Binary complement mode	Overflow
VIN+ - VIN-	< -VREF – 0.5LSB	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ - VIN-	= -VREF	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ - VIN-	=0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ - VIN-	=+VREF – 1LSB	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ - VIN-	>+VREF – 0.5LSB	11 1111 1111 1111	01 1111 1111 1111	1

- **Digital Output Enable (OEB)**

The ADCP9268 features flexible tri-state functionality for its digital output pins. Tri-state mode can be enabled using the OEB pin or via SPI configuration. If the OEB pin is low, the output I/O and DCO are enabled . If the OEB pin is high, the output I/O and DCO are in a high-impedance state. This OEB function is not used for fast access to the data bus. Note that the voltage when OEB is high is the digital supply voltage (DRVDD) and should not be exceeded. When configured using SPI , this can be achieved by pulling the output disable (OEB) bit (bit 4) high in register 0x14 . The data output and DCO output of each channel can be independently configured as tri-state outputs.

- **Time series**

The ADCP9268 provides a pipelined latency of 19 clock cycles for latching data . Data output is available after a propagation delay (tPD) following the rising edge of the clock signal. Minimizing the length of the output data lines and the load applied to them reduces transients

www.dsown.com
Email：info@dsown.com

in the ADCP9268 that can degrade the converter's dynamic performance. The ADCP9268 has a minimum typical conversion rate of 3 MSPS ; dynamic performance may degrade at clock rates below 3 MSPS .

- **Data Clock Output (DCO)**

The ADCP9268 provides two Data Clock Output (DCO) signals for capturing data from the digital output. Unless the DCO clock polarity is changed via SPI , the CMOS data output is valid on the rising edge of the DCO . See Figures 2 and 3 for a graphical timing description.

- **Built-in self-test (BIST)**

BIST is a thorough test of the digital portion of the selected ADCP9268 output path. The BIST test is performed after a reset to ensure the component is in a known state. During BIST , data from an internal pseudo-random noise (PN) source starts at the ADC block output and is driven through the digital data path of two channels. At the data path output, CRC logic calculates a signature based on the data. The BIST sequence runs for 512 cycles and then stops. Once complete, BIST compares the signature result with a predetermined value. If the signature matches, BIST sets bit 0 of register 0x24 , indicating a pass. If the BIST test fails, bit 0 of register 0x24 is cleared. During this test, the output pins are connected, so the PN sequence can be observed running through the data output pins. Writing the value 0x05 to register 0x0E runs BIST . This enables bit 0 of register 0x0E (BIST enabled) and resets the PN sequence generator, bit 2 of register 0x0E (BIST INIT). Bit 0 of register 0x24 is automatically cleared when BIST completes . The PN sequence can be continued from the last value by writing 0 to bit 2 of register 0x0E . However, if the PN sequence is not reset, the signature calculation will not equal the predetermined value at the end of the test. In this case, the user needs to rely on the verification output data.

- **Output test mode**

Table 11 describes the output test options at address 0x0D . When output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end block, and the test mode runs via the output formatting block. Some test modes are constrained by the output format, while others are not. The PN generator from the PN sequence test can be reset by setting bit 4 or bit 5 of register 0x0D . These tests may or may not use analog signals (if present, analog signals are ignored), but a normal sampling clock input is required.

9. Serial Port Interface (SPI)

ADCP9268 Serial Port Interface (SPI) allows users to configure the corresponding internal function registers of the ADC to meet specific functional and operational needs. The serial port allows access to and reading from the address space. The ADC's SPI consists of three parts: the SCLK pin, the SDIO pin, and the CSB pin. The SCLK (Serial Clock) pin is used to synchronize the ADC's read and write data; the SDIO (Serial Data Input / Output) dual-function pin allows data to be sent to or read from internal registers; the CSB (Chip Select) pin is an active-low control pin that enables or disables read/write cycles. Timing requirements are shown in Figure 4 .

Table 11. Register List

Address (HEX)	Register name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default value (HEX)	Notes
0x00	Port configuration	0	LSBfirst	Soft reset	1	1	Soft reset	LSB first	0	0x18	LSB or MSB mode register
0x01	Chip ID	chip ID 0x32								0x32	ID used to distinguish devices ; read-only.
0x02	Chip level		001 = 125 MSPS 010 = 105 MSPS 011 = 80 MSPS								ID that distinguishes the device ; read-only.
0x05	Channel selection							Data Channel B	Data Channel A	0x03	This determines which channel on the chip will receive the next write command; the default value is all channels on the chip.
0x08	Model	External Power-down enable	External pin function 0x00full power-down 0x01 standby					00 = chip run 01 = full power-down 10 = standby 11 = digital reset		0x80	Determine the various general modes of chip operation
0x0B	Clock division						Clock divider ratio [2:0] 000 = divided by 1 001 = divided by 1 010 = divided by 2 011 = divided by 3 100 = divided by 4 101 = divided by 5			0x00	

							110 = divided by 6 111 = divided by 7		

Address (HEX)	Register name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default value (HEX)	Notes
0x0D	Test mode	User input test mode 00=single 01=alternative 10=single once 11=alternate once		Reset PN long sequence	Reset PN short sequence	Output test mode: 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = one/ zero word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1x sync 1011 = one bit high 1100 = mixed bit frequency				0x00	After configuration, the test data is placed on the output pin instead of the normal data.
0x0E	BIST enable						BIST INIT		BIST enable	0x00	Whether to enable the BIST function
0x0F	ADC_I NPUT								Common mode servo enable	0x00	
0x10	Offset adjustment	8-bit device offset adjustment [7:0] Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	Offset fine-tuning
0x14	ADC output mode	Drive Strength 0 = ANSI LVDS; 1 = reduced swing LVDS	Output Type 0 = CMOS 1=LVDS	CMOS Output Interleaved enable	Output disable		Output Invert	00=offset binary 01=twos complement 10 = gray code 11 = offset binary		0x00	Configure output and data format
0x16	Output phase	DCO output polarity 0= normal 1= inverted					Input clock adjust phase [2:0] (Value is number of input clock cycles of phase delay) 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles			0x00	On devices using global clock division, determine which phase of the divider output is used to provide the output clock; the internal latch remains unaffected.

www.dsown.com
Email：info@dsown.com

							111 = 7 input clock cycles		
0x17	Output delay		DATA_Delay 000 = 0.29 ns 001 = 0.58 ns 010 = 0.87 ns 011 = 1.16 ns 100 = 1.45 ns 101 = 1.74 ns 110 = 2.03 ns 111 = 2.32 ns				DCO_Delay 000 = 0.29 ns 001 = 0.58 ns 010 = 0.87 ns 011 = 1.16 ns 100 = 1.45 ns 101 = 1.74 ns 110 = 2.03 ns 111 = 2.32 ns	0x00	This sets a fine output delay for the output clock, but does not change the internal timing.

Address (HEX)	Register name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default value (HEX)	Notes
0x19	USER_ PATT1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined mode, 1 LSB
0x1A	USER_ PATT1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined mode, 1MSB
0x1B	USER_ PATT2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined mode, 2 LSB
0x1C	USER_ PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined mode, 2 MSB
0x24	MISR_LSB								B0	0x00	The least significant byte of MISR ; read-only
0x2A	Feature								OR Output Enable	0x01	Disable the OR pin of the index channel
0x2E	Output allocation								0=ADC A 1=ADC B	ChA = 0x00 ChB = 0x01	Assign the ADC to the output channel
0x100	Sync control						Clock Divider Next Sync only	Clock Divider Sync enable	Master Sync enable	0x01	
0x101	USR2	Enable OEB Pin 47								0x80	

10. Application Information

- **Power supply and grounding recommendations**

It is recommended to use two independent power supplies for the ADCP9268: one for the analog power supply AVDD and one for the digital output power supply DRVDD. For AVDD and DRVDD, multiple different decoupling capacitors should be used to shield against high-frequency and low-frequency noise. The decoupling capacitors should be placed close to the device pins, and trace lengths should be minimized. The ADCP9268 requires only one PCB ground plane. Optimal performance can be easily achieved through proper decoupling and clever separation of the PCB analog, digital, and clock modules.

- **Recommendations for exposed pad heat sinks**

To achieve optimal electrical and thermal performance, the exposed pads on the bottom of the ADC must be connected to analog ground (AGND). The exposed continuous copper plane on the PCB should match the exposed pads of the ADCP9268. Multiple vias should be present on the copper plane to provide the lowest possible thermal resistance path for heat dissipation through the bottom of the PCB. These vias should be filled or blocked to prevent solder bleed-through, which could affect connectivity. To maximize coverage and connection between the ADC and the PCB , a silkscreen layer should be applied to the PCB to divide the continuous plane into multiple equal sections. This provides multiple connection points between the ADC and the PCB during reflow soldering. A continuous, undivided plane, on the other hand, only guarantees one connection point between the ADC and the PCB.

- **VCM**

The VCM pin should be decoupled to ground via a 0.1uF capacitor.

- **RBIAS**

The ADCP9268 requires a 10kΩ resistor placed between the RBIAS pin and ground. This resistor is used to set the main reference current of the ADC core and has a tolerance of at least 1%.

- **Reference voltage source decoupling**

The VREF pin should be decoupled to ground via a parallel connection of an external 0.1uF low-ESR ceramic capacitor and a 1.0uF low-ESR capacitor.

- **SPI port**

The SPI port should be disabled when the converter needs to fully utilize its dynamic performance. Typically, the SCLK , CSB , and SDIO signals are asynchronous with the ADC clock; therefore, noise in these signals can degrade converter performance. If other devices use the on-board SPI bus, a buffer may be needed between this bus and the ADCP9268 to prevent these signals from changing at the converter input during critical sampling periods.

11. Package Outline Dimensions

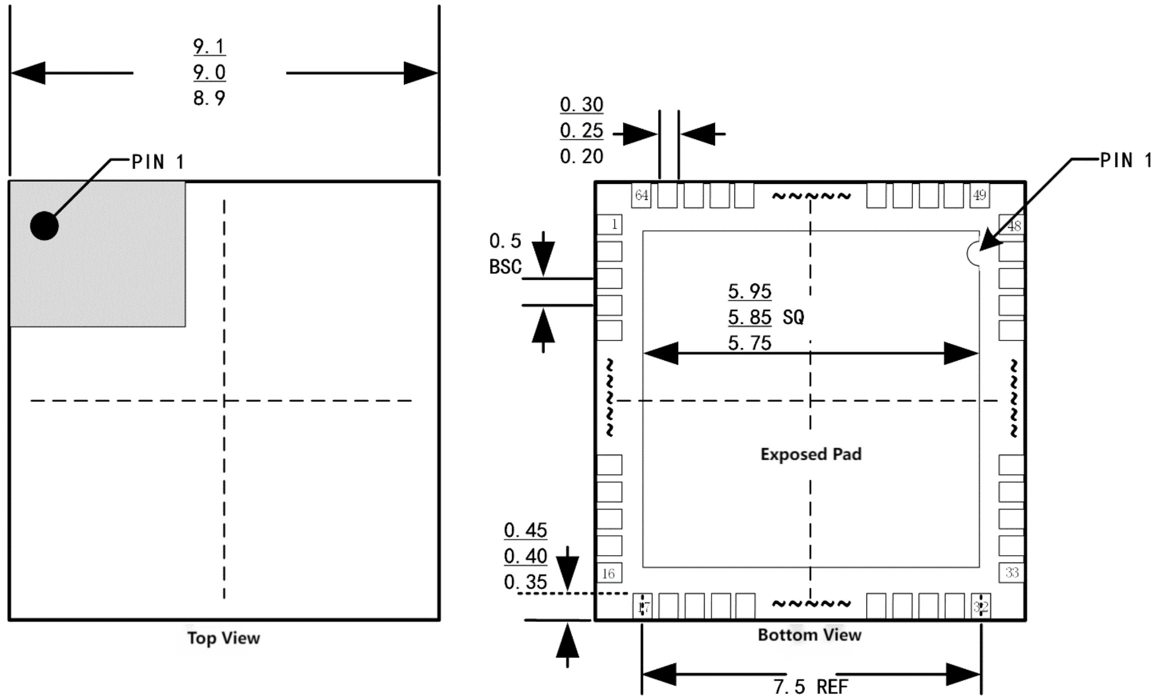


Figure 21. ADCP9268-80/105/125 Package Outline Dimensions.

Note: All dimensions are in mm.

12. Ordering Information

Model	Temperature Range	Packaging Type	Package
ADCP9268-125	-40℃ to 85℃	64-QFN	260/reel
ADCP9268-105	-40℃ to 85℃	64-QFN	260/reel
ADCP9268-80	-40℃ to 85℃	64-QFN	260/reel

www.dsown.com
Email：info@dsown.com