# ADCP9253E-125/105/80 4-Channal, 14-Bit, Serial LVDS 1.8V ADC

## Features:

- 1.8V power supply
- Low power consumption: 120mW per channel (125/105/80MSPS)
- Signal-to-noise ratio (SNR):

  74dBFS (70MHz, 2.0V pp input range)

  75dBFS (70MHz, 2.6V pp input range)
- SFDR: 88dBc (to Nyquist, 2.0V pp input range)
- DNL: ±0.7LSB; INL: ±2LSB (2.0V pp input range)
- Serial LVDS, low power consumption, narrowing range options
- 650MHz full-power analog bandwidth
- 2V pp input voltage range (supports up to 2.6V pp)
- Serial port control

## Applications:

- Medical ultrasound and MRI
- Orthogonal radio receiver
- Diversity radio receiver
- Test equipment

## Product Description:

The ADCP9253E-x is a 4-channel, 14-bit, 125/105/80MSPS analog-to-digital converter (ADC) with on-chip sample-and-hold circuitry, specifically designed for low cost, low power consumption, small size, and ease of use. Offering conversion rates up to 125MSPS, it features excellent dynamic performance and low power consumption, making it suitable for applications where small package size is critical. This ADC requires a single 1.8V supply and an LVPECL/CMOS/LVDS compatible sampling rate clock signal to fully realize its performance. It meets the needs of many applications without requiring an external reference voltage source or driver. The ADC automatically multiplies the sampling rate clock to generate an appropriate LVDS serial data rate. It provides a Data Clock Output (DCO) for capturing data at the output and a Frame Clock Output (FCO) for sending new output bytes. It also supports independent channel shutdown; typical power consumption is less than 2mW when all channels are disabled. The ADC incorporates various features to optimize device flexibility and minimize system cost, such as programmable output clock and data alignment, and generation of digital test codes. Available digital test codes include built-in fixed codes and pseudo-random codes, as well as user-defined test codes input via the serial port interface (SPI).

## Characteristics:

Small size, integrating four ADCs in a compact package, saving space. Low power consumption: 120mW per channel (125/105/80MSPS, power option adjustable). Data clock output (DCO) operates at frequencies up to 500 MHz, supporting Double Data Rate (DDR) operation. SPI control provides rich and flexible features to meet the needs of various specific systems. The chip is suitable for the entire industrial range (-55°C to +125°C) and is packaged in a QFN package.

## Functional Block Diagram:

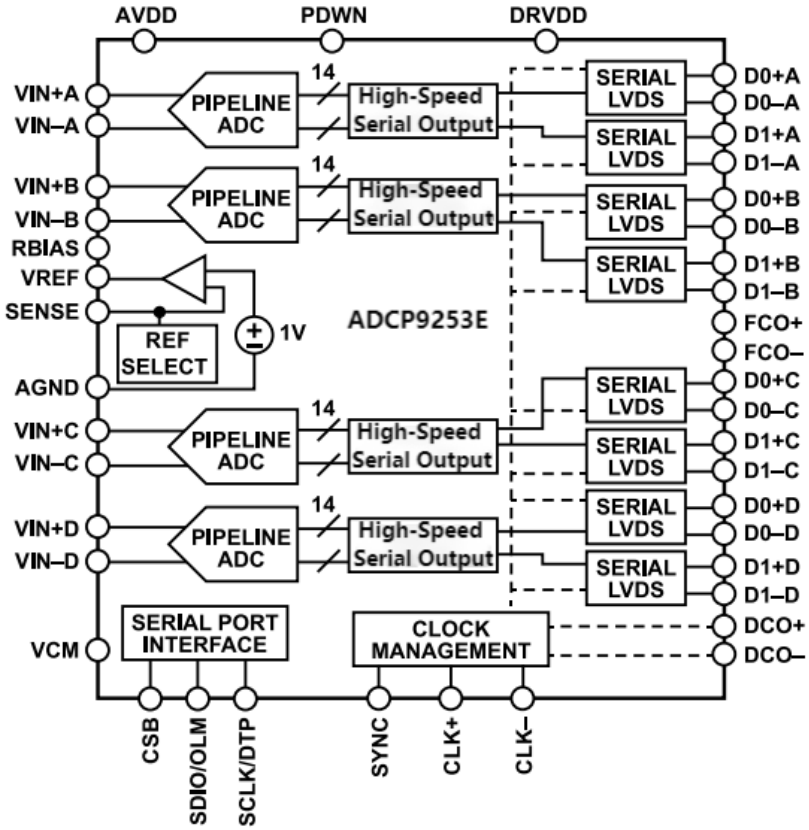



Figure1. Functional Block Diagram

## Absolute Maximum Ratings

Unless otherwise stated, operate within the room temperature range (1).

| | Rated value | Unit |
|---|---|---|
| AVDD to AGND | -0.3 to +2.0 | V |
| DRVDD to AGND | -0.3 to +2.0 | V |
| Digital outputs (D0±x, D1±x, DCO+, DCO - , FCO + , FCO - ) to AGND | -0.3 to +2.0 | V |
| CLK+, CLK- to AGND | -0.3 to +2.0 | V |
| AVIN+x, VIN-x to ANGD | -0.3 to +2.0 | V |
| SCLK/DTP, SDIO/OLM, CSB to AGND | -0.3 to +2.0 | V |
| SYNC, PDWN to AGND | -0.3 to +2.0 | V |
| RBIAS to AGND | -0.3 to +2.0 | V |
| VREF, SENSE to AGND | -0.3 to +2.0 | V |
| Operating temperature (ambient temperature, Vref = 1.0V) | -55 to +125 | ℃ |
| Operating temperature (ambient temperature, Vref = 1.3V) | -55 to +125 | ℃ |
| Maximum junction temperature | 150 | ℃ |
| Pin temperature (soldering, 10 seconds) | 300 | ℃ |
| Storage temperature (ambient temperature) | -65 to +150 | ℃ |

(1) Stress exceeding these ratings may cause permanent damage. Prolonged exposure to absolute maximum conditions may reduce the reliability of the equipment. These are only stress ratings and do not imply functional operation of the equipment under these conditions or any other conditions exceeding the specified conditions.

## Electrical Characteristics

**DC specifications**

Unless otherwise noted, the full-scale differential input is 2.0Vp-p when AVDD=1.8V, DRVDD=1.8V, −1.0dBFS; $V_{REF}$=1.0V, DCS off.

**Table 1:**

| Parameter | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Resolution | | | 14 | | Bit |
| Accuracy | | | | | |
| No missing codes | Full | | Guaranteed | | |
| Offset error | Full | -0.49 | -0.3 | 0.17 | %FSR |
| Mismatch | Full | -0.14 | +0.2 | 0.39 | %FSR |
| Gain error | Full | - 8 | -5 | 2.37 | %FSR |
| Gain Matching | Full | 1.0 | 1.1 | 1.5 | %FSR |
| Differential Nonlinearity (DNL) | Full | -0.77 | | 0.95 | LSB |
| | 25℃ | | ±0.7 | | LSB |
| Integral nonlinearity (INL) | Full | - 4 | | 4 | LSB |
| | 25℃ | | ±3.5 | | LSB |
| Temperature drift | | | | | |
| Offset error | Full | | 3.5 | | ppm/℃ |
| Internal reference voltage source | | | | | |
| Output voltage (1.0V mode) | Full | 0.98 | 1.0 | 1.01 | V |
| Load regulation at 1.0mA (Vref = 1.0V) | Full | | 2 | | mV |
| Input resistance | 25℃ | | 7.5 | | kΩ |
| Input noise | | | | | |
| Vref = 1.0V | 25℃ | | 2.7 | | LSB rms |
| Analog Input | | | | | |
| Differential input voltage (Vref = 1.0V) | Full | | 2 | | V pp |
| Common mode voltage | Full | | 0.9 | | V |
| Common mode range | 25℃ | 0.5 | | 1.3 | V |
| Differential input resistor | 25℃ | | 2.6 | | kΩ |
| Differential input capacitor | 25℃ | | 7 | | pF |
| power supply | | | | | |
| AVDD | Full | 1.7 | 1.8 | 1.9 | V |
| DRVDD | Full | 1.7 | 1.8 | 1.9 | V |
| $I_{AVDD}$ [1] | Full | | 305 | 330 | mA |
| $I_{DRVDD}$ (ANSI-644 mode) | Full | | 60 | 64 | mA |
| $I_{DRVDD}$ (Zoom-out mode) | 25℃ | | 45 | | mA |
| Total power consumption | | | | | |
| DC input | Full | | 607 | 649 | mW |
| Sine wave input (four channels, including output driver, ANSI-644 mode) | Full | | 657 | 780 | mW |
| Sine wave input (four channels, including output driver, narrowing range mode) | 25℃ | | 630 | | mW |
| Turn off | 25℃ | | 2 | | mW |
| Standby [2] | Full | | 356 | 392 | mW |

(1) Measurement conditions: All four channels use full-scale sine waves with low input frequency.

(2) It can be controlled via SPI.

## Electrical Characteristics (continued)

**DC specifications**

Unless otherwise noted, the full-scale differential input is 2.0Vp-p when AVDD=1.8V, DRVDD=1.8V, −1.0dBFS; $V_{REF}$=1.0V, DCS off.

**Table 2:**

| Parameter | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Resolution | | | 14 | | Bit |
| Accuracy | | | | | |
| No missing codes | 25℃ | | Guaranteed | | |
| Offset error | 25℃ | | -0.3 | | %FSR |
| Mismatch | 25℃ | | +0.2 | | %FSR |
| Gain error | 25℃ | | -5 | | %FSR |
| Gain Matching | 25℃ | | 1.1 | | %FSR |
| Differential Nonlinearity (DNL) | 25℃ | | ±0.8 | | LSB |
| Integral nonlinearity (INL) | 25℃ | | ±5.0 | | LSB |
| Temperature drift | | | | | |
| Offset error | 25℃ | | 3.5 | | ppm/℃ |
| Internal reference voltage source | | | | | |
| Output voltage (1.3V mode) | 25℃ | | 1.3 | | V |
| Load regulation at 1.0mA (Vref = 1.3V) | 25℃ | | 6.5 | | mV |
| Input resistance | 25℃ | | 7.5 | | kΩ |
| Input noise | | | | | |
| Vref = 1.3V | 25℃ | | 2.1 | | LSB rms |
| Analog Input | | | | | |
| Differential input voltage (Vref = 1.3V) | 25℃ | | 2.6 | | V pp |
| Common mode voltage | 25℃ | | 0.9 | | V |
| Common mode range | 25℃ | 0.6 | | 1.3 | V |
| Differential input resistor | 25℃ | | 2.6 | | kΩ |
| Differential input capacitor | 25℃ | | 7 | | pF |
| power supply | | | | | |
| AVDD | 25℃ | | 1.8 | | V |
| DRVDD | 25℃ | | 1.8 | | V |
| $I_{AVDD}$ [1] | 25℃ | | 314 | | mA |
| $I_{DRVDD}$ (ANSI-644 mode) | 25℃ | | 60 | | mA |
| $I_{DRVDD}$ (Zoom-out mode) | 25℃ | | 45 | | mA |
| Total power consumption | | | | | |
| DC input | 25℃ | | 614 | | mW |
| Sine wave input (four channels, including output driver, ANSI-644 mode) | 25℃ | | 673 | | mW |
| Sine wave input (four channels, including output driver, narrowing range mode) | 25℃ | | 646 | | mW |
| Turn off | 25℃ | | 2 | | mW |
| Standby [2] | 25℃ | | 371 | | mW |

(1) Measurement conditions: All four channels use full-scale sine waves with low input frequency.

(2) It can be controlled via SPI.

## Electrical Characteristics (continued)

**Communication Specifications**

Unless otherwise noted, the full-scale differential input is 2.0Vp-p when AVDD=1.8V, DRVDD=1.8V, −1.0dBFS; $V_{REF}$=1.0V, DCS off.

**Table 3:**

| Parameter | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Signal-to-noise ratio (SNR) | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | 75.5 | | dBFS |
| $f_{IN}$ = 15MHz | 25℃ | | 75.3 | | dBFS |
| $f_{IN}$ = 70MHz | Full | 73 | 74 | | dBFS |
| $f_{IN}$ = 128MHz | 25℃ | | 71.4 | | dBFS |
| $f_{IN}$ = 200MHz | 25℃ | | 7 0 | | dBFS |
| SINAD | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | 78 | | dBFS |
| $f_{IN}$ = 15MHz | 25℃ | | 77.7 | | dBFS |
| $f_{IN}$ = 70MHz | Full | 74.6 | 76.1 | | dBFS |
| $f_{IN}$ = 128MHz | 25℃ | | 73.6 | | dBFS |
| $f_{IN}$ = 200MHz | 25℃ | | 70.3 | | dBFS |
| Significant digits (ENOB) | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | 12.7 | | Bits |
| $f_{IN}$ = 15MHz | 25℃ | | 12.6 | | Bits |
| $f_{IN}$ = 70MHz | Full | 12.1 | 12.4 | | Bits |
| $f_{IN}$ = 128MHz | 25℃ | | 11.9 | | Bits |
| $f_{IN}$ = 200MHz | 25℃ | | 11.4 | | Bits |
| Spurious-free dynamic range (SFDR) | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | 95 | | dBc |
| $f_{IN}$ = 15MHz | 25℃ | | 92 | | dBc |
| $f_{IN}$ = 70MHz | Full | 77 | 88 | | dBc |
| $f_{IN}$ = 128MHz | 25℃ | | 86 | | dBc |
| $f_{IN}$ = 200MHz | 25℃ | | 76 | | dBc |
| Worst harmonic (second or third) | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | -98 | | dBc |
| $f_{IN}$ = 15MHz | 25℃ | | -93 | | dBc |
| $f_{IN}$ = 70MHz | Full | -78 | -89 | | dBc |
| $f_{IN}$ = 128MHz | 25℃ | | -87 | | dBc |
| $f_{IN}$ = 200MHz | 25℃ | | -77 | | dBc |
| Worst case: other harmonics or strays | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | -96 | | dBc |
| $f_{IN}$ = 15MHz | 25℃ | | -98 | | dBc |
| $f_{IN}$ = 70MHz | Full | -85 | -94 | | dBc |
| $f_{IN}$ = 128MHz | 25℃ | | -89 | | dBc |
| $f_{IN}$ = 200MHz | 25℃ | | -83 | | dBc |
| Intermodulation distortion (IMD) – AIN1 and AIN2 = -7.0 dBFS | | | | | |
| $f_{IN1}$ = 70.5MHz, $f_{IN2}$ = 72.5MHz | 25℃ | | -90 | | dBc |
| Crosstalk [1] | 25℃ | | 91 | | dB |
| Crosstalk (over-range condition) [2] | 25℃ | | 87 | | dB |
| Power Supply Rejection Ratio (PSRR) [3] | | | | | |
| AVDD | 25℃ | | 31 | | dB |
| DRVDD | 25℃ | | 79 | | dB |
| Analog input bandwidth (full power) | 25℃ | | 650 | | MHz |

(1) Measurement conditions for crosstalk: One channel has a parameter of 70MHz, -1.0dBFS analog input and no input signal on adjacent channels.

(2) The over-range condition is defined as the input being 3dB higher than the full scale.

(3) PSRR measurement method: Inject a 10MHz sine wave signal into the power pin, and measure the output spurious of the FFT. PSRR is equal to the amplitude of the spurious voltage divided by the pin voltage, and is expressed in decibels (dB).

## Electrical Characteristics (continued)

**Communication Specifications**

Unless otherwise noted, the full-scale differential input is 2.0Vp-p when AVDD=1.8V, DRVDD=1.8V, −1.0dBFS; $V_{REF}$=1.3V, DCS off.

**Table 4:**

| Parameter | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Signal-to-noise ratio (SNR) | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | 77.5 | | dBFS |
| $f_{IN}$ = 15MHz | 25℃ | | 77 | | dBFS |
| $f_{IN}$ = 70MHz | Full | | 75 | | dBFS |
| $f_{IN}$ = 128MHz | 25℃ | | 72 | | dBFS |
| $f_{IN}$ = 200MHz | 25℃ | | 69.8 | | dBFS |
| SINAD | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | 79.8 | | dBFS |
| $f_{IN}$ = 15MHz | 25℃ | | 79.2 | | dBFS |
| $f_{IN}$ = 70MHz | Full | | 76.1 | | dBFS |
| $f_{IN}$ = 128MHz | 25℃ | | 74 | | dBFS |
| $f_{IN}$ = 200MHz | 25℃ | | 69.9 | | dBFS |
| Significant digits (ENOB) | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | 13 | | Bits |
| $f_{IN}$ = 15MHz | 25℃ | | 12.9 | | Bits |
| $f_{IN}$ = 70MHz | Full | | 12.3 | | Bits |
| $f_{IN}$ = 128MHz | 25℃ | | 12 | | Bits |
| $f_{IN}$ = 200MHz | 25℃ | | 11.3 | | Bits |
| Spurious-free dynamic range (SFDR) | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | 93 | | dBc |
| $f_{IN}$ = 15MHz | 25℃ | | 93 | | dBc |
| $f_{IN}$ = 70MHz | Full | | 81 | | dBc |
| $f_{IN}$ = 128MHz | 25℃ | | 85 | | dBc |
| $f_{IN}$ = 200MHz | 25℃ | | 74 | | dBc |
| Worst harmonic (second or third) | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | -94 | | dBc |
| $f_{IN}$ = 15MHz | 25℃ | | -94 | | dBc |
| $f_{IN}$ = 70MHz | Full | | -82 | | dBc |
| $f_{IN}$ = 128MHz | 25℃ | | -87 | | dBc |
| $f_{IN}$ = 200MHz | 25℃ | | -75 | | dBc |
| Worst case: other harmonics or strays | | | | | |
| $f_{IN}$ = 9.7MHz | 25℃ | | -100 | | dBc |
| $f_{IN}$ = 15MHz | 25℃ | | -99 | | dBc |
| $f_{IN}$ = 70MHz | Full | | -96 | | dBc |
| $f_{IN}$ = 128MHz | 25℃ | | -86 | | dBc |
| $f_{IN}$ = 200MHz | 25℃ | | -84 | | dBc |
| Intermodulation distortion (IMD) – AIN1 and AIN2 = -7.0 dBFS | | | | | |
| $f_{IN1}$ = 70.5MHz, $f_{IN2}$ = 72.5MHz | 25℃ | | -90 | | dBc |
| Crosstalk [1] | 25℃ | | 91 | | dB |
| Crosstalk (over-range condition) [2] | 25℃ | | 87 | | dB |
| Power Supply Rejection Ratio (PSRR) [3] | | | | | |
| AVDD | 25℃ | | 31 | | dB |
| DRVDD | 25℃ | | 79 | | dB |
| Analog input bandwidth (full power) | 25℃ | | 650 | | MHz |

(1) Measurement conditions for crosstalk: One channel has a parameter of 70MHz, -1.0dBFS analog input and no input signal on adjacent channels.

(2) The over-range condition is defined as the input being 3dB higher than the full scale.

(3) PSRR measurement method: Inject a 10MHz sine wave signal into the power pin, and measure the output spurious of the FFT. PSRR is equal to the amplitude of the spurious voltage divided by the pin voltage, and is expressed in decibels (dB).

## Digital Specifications

Unless otherwise noted, AVDD=1.8V, DRVDD=1.8V.

**Table 5:**

| Parameter | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock input (CLK+, CLK-) | | | | | |
| Logical compatibility | | | CMOS/LVDS/LVPECL | | |
| Differential input voltage [1] | Full | 0.2 | | 3.6 | V pp |
| Input voltage range | Full | AGND − 0.2 | | AGND + 0.2 | V |
| Input common mode voltage | Full | | 0.9 | | V |
| Input resistance (differential) | 25℃ | | 15 | | V |
| Input capacitor | 25℃ | | 4 | | pF |
| Logical inputs (PDWN, SYNC, SCLK) | | | | | |
| Logic 1 voltage | Full | 1.2 | | AVDD + 0.2 | V |
| Logic 0 voltage | Full | 0 | | 0.8 | V |
| Input resistance | 25℃ | | 30 | | kΩ |
| Input capacitor | 25℃ | | 2 | | pF |
| Logical Input (CSB) | | | | | |
| Logic 1 voltage | Full | 1.2 | | AVDD + 0.2 | V |
| Logic 0 voltage | Full | 0 | | 0.8 | V |
| Input resistance | 25℃ | | 26 | | kΩ |
| Input capacitor | 25℃ | | 2 | | pF |
| Logical Input (SDIO) [2] | | | | | |
| Logic 1 voltage | Full | 1.2 | | AVDD + 0.2 | V |
| Logic 0 voltage | Full | 0 | | 0.8 | V |
| Input resistance | 25℃ | | 26 | | kΩ |
| Input capacitor | 25℃ | | 5 | | pF |
| SDIO (Logical Output) | | | | | |
| Logic 1 voltage ($I_{OH}$ = 800μA) | Full | | 1.79 | | V |
| Logic 0 voltage ($I_{OL}$ = 50μA) | Full | | | 0.05 | V |
| Digital outputs (D0±x, D1±x), ANSI-644 | | | | | |
| Logical compatibility | | | LVDS | | |
| Differential output voltage ($V_{OD}$) | Full | 290 | 345 | 400 | mV |
| Output offset voltage ($V_{OS}$) | Full | 1.15 | 1.25 | 1.35 | V |
| Output encoding (default) | | | Binary two's complement | | |
| Digital outputs (D0±x, D1±x), low power consumption, reduced signal options | | | | | |
| Logical compatibility | | | LVDS | | |
| Differential output voltage ($V_{OD}$) | Full | 160 | 200 | 230 | mW |
| Output offset voltage ($V_{OS}$) | Full | 1.15 | 1.25 | 1.35 | mW |
| Output encoding (default) | | | Binary two's complement | | V |

(1) Only for LVDS and LVPECL.

(2) For the 13 SDIO/OLM pins that share the same connection.

## Switch Specifications

Unless otherwise specified, AVDD=1.8V, DRVDD=1.8V.

**Table 6:**

| Parameter | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock [1] | | | | | |
| Input clock rate | Full | 20 | | 1000 | MHz |
| Conversion rate | Full | 20 | | 125 | MSPS |
| Clock high-level pulse width ( $t_{EH}$ ) | Full | | 4.00 | | ns |
| Clock low-level pulse width ( $t_{EL}$ ) | Full | | 4.00 | | ns |
| Output parameter [1] | | | | | |
| Propagation delay ( $t_{PD}$ ) | Full | | 2.3 | | ns |
| Rise time ( $t_R$ ) (20% to 80%) | Full | | 300 | | ps |
| Fall time ( $t_F$ ) (20% to 80%) | Full | | 300 | | ps |
| FCO propagation delay ( $t_{FCO}$ ) | Full | 1.5 | 2.3 | 3.1 | ns |
| DCO propagation delay ($t_{CPD}$) [2] | Full | | $t_{FCO}$ + ($t_{SAMPLE}$ / 14) | | ns |
| DCO to data delay ($t_{DATA}$) [2] | Full | ($t_{SAMPLE}$ / 14) - 300 | ($t_{SAMPLE}$ / 14) | ($t_{SAMPLE}$ / 14) + 300 | ps |
| DCO to FCO delay ($t_{FRAME}$) [2] | Full | ($t_{SAMPLE}$ / 14) - 300 | ($t_{SAMPLE}$ / 14) | ($t_{SAMPLE}$ / 14) + 300 | ps |
| Channel delay ( $t_{LD}$ ) | | | 90 | | ps |
| Data to data skew ($t_{DATA-MAX}$) − $t_{DATA-MIN}$ ) | Full | | ±50 | ±200 | ps |
| Wake-up time (standby) | 25℃ | | 250 | | ns |
| Wake-up time (power saving mode) [3] | 25℃ | | 375 | | μs |
| Pipeline delay | Full | | 16 | | clock cycle |
| Aperture | | | | | |
| Aperture delay ( $t_A$ ) | 25℃ | | 1 | | ns |
| Aperture uncertainty (jitter, $t_J$ ) | 25℃ | | 135 | | fs rms |
| Out-of-range recovery time | 25℃ | | 1 | | clock cycle |

(1) It can be adjusted via SPI. The conversion rate refers to the clock rate after frequency division.

(2) $t_{SAMPLE}$ / 14 is based on the number of bits in the two LVDS data channels. $t_{SAMPLE} = 1/f_s$.

(3) Wake-up time refers to the time required to return from power saving mode to normal working mode.

## Timing Specification

**Table 7:**

| Parameter | Description | Limit | Unit |
|---|---|---|---|
| Synchronization timing requirements | | | |
| $t_{SSYNC}$ | Setup time from SYNC to CLK+ rising edge | 0.24 | ns (typical value) |
| $t_{HSYNC}$ | Hold time from the rising edge of SYNC to CLK+ | 0.40 | ns (typical value) |
| SPI Timing Requirements | | | |
| $t_{DS}$ | Setup time between data and the rising edge of SCLK | 2 | ns (minimum value) |
| $t_{DH}$ | Hold time between data and the rising edge of SCLK | 2 | ns (minimum value) |
| $t_{CLK}$ | SCLK cycle | 40 | ns (minimum value) |
| $t_{S}$ | Establishment time between CSB and SCLK | 2 | ns (minimum value) |
| $t_{H}$ | The duration of the hold between CSB and SCLK | 2 | ns (minimum value) |
| $t_{HIGH}$ | SCLK high-level pulse width | 10 | ns (minimum value) |
| $t_{LOW}$ | SCLK low-level pulse width | 10 | ns (minimum value) |
| $t_{EN\_SDIO}$ | The time required for an SDIO pin to switch from an input state to an output state relative to the falling edge of SCLK. | 10 | ns (minimum value) |
| $t_{DIS\_SDIO}$ | The time required for an SDIO pin to switch from an output state to an input state relative to the rising edge of SCLK. | 10 | ns (minimum value) |

## Timing Diagram

For SPI register settings, see the " Memory Mapped Registers Description " section and Table 23.

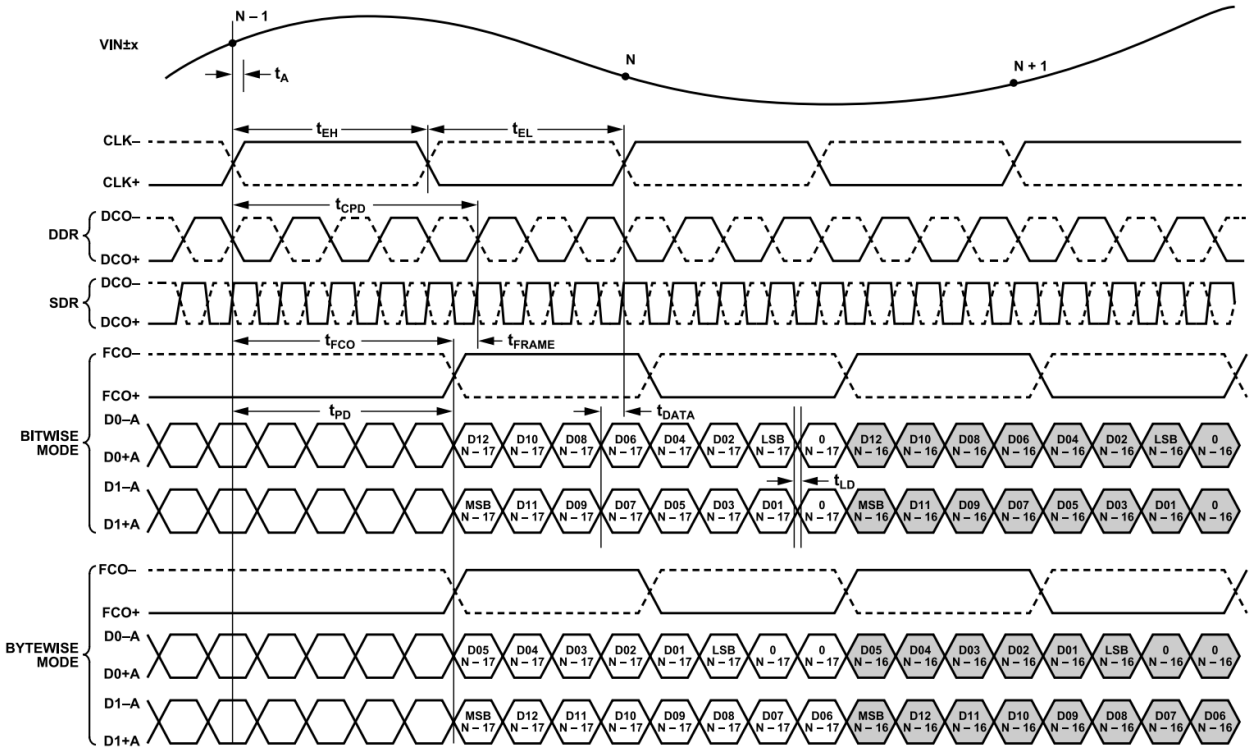



Figure 2. 16-Bit DDR/SDR, Dual Channel, 1x Frame Mode (Default)

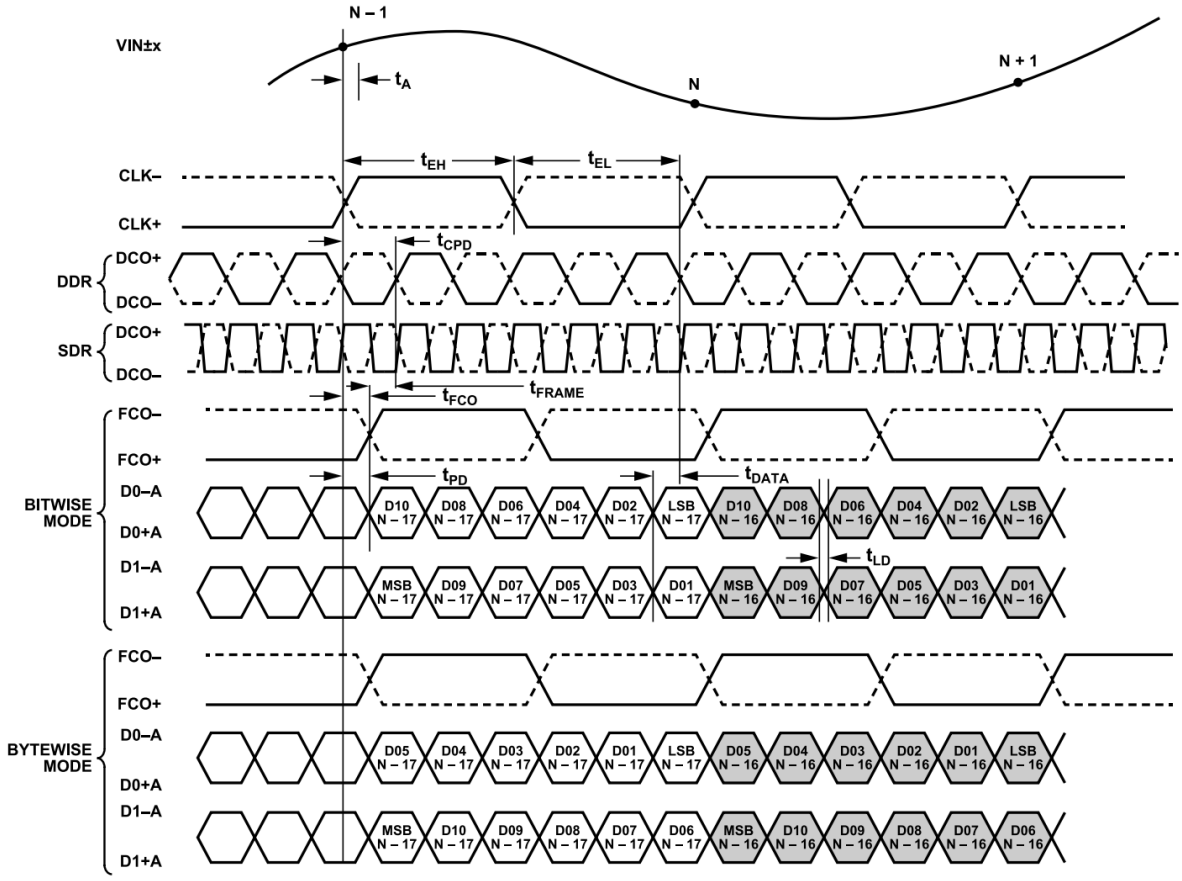



Figure 3. 12-Bit DDR/SDR, Dual Channel, 1x Frame Mode

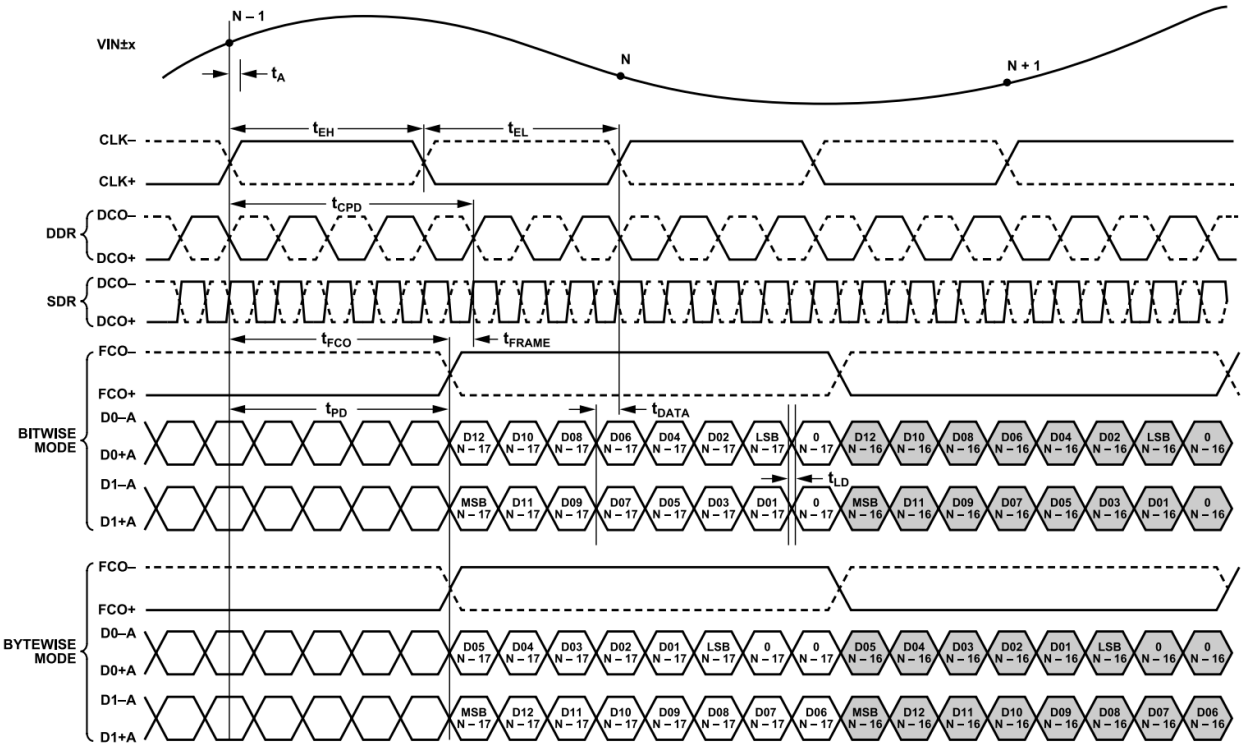



Figure 4. 16-Bit DDR/SDR, Dual Channel, 2x Frame Mode

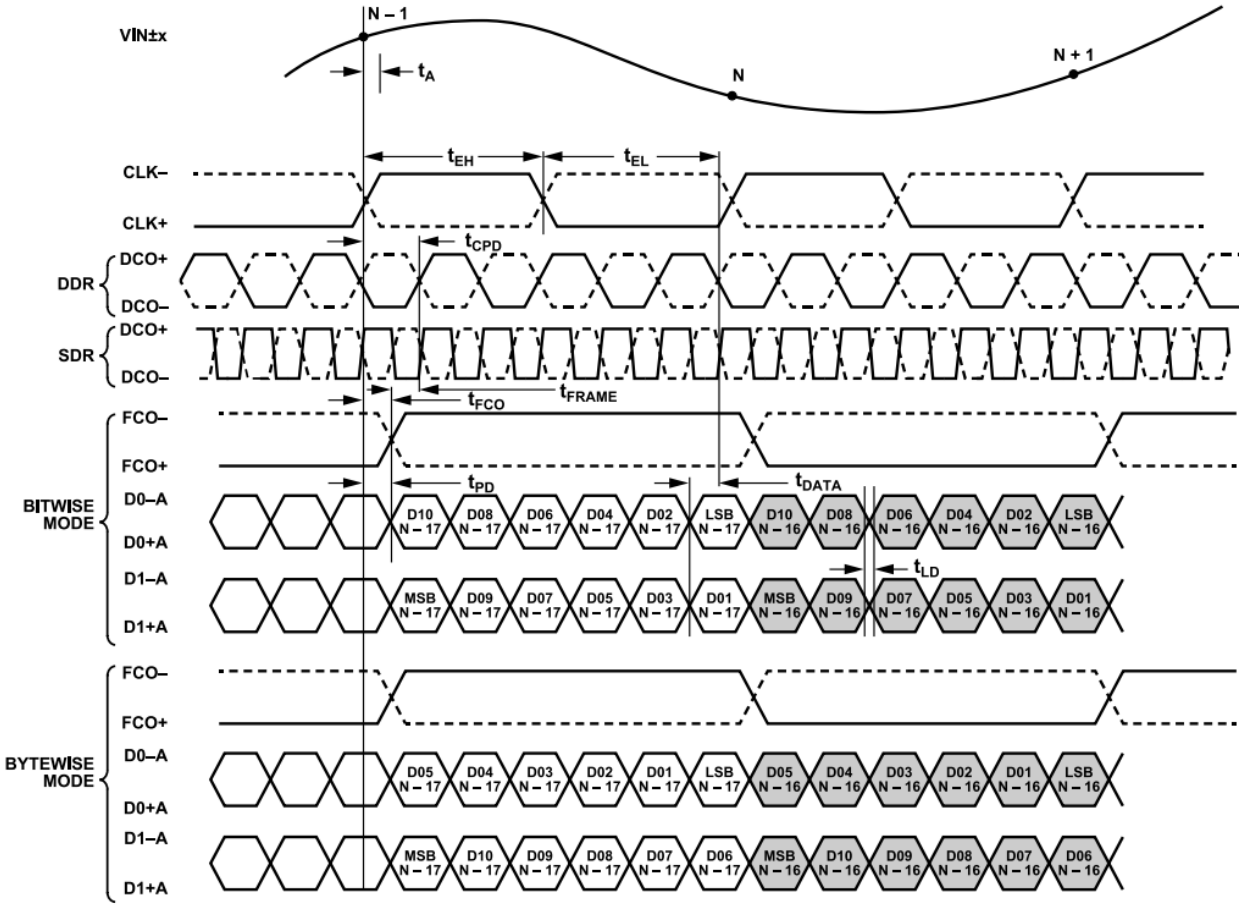



Figure 5. 12-Bit DDR/SDR, Dual Channel, 2x Frame Mode

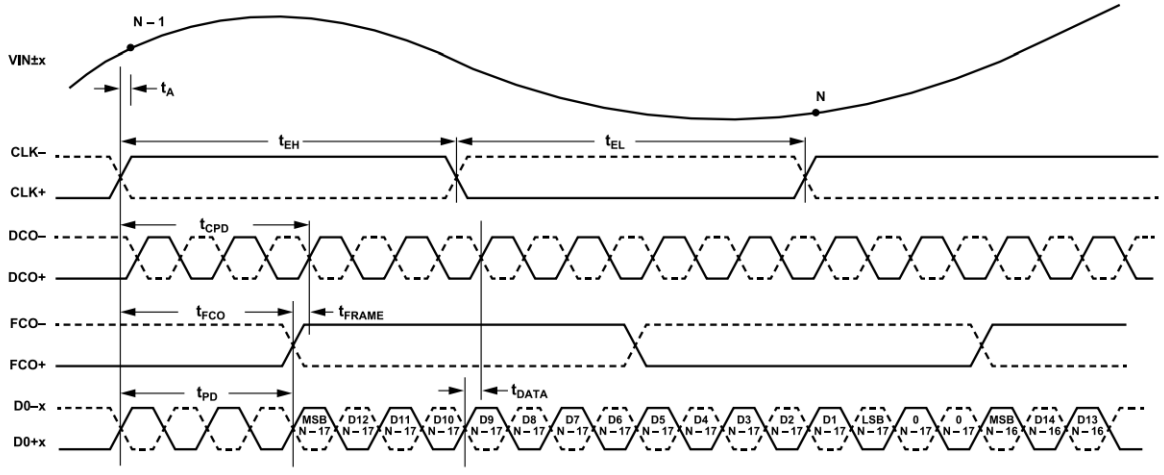



Figure 6. Byte-by-byte DDR, single-channel, 1x-frame, 16-bit output mode

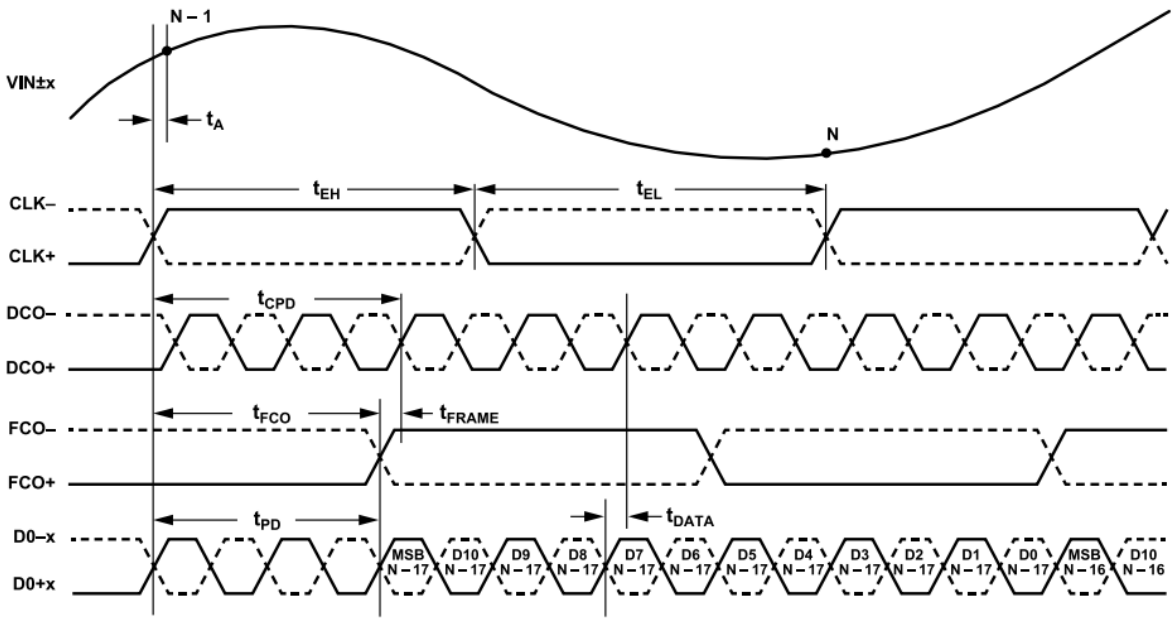



Figure 7. Byte-by-byte DDR, single-channel, 1x-frame, 12-bit output mode

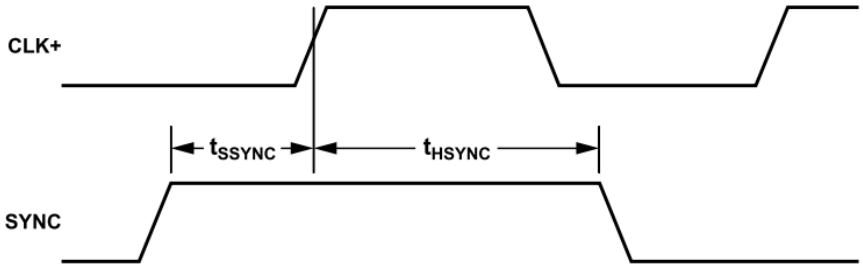



Figure 8. SYNC input timing requirements

### ADCP9253E-125 Pin Assignment

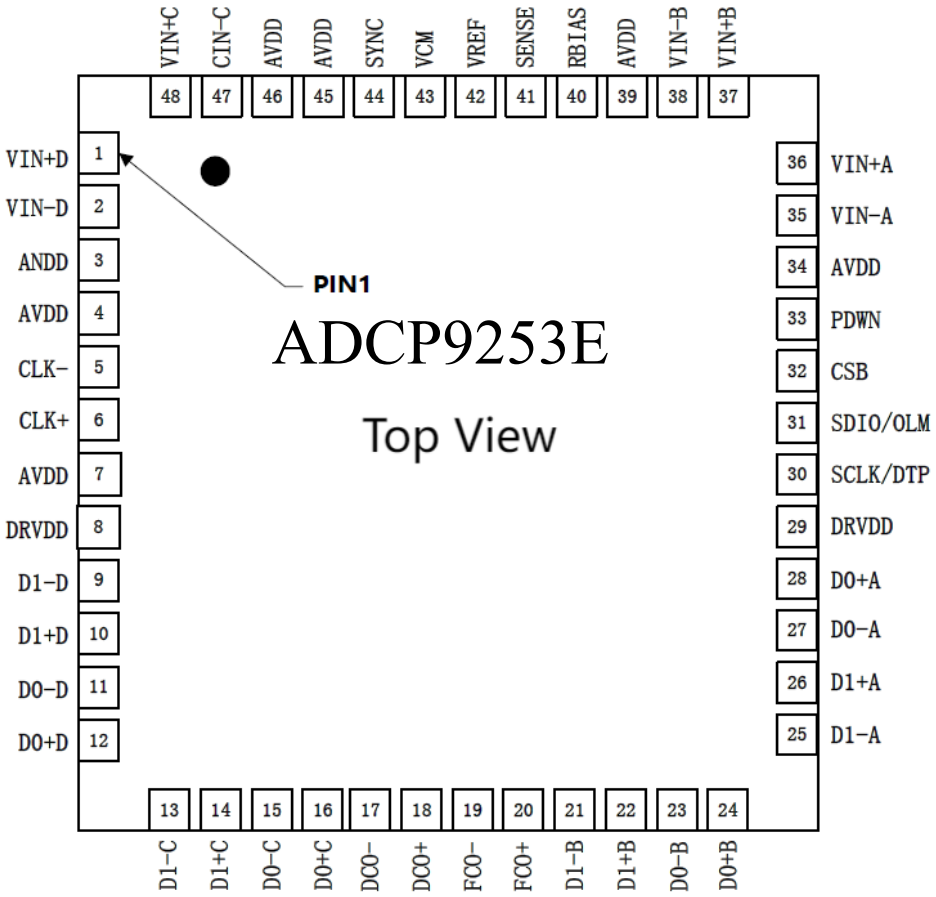



Figure 9. Pin configuration diagram of ADCP9253E-125

**Table 8: ADCP9253E-125 Pin Definitions**

| Pin | | Description |
|---|---|---|
| Name | No. | |
| AGND/PAD | 0 | Analog ground, exposed pads. Must be connected to ground to function properly. |
| VIN+D | 1 | ADC D analog input (+). |
| VIN-D | 2 | ADC D analog input ( - ). |
| AVDD | 3, 4, 7, 34, 39, 45, 46 | 1.8V analog power supply pin. |
| CLK-,CLK+ | 5,6 | Differential coded clock. PECL, LVDS, or 1.8V CMOS input. |
| DRVDD | 8,29 | Digital output driver power supply. |
| D1-D, D1+D | 9,10 | Channel D digital output. |
| D0-D,D0+D | 11,12 | Channel D digital output. |
| D1-C, D1+C | 13,14 | Digital C output. |
| D0-C,D0+C | 15,16 | Digital C output. |
| DCO-,DCO+ | 17,18 | Data clock output. |
| FCO-, FCO+ | 19,20 | Frame clock output. |
| D1-B, D1+B | 21,22 | Channel B digital output. |
| D0-B,D0+B | 23,24 | Channel B digital output. |
| D1-A, D1+A | 25,26 | Channel A digital output. |
| D0-A,D0+A | 27,28 | Channel A digital output. |

**Table 8: ADCP9253E-125 Pin Definitions (Continued)**

| Pin | | Description |
|---|---|---|
| Name | No. | |
| SCLK/DTP | 30 | SPI clock input/digital test code. |
| SDIO/OLM | 31 | SPI data input and output (bidirectional SPI data) / output channel mode. |
| CSB | 32 | SPI chip select signal. Active low for enable, with an internal 30kΩ pull-up resistor. |
| PDWN | 33 | Digital input, 30kΩ internal pull-down resistor.<br>PDWN high level = device off; PDWN low level = normal operation. |
| VIN-A | 35 | ADC A analog input ( - ). |
| VIN+A | 36 | ADC A analog input (+). |
| VIN+B | 37 | ADC B analog input (+). |
| VIN-B | 38 | ADC B analog input ( - ). |
| RBIAS | 40 | Set the analog current bias. Connect to a 10kΩ (1% tolerance) resistor to ground. |
| SENSE | 41 | Reference voltage mode selection. |
| VREF | 42 | Reference voltage input and output pins. |
| VCM | 43 | Analog input common-mode voltage. |
| SYNC | 44 | Digital input. SYNC input for the clock divider. |
| VIN-C | 47 | ADC C analog input ( - ). |
| VIN+C | 48 | ADC D analog input (+). |

## Equivalent Circuit

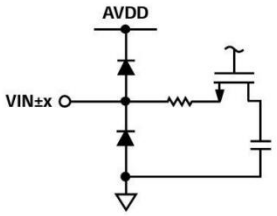



Figure 10. Equivalent Analog Input Circuit

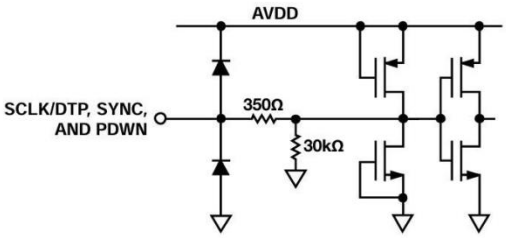



Figure 14. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

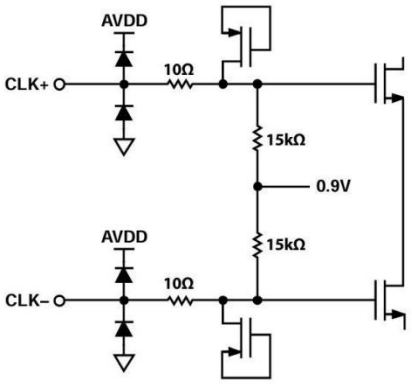



Figure 11. Equivalent Clock Input Circuit

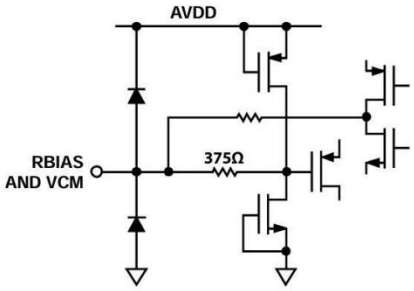



Figure 15. Equivalent RBIAS and VCM Circuit

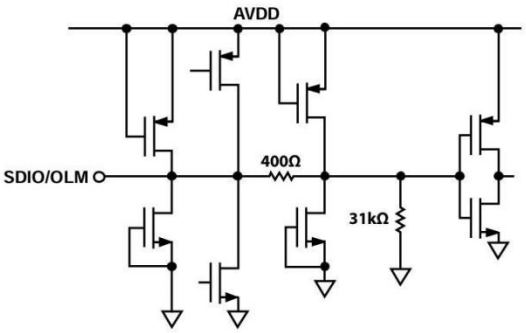



Figure 12. Equivalent SDIO/OLM Input Circuit

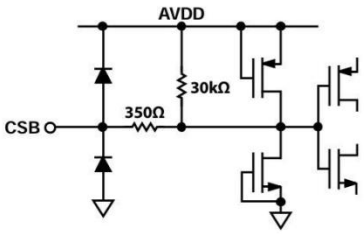



Figure 16. Equivalent CSB Input Circuit

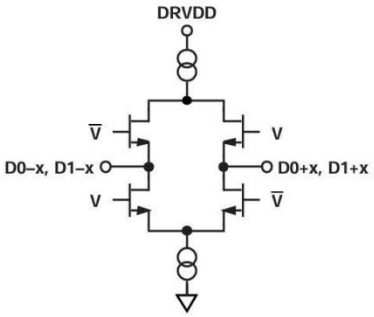



Figure 13. Equivalent Digital Output Circuit

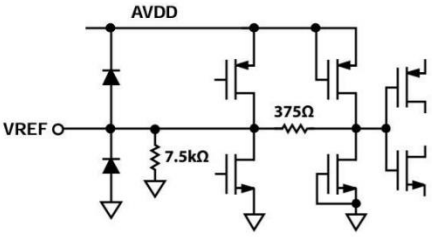



Figure 17. Equivalent VREF Circuit

## Working Principle

The ADCP9253E-125 is a multi-stage, pipelined ADC where each stage provides sufficient overlap to correct for Flash errors in the previous stage. The quantized outputs of each stage are combined and ultimately formed into a 14-bit conversion result in the digital correction logic. This converted data is sent in a 14-bit output format by a serializer. The pipelined architecture allows the first stage to process a new input sample while other stages continue processing previous samples. Sampling occurs on the rising edge of the clock. Each stage of the pipeline, except the last, consists of a low-resolution Flash ADC, a connected switched-capacitor DAC, and an interstage margin amplifier (e.g., a multiplicative digital-to-analog converter (MDAC)). The margin amplifier amplifies the difference between the reconstructed DAC output and the Flash input to provide to the next stage in the pipeline. To aid in digital correction of Flash errors, each stage is configured with one bit of redundancy. The final stage consists of only a single Flash ADC. The output stage module performs data alignment, error correction, and data transfer to the output buffer. The data is then serialized and aligned with the frame and data clock.

## Analog Input

Consider the analog input of the ADCP9253E-125, which is a differential switched-capacitor circuit designed to handle differential input signals. This circuit supports a wide common-mode range while maintaining excellent performance. Signal-dependent errors are minimized and optimal performance is achieved when the input common-mode voltage is at the intermediate supply voltage.

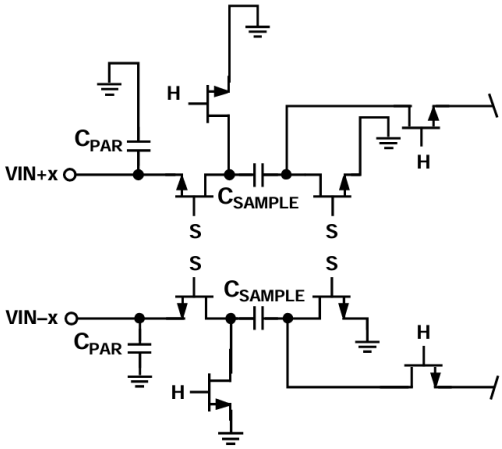



Figure 18. Switched capacitor input circuit

The input circuitry switches between sample and hold modes based on the clock signal (see Figure 18). When the input circuitry switches to sample mode, the signal source must be able to charge the sampling capacitor and complete the build-up within half a clock cycle. A small resistor is connected in series at each input to help reduce peak transient current injected from the driver output stage. Furthermore, low-Q inductors or ferrite beads can be used on each side of the inputs to reduce the high differential capacitance at the analog inputs, thereby maximizing the ADC's bandwidth. Low-Q inductors or ferrite beads must be used when driving the converter front end at high-frequency (IF). A differential capacitor or two single-ended capacitors can be used at the inputs to provide a matched passive network. This ultimately forms a low-pass filter at the inputs to limit unwanted broadband noise.

## Input Common Modulus

The ADCP9253E-125's analog inputs have no internal DC bias. Therefore, in AC-coupled applications, the user must provide an external bias. For optimal performance, it is recommended that the device be configured so that VCM = AVDD/2; however, reasonable performance can be achieved over a wider range. The chip provides an on-chip common-mode reference voltage via the VCM pin. A 0.1 μF capacitor must be used to bypass the VCM pin to ground. In a differential configuration, setting the ADC to its maximum range will achieve the highest SNR performance.

## Differential Input Configuration

There are various active or passive methods to drive the ADCP9253E-125; however, differential driving of the analog input achieves the best performance. In baseband applications, driving the ADCP9253E-125 with a differential dual-balun configuration provides excellent performance and a flexible interface for the ADC (see Figure 21). In applications where SNR is a critical parameter, differential transformer coupling is recommended in the input configuration (see Figure 22) because the noise performance of most amplifiers is insufficient to realize the true performance of the ADCP9253E-125. Regardless of the configuration used, the shunt capacitor value C depends on the input frequency and may need to be reduced or removed. Driving the ADCP9253E-125 input in a single-ended manner is not recommended.

## Reference Voltage Source

The ADCP9253E-125 integrates a stable and accurate reference voltage source. VREF can be configured to generate a reference voltage based on user selection, using an internal 1.0 V reference voltage, an externally applied 1.0 V to 1.3 V reference voltage, or an external resistor applied to the internal reference voltage. For a summary of various reference voltage source modes, please refer to the "Internal Reference Voltage Source Connection" and "External Reference Voltage Configuration" sections. The VREF pin should be bypassed to ground via a parallel combination of an external 0.1 µF low-ESR ceramic capacitor and a 1.0 µF low-ESR capacitor.

## Internal reference voltage connection

The ADCP9253E-125's built-in comparator detects the voltage at the SENSE pin, thus configuring the reference voltage into one of three possible modes (see Table 11). If the SENSE pin is grounded, the reference amplifier switch is connected to an internal resistor divider (see Figure 19), thus setting the voltage VREF at the VREF pin to 1.0 V. If SENSE is connected to an external resistor divider (see Figure 20), VREF is defined as follows:

$$V_{REF} = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

where:

$$7\ \text{k}\Omega \le (R1 + R2) \le 10\ \text{k}\Omega$$

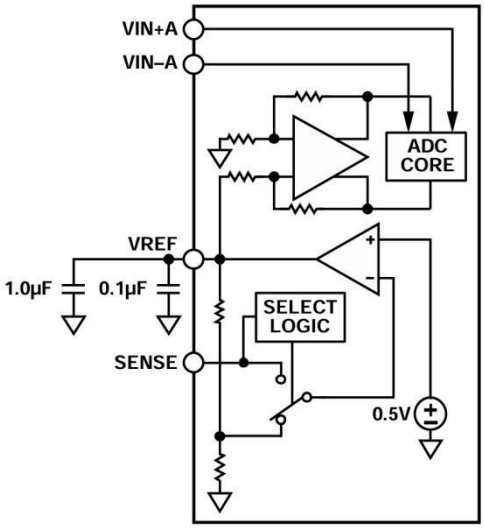



Figure 19. 1.0V internal reference voltage configuration

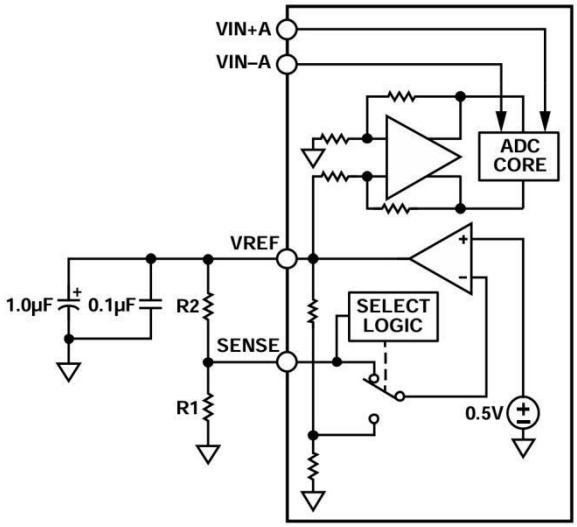



Figure 20. Programmable internal reference voltage configuration

**Table 11: Reference Voltage Configuration Table**

| Selected mode | SENSE voltage (V) | The corresponding $V_{REF}$ (V) | The corresponding difference range (Vp-p) |
|---|---|---|---|
| Fixed internal reference voltage | AGND to 0.2 | 1.0, Internal | 2.0 |
| Programmable internal reference voltage source | Connect an external R divider (see Figure 20) | 0.5 x (1 + R2/R1), for example, R1 = 3.5kΩ, R2 = 5.6kΩ ($V_{REF}$ = 1.3V) | 2 x $V_{REF}$ |
| Fixed external reference voltage | AVDD | 1.0 to 1.3, applied to the external VREF pin. | 2.0 to 2.6 |

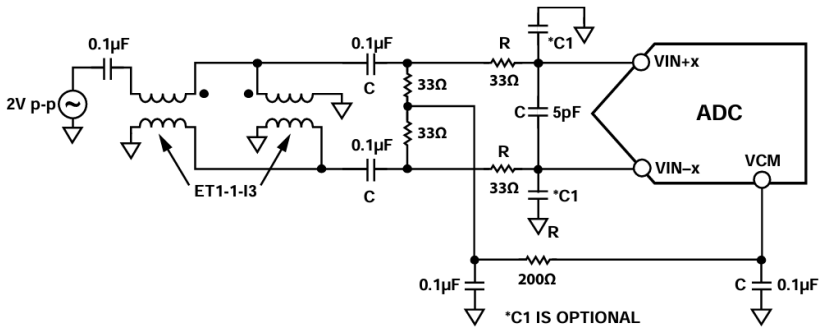



Figure 21. Differential dual-balun input configuration for baseband applications

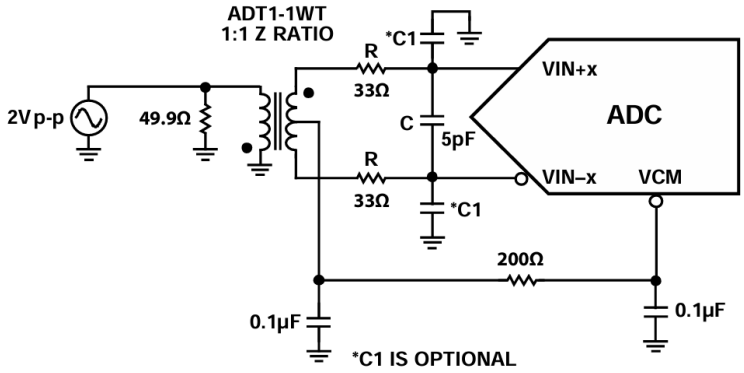



Figure 22. Differential transformer coupling configuration for baseband applications.

If the internal reference voltage of the ADCP9253E-125 is to be used to drive multiple converters to improve gain matching, the load of other converters on the reference voltage must be taken into account.

## External Reference Voltage

Using an external reference voltage may further improve ADC gain accuracy or thermal drift characteristics. Connecting the SENSE pin to AVDD disables the internal reference voltage source, allowing the use of an external reference voltage source. The internal reference voltage buffer provides a load equivalent to 7.5kΩ for an external reference voltage source. The internal buffer generates positive and negative full-scale reference voltages for the ADC core. Floating the SENSE pin is not recommended.

## Clock Input Vonsiderations

To fully utilize the chip's performance, a differential signal should be used as the clock signal for the ADCP9253E-125's sampling clock inputs (CLK+ and CLK− ) . This signal is typically AC-coupled to the CLK+ and CLK− pins using a transformer or capacitor . These two pins have internal bias and require no external bias.

## Clock Input Option

The ADCP9253E-125 features a flexible clock input configuration. CMOS, LVDS, LVPECL, or sine wave signals can all be used as its clock input. Regardless of the signal used, clock source jitter must be taken into account (see the Jitter Considerations section). Figures 23 and 24 show two preferred methods for providing a clock signal to the ADCP9253E-125 (clock rates up to 1 GHz before internal clock division). A single-ended signal from a low-jitter clock source can be converted to a differential signal using an RF transformer or RF balun. For clock frequencies from 125 MHz to 1 GHz, an RF balun configuration is recommended; for clock

frequencies from 20 MHz to 200 MHz, an RF transformer configuration is recommended. Back-to-back Schottky diodes connected across the secondary windings of the transformer/balun can limit the clock signal input to the ADCP9253E-125 to approximately a differential peak-to-peak value of 0.8 V. This prevents large clock voltage swings from feeding into other parts of the ADCP9253E-125 while preserving the signal's rapid rise and fall times, which is crucial for achieving low jitter performance. However, diode capacitance can have an impact at frequencies above 500MHz. Careful selection of the appropriate signal limiting diode is essential.

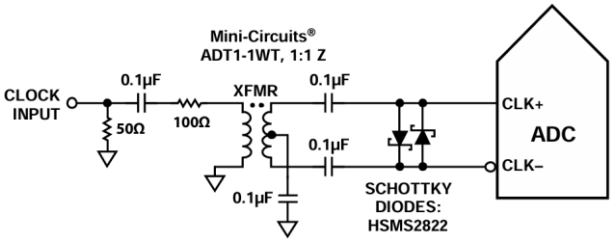



Figure 23. Transformer-coupled differential clock (frequency up to 200MHz)

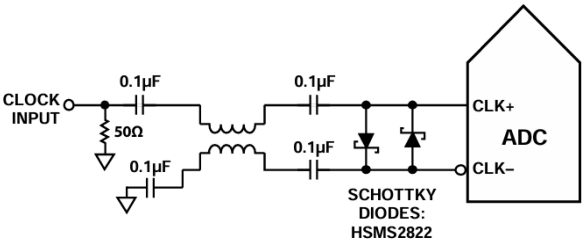



Figure 24. Balun-coupled differential clock (frequency up to 1GHz)

If a low-jitter clock source is unavailable, another approach is to AC couple the differential PECL signal to the sampling clock input pin (as shown in Figure 25).

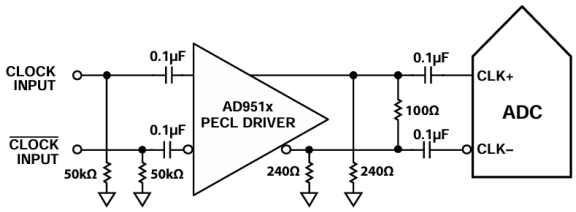



Figure 25. Differential PECL sampling clock (frequency up to 1GHz)

The third method is to AC couple the differential LVDS signal to the sampling clock input pin (as shown in Figure 26).

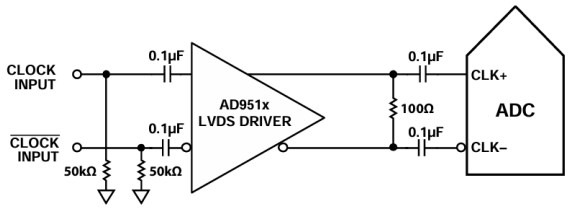



Figure 26. Differential LVDS sampling clock (frequency up to 1GHz)

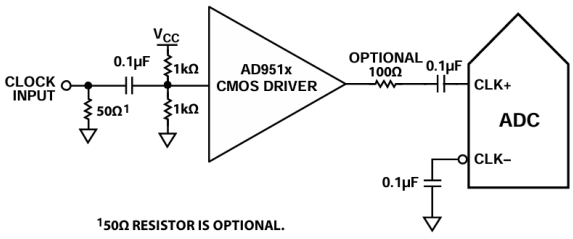



Figure 27. Single-ended 1.8V CMOS input clock (frequency up to 200MHz)

## Input Clock Divider

The ADCP9253E-125 incorporates an input clock divider that can divide the input clock by integer multiples from 1 to 8. The ADCP9253E-125 clock divider can be synchronized using an external SYNC input signal. By writing to bits 0 and 1 of register 0x109, the clock divider can be resynchronized upon each SYNC signal received, or only upon the first SYNC signal received. A valid SYNC resets the divider to its initial state. This synchronization feature allows the clock dividers of multiple devices to be aligned, ensuring simultaneous input sampling.

## Clock Duty Cycle

Typical high-speed ADCs utilize two clock edges to generate different internal timing signals, making them highly sensitive to clock duty cycle. Generally, to maintain the dynamic performance of an ADC, the clock duty cycle tolerance should be ± 5%. The ADCP9253E-125 incorporates a duty cycle stabilizer (DCS) that retims non-sampling edges (falling edges) and provides an internal clock signal with a nominal duty cycle of 50%. This feature minimizes performance degradation when the clock input duty cycle deviates from the nominal 50% value by more than ± 5%. When the DCS is enabled, noise and distortion performance is nearly flat over a wider duty cycle range. Input rising edge jitter remains a concern and cannot be easily reduced using internal stabilization circuitry. The duty cycle control loop is inactive when the clock rate is below 20MHz (nominal). In applications with dynamically changing clock rates, the time constant associated with this loop must be considered. Before the DCS loop relocks the input signal, it needs to wait for 1.5 μs to 5 μs.

## Precautions

High-speed, high-resolution ADCs are highly sensitive to the quality of the clock input signal. The formula for calculating the signal-to-noise ratio (SNR) drop caused solely by aperture jitter (tJ) at a given input frequency (fA) is as follows:

$$SNR\ Degradation = 20\log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In the formula, RMS aperture jitter represents the root mean square of all jitter sources (including the clock input signal, analog input signal, and ADC aperture jitter specification). Intermediate frequency undersampling applications are particularly sensitive to jitter. When aperture jitter may affect the dynamic range of the ADCP9253E-125, the clock input signal should be treated as an analog signal. The clock driver power supply should be isolated from the ADC output driver power supply to prevent digital noise from being introduced into the clock signal. A low-jitter crystal-controlled oscillator provides the optimal clock source. If the clock signal comes from other types of clock sources (via gating, division, or other methods), the original clock should be retied at the end.

## Power Consumption and Power Saving Mode

The power consumption of the ADCP9253E-125 is proportional to its sampling rate. Digital power consumption remains relatively stable, primarily determined by the DRVDD power supply and the bias current of the LVDS output driver. The ADCP9253E-125 can be put into power-down mode via the SPI port or by setting the PDWN pin high. In this state, the typical power consumption of the ADC is 2mW. In power-down mode, the output driver is in a high-impedance state. Setting the PDWN pin low returns the ADCP9253E-125 to normal operating mode. Note that PDWN is referenced to the data output driver power supply voltage (DRVDD) and must not exceed this voltage. Low power consumption is achieved in power-down mode by disabling the reference voltage source, reference voltage buffer, bias network, and clock. Internal capacitors discharge when entering power-down mode; they must be recharged upon returning to normal operating mode. Therefore, the wake-up time is related to the time spent in power-down mode; the shorter the time spent in power-down mode, the shorter the wake-up time. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. For shorter wake-up times, standby mode can be used, in which the internal reference voltage circuit is powered on. For more information on using these functions, see the " Memory Mapping " section.

## Digital Output and Timing

When powered on with default settings, the ADCP9253E-125 differential outputs conform to the ANSI-644 LVDS standard. It can be changed to a low-power, reduced-signal option (similar to the IEEE 1596.3 standard) via the SPI interface. The LVDS driver current is drawn from the chip, setting the output current at each output terminal to a nominal 3.5mA. The LVDS receiver input has a 100Ω differential termination resistor, resulting in a nominal receiver swing of 350mV (or 700mV p-p differential). In reduced-range mode, the output current drops to 2mA, and the receiver swing across the 100Ω termination resistor is 200mV (or 400mV p-p differential). The ADCP9253E-125 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs, enabling excellent switching performance in high-noise environments. A single point-to-point network topology is recommended, with the 100Ω termination resistor placed as close to the receiver as possible. Without remote receiver termination resistors, or with poor differential trace routing, timing errors may occur. To avoid timing errors, it is recommended that trace lengths not exceed 24 inches, and differential output traces should be as close to each other as possible and of equal length. When trace lengths exceed 24 inches, the user must ensure that the waveform meets the design's timing budget requirements. An additional SPI option allows the user to further increase the internal termination resistors (increasing current) of all four outputs, thereby driving longer traces. This can be achieved by setting register 0x15. While this produces steeper rise and fall times on data edges and is less prone to bit errors, using this option increases power consumption of the DRVDD power supply. The output data format is two's complement by default. Table 12 provides an example of an output encoding format. To change the output data format to offset binary, see the "Memory Mapping" section. In DDR mode, data from each ADC is serialized and provided through different channels. The data rate for each serial stream is equal to 14 bits multiplied by the sampling clock rate, with a maximum of 500 Mbps per channel [(14 bits × 125 MSPS) / (2 × 2) = 500 Mbps/channel]. The typical minimum conversion rate is 20 MSPS. See the "Memory Mapping" section for more information on using this feature. To aid in data capture from the ADCP9253E-125, the device provides two output clocks. The DCO is used to time the output data; in the default operating mode, it is equal to four times the sampling clock (CLK) rate. Data is output from the ADCP9253E-125 one byte at a time and must be captured on the rising and falling edges of the DCO; the DCO supports double data rate (DDR) capture. The FCO is used to indicate the start of a new output byte; in 1 × frame mode, it is equal to the sampling clock rate. See the timing diagram section for more information. When using SPI, the DCO phase can be adjusted in 60 ° increments relative to the data edges . This allows users to optimize system timing margins as needed. The default timing of DCO+ and DCO- is 90 ° relative to the output data edge . In default mode, the data output serial stream outputs the MSB first. However, this can be reversed using SPI, causing the data output serial stream to output the LSB first. There are 12 digital output test code options that can be initiated via SPI. This feature is useful when verifying receiver capture and timing. See Table 12 for available output bit sequence options. Some test codes have two serial sequence words that can be alternated in various ways, depending on the selected test code. Note that some test codes may not adhere to the data format selection options. Additionally, user-defined test codes can be specified in register addresses 0x19, 0x1A, 0x1B, and 0x1C.

**Table 12: Digital Output Encoding**

| Input (V) | Condition(V) | Offset binary output mode | Binary two's complement mode |
|---|---|---|---|
| VIN+ - VIN- | <-VREF – 0.5 LSB | 0000 0000 0000 0000 | 1000 0000 0000 0000 |
| VIN+ - VIN- | -VREF | 0000 0000 0000 0000 | 1000 0000 0000 0000 |
| VIN+ - VIN- | 0V | 1000 0000 0000 0000 | 0000 0000 0000 0000 |
| VIN+ - VIN- | +VREF – 1.0 LSB | 1111 1111 1111 1111 | 0111 1111 1111 1111 |
| VIN+ - VIN- | >+VREF – 0.5 LSB | 1111 1111 1111 1111 | 0111 1111 1111 1111 |

**Table 13: Flexible Output Test Modes**

| Output test mode bit sequence | Test code name | Digital output word 1 | Digital output word 2 | Accepted data format selection | Notes |
|---|---|---|---|---|---|
| 0000 | Off (default) | N/A | N/A | N/A | |
| 0001 | Intermediate level short code | 1000 0000 0000 0000 (16-bit) | N/A | yes | The image shows the binary offset complement. |
| 0010 | +Full-scale short code | 1000 0000 0000 0000 (16-bit) | N/A | yes | The image shows the binary offset complement. |
| 0011 | -Full-scale short code | 1000 0000 0000 0000 (16-bit) | N/A | yes | The image shows the binary offset complement. |
| 0100 | chessboard mode | 1010 1010 1010 1010 (16-bit) | 0101 0101 0101 0101 (16-bit) | no | |
| 0101 | PN long sequence | N/A | N/A | yes | PN23<br>ITU 0.150<br>$X^{23} + X^{18} + 1$ |
| 0110 | PN short sequence | N/A | N/A | yes | PN9<br>ITU 0.150<br>$X^{9} + X^{5} + 1$ |
| 0111 | 1/0 word reversal | 1111 1111 1111 1100 (16-bit) | 0000 0000 0000 0000 (16-bit) | no | |
| 1000 | User input | Registers 0x19 to 0x1A | Registers 0x1B to 0x1C | no | |
| 1001 | 1/0 bit reversal | 1010 1010 1010 1000 (16-bit) | N/A | no | |
| 1010 | 1X Synchronization | 0000 0001 1111 1100 (16-bit) | N/A | no | |
| 1011 | 1 bit high level | 1000 0000 0000 0000 (16-bit) | N/A | no | Test codes related to external pins |
| 1100 | Mixed frequency | 1010 0001 1001 1100 (16-bit) | N/A | no | |

The PN short sequence test code generates a pseudo-random bit sequence, repeating every $2^9 - 1$ or 511 bits. The seed value is all 1s (initial values are shown in Table 14). The output is a parallel representation of the serial PN9 sequence (MSB-first format). The first output word is the first 14 bits of the PN9 sequence in MSB-aligned form.

The PN long sequence test code generates a pseudo-random bit sequence, repeating every $2^{23} - 1$ or 8,388,607 bits. The seed value is all 1s (initial values are shown in Table 14), and the bit stream of ADCP9253E-125 is the reverse of the ITU standard. The output is a parallel representation of the serial PN23 sequence (MSB-first format). The first output word is the first 14 bits of the PN23 sequence in MSB-aligned form.

**Table 14: PN sequences**

| Sequence | Initial value | The first three sampled outputs (MSB first) are in two's complement binary format. |
|---|---|---|
| PN short sequence | 0x1FE0 | 0x1DF1,0x3CC8,0x294E |
| PN long sequence | 0x1FFF | 0x1FE0,0x2001,0x1C00 |

For information on how to change the timing characteristics of these additional digital outputs via SPI, see the " Memory Mapping " section.

## SDIO/OLM Pin

For applications that do not require SPI operation mode, connect the CSB pin to AVDD, and control the output channel mode using the SDIO/OLM pins according to Table 15. Note that when the CSB pin is connected to AVDD, the ADCP9253E-125DCS is enabled by default and remains enabled until the device enters SPI mode and is controlled via SPI. For more information on the DCS, see the " Clock Duty Cycle " section. For applications that do not use the SDIO/OLM pins, CSB should be connected to AVDD. When using single-channel mode, the conversion rate should not exceed 62.5 MSPS, meeting the maximum output rate requirement of 1 Gbps.

**Table 15. Output Channel Mode Pin Settings**

| OLM pin voltage | Output mode |
|---|---|
| AVDD (default) | Dual-channel. 1x frame, 16-bit serial output. |
| GND | Single channel. 1x frame, 16-bit serial output. |

## SCLK/DTP Pin

For applications that do not require SPI operation, the SCLK/DTP pin can be used to select the Digital Test Code (DTP). If this pin and the CSB pin are held high during device power-up, it enables a digital test code. When SCLK/DTP is connected to AVDD, the ADC channel outputs are shifted out of the following test code: 1000 0000 0000 0000. The FCO and DCO operate normally, and all channels are shifted out of the repeating test code. This test code allows the user to perform timing alignment on the FCO, DCO, and output data. This pin is connected to GND through an internal 10kΩ resistor . It can be disconnected.

**Table 16. Digital Test Code Pin Settings**

| Selected DTP | DTP voltage | Cases of D0±x and D1±x |
|---|---|---|
| Normal work | 10kΩ to AGND | Normal work |
| DTP | AVDD | 1000 0000 0000 0000 |

Additional and custom test codes can also be observed when commands are issued from the SPI port. See the " Memory Mapping " section for information on available options.

## CSB Pin

For applications that do not require SPI operation mode, the CSB pin should be connected to AVDD. Connecting CSB high will ignore all SCLK and SDIO information. Note that when the CSB pin is connected to AVDD, the ADCP9253E-125 DCS is enabled by default and remains enabled until the device enters SPI mode and is controlled via SPI. For more information on DCS, see the " Clock Duty Cycle " section.

## RBIAS Pin

To set the core bias current of the ADC, a 10.0 kΩ, 1% tolerance ground resistor should be connected in series on the RBIAS pin.

## Output Test Mode

The output test options are shown in Table 13 and are controlled by the output test mode bit at address 0x0D. When the output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end module, and the test codes pass through the output formatting module. Some test codes require output formatting, while others do not. Setting bit 4 or bit 5 of register 0x0D will reset the PN generator for the PN sequence test. Analog signals are optional during these tests (if present, they are ignored), but the encoding clock is essential.

## Serial Port Interface (SPI)

The ADCP9253E-125's Serial Port Interface (SPI) allows users to configure the converter using a structured register space within the ADC to meet specific functional and operational needs. SPI offers flexibility and can be customized for specific applications. The address space can be accessed and read from/written to via the serial port. The memory space is organized in bytes and can be further subdivided into multiple regions, as described in the " Memory Mapping " section.

## Configuration using SPI

The SPI of this ADC consists of three pins: SCLK, SDIO, and CSB (see Table 17). The SCLK (Serial Clock) pin is used to synchronize the ADC's read and write operations. The SDIO (Serial Data Input/Output) dual-function pin allows data to be sent to or read from the internal ADC memory-mapped register. The CSB (Chip Select) pin is an active-low control pin that enables or disables read/write cycles.

**Table 17. Output Channel Mode Pin Settings**

| Pin | Function |
|---|---|
| SCLK | Serial clock. Serial shift clock input, used to synchronize read and write operations of the serial interface. |
| SDIO | Serial data input/output. Dual-function pin; typically used as either input or output, depending on the command sent and its relative position in the timing frame. |
| CSB | Chip select signal. Active low, this control pin is used to select the read/write cycle. |

The falling edge of CSB and the rising edge of SCLK together determine the start of a frame. Figure 28 shows an example of a serial timing diagram, and the corresponding definitions are shown in Table 7. CSB can operate in several modes. CSB can always be kept low, thus keeping the device always enabled; this is called streaming. CSB can remain high between bytes, allowing for other external timing. When the CSB pin is connected high, the SPI function is in high-impedance mode. In this mode, a secondary function of the SPI pin can be enabled. One 16-bit instruction is transmitted in one instruction cycle. Data transmission occurs after the instruction transmission, and the data length is determined by bits W0 and W1. In addition to the word length, the instruction cycle also determines whether the serial frame is a read or write operation, thus programming the chip and reading data from on-chip memory through the serial port. The first bit of the first byte in a multi-byte serial data transmission frame indicates whether a read or write command is issued. If the instruction is a readback operation, performing the readback operation will change the data transmission direction of the Serial Data Input/Output (SDIO) pin from input to output at a certain position in the serial frame. All data consists of 8-bit words. Data can be sent in either MSB priority mode or LSB priority mode. The default mode after chip power-on is MSB priority, but the data transmission method can be changed via the SPI port configuration register.

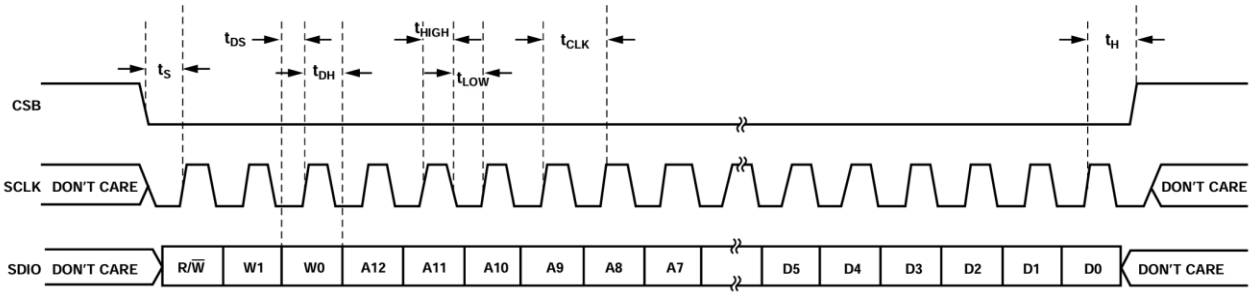



Figure 28. Serial port interface timing diagram

## Hardware Interface

The pins described in Table 17 comprise the physical interface between the user-programmable device and the serial port of the ADCP9253E-125. When using the SPI interface, the SCLK and CSB pins are used as input pins. The SDIO pin is bidirectional, used as an input during the write phase and as an output during the readback phase. The SPI interface is highly flexible and can be controlled by either an FPGA or a microcontroller. The SPI port should be disabled when the converter needs to fully utilize its dynamic performance. Typically, the SCLK, CSB, and SDIO signals are asynchronous with the ADC clock; therefore, noise in these signals can degrade converter performance. If other devices use the on-board SPI bus, a buffer may be needed between the bus and the ADCP9253E-125 to prevent these signals from changing at the converter's inputs during critical sampling periods. When the SPI interface is not used, some pins serve secondary functions. These pins perform specific functions when connected to DRVDD or ground during device power-up. Tables 15 and 16 illustrate the bonding functions supported by the ADCP9253E-125.

## Configuration without using SPI

In applications that do not use the SPI control register interface, the SDIO/OLM, SCLK/DTP, and PDWN pins are used as independent CMOS-compatible control pins. When the device is powered on, it is assumed that the user intends to use these pins as static control lines to control the output channel mode, digital test code, and power-down characteristics, respectively. In this mode, the CSB pin should be connected to AVDD to disable the serial port interface. Note that when the CSB pin is connected to AVDD, the ADCP9253E-125 DCS is enabled by default and remains enabled until the device enters SPI mode and is controlled via SPI. For more information on DCS, see the " Clock Duty Cycle " section. When the device is in SPI mode, the PDWN pin (if enabled) remains active. To save power when controlled via SPI, the PDWN pin should be set to the default state.

## SPI Access Features

Table 18 briefly illustrates the general characteristics that can be accessed via SPI.

**Table 18. Features accessible via SPI**

| Feature Name | Description |
|---|---|
| Power consumption mode | Allows users to set a power-saving mode or standby mode |
| Clock | Allows users to configure the clock divider, set the clock divider phase, and enable synchronization |
| Disorder | Allows users to adjust converter offset digitally |
| Test I/O | Allows users to set a test mode so that known data can be obtained on the output bits |
| Output mode | Allow users to set the output mode |
| Output phase | Allows users to set the output clock polarity |

## Memory Mapping

### Read the memory-mapped register table

Each row of the memory-mapped register table has 8 bits. The memory map is broadly divided into three parts: chip configuration registers (addresses 0x00 to 0x02), device index and transfer registers (addresses 0x05 and 0xFF), and global ADC function registers, including setup, control, and test (addresses 0x08 to 0x109). The memory-mapped register table (see Table 19) lists each hexadecimal address and its hexadecimal default value. The 7th bit (MSB) column is the starting bit of a given hexadecimal default value. For example, the hexadecimal default value for the device index register (address 0x05) is 0x3F, which means that at address 0x05, bits [7:6] = 0 and the remaining bits [5:0] = 1. This setting is the default channel index setting. This default value causes both ADC channels to receive the next write command. The "Memory-Mapped Register Description" section describes the other registers.

### Disabled location

This device does not currently support all addresses and bits not listed in Table 19. Unused bits in a valid address should be written to 0. Write operations are only required for addresses (e.g., address 0x05) if only some bits are disabled. If an entire address (e.g., address 0x13) is disabled or not listed in Table 19, no write operations should be performed on that address.

### Default value

After the ADCP9253E-125 is reset, critical registers will be loaded with their default values. Table 19 (Memory-Image Register Table) lists the default values for each register. Logic Levels: The following is a description of the terminology for logic levels:

• " Setting " refers to "set a bit to logic 1" or "write logic 1 to a bit".

• " Clear bit " refers to " set a bit to logic 0" or " write logic 0 to a bit".

### Specific channel register

Certain channel functions (e.g., signal monitoring thresholds) can be programmed individually for each channel. In these cases, the channel address location can be copied internally for each channel. These registers and their corresponding bits are referred to as local registers in Table 19. These local registers and their corresponding bits can be accessed by setting the appropriate data channel bit (A, B, C, or D), clock channel DCO bit (bit 5), and FCO bit (bit 4) of register 0x05. If all bits are set, subsequent write operations will affect the registers of all channels and the DCO/FCO clock channels. In a read cycle, only one channel (A, B, C, or D) is set, and a read operation is performed on one of the four registers. If all bits are set in an SPI read cycle, the device returns the value for channel A. The global registers and their corresponding bits given in Table 19 affect the characteristics of the entire device or channel and cannot be set individually for each channel. Settings in register 0x05 do not affect the values of the global registers and their corresponding bits.

### Memory Mapped Register Table

The ADCP9253E-125 uses a 3-wire interface and 16-bit addressing. Therefore, bits 0 and 7 of register 0x00 are set to 0, and bits 3 and 4 are set to 1. When bit 5 of register 0x00 is set to 1, the SPI enters a soft reset, all user registers are restored to their default values, and bit 2 is automatically cleared to 0.

**Table 19:**

| Address (hexade-cimal) | Parameter name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default value (hexade-cimal) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Chip configuration register** | | | | | | | | | | | |
| 0x00 | SPI port configur a-tion | 0 = SDO valid | LSB priority | Soft reset | 1 = 16-bit address | 1 = 16-bit addres s | Soft reset | LSB priority | 0 = SDO valid | 0x18 | The nibbles are mirror images of each other, ensuring that the registers can correctly record data in either LSB-first or MSB-first mode. The default value for the ADC is 16-bit mode. |
| 0x01 | Chip ID (Global) | 8-bit chip ID, bits [7:0]<br>ADCP414 - x 0xB5 = Quad-channel, 14-bit, 125/105/80MSPS serial LVDS | | | | | | | | 0xB5 | A unique chip ID is used to distinguish devices and is read-only. |
| 0x02 | Disable | Disable | Disable | Disable | Disable | Disable | Disable | Disable | Disable | | Disable |
| **Device Index and Transfer Register** | | | | | | | | | | | |
| 0x05 | Device Index | Disable | Disable | Clock Channel DCO | Clock Channel FCO | Data Channel D | Data Channel C | Data Channel B | Data Channel A | 0x3F | These bits determine which on-chip device will accept the next write command. The default is all on-chip devices. |
| 0xFF | Transmiss-ion | Disable | Disable | Disable | Disable | Disable | Disable | Disable | Startup Cover-age | 0x00 | Set sampling rate coverage. |
| **Global ADC Function Register** | | | | | | | | | | | |
| 0x08 | Power consumpti on mode (global) | Disable | Disable | External power-down pin function<br>0 = Complet e power outage<br>1 = Standby | Disable | Disable | Disable | Power consumption mode<br>00 = Chip Operation<br>01 = Complete power outage<br>10 = Standby<br>11 = Reset | | 0x00 | It determines the general operating mode of the chip. |
| 0x09 | Clock (Global) | Disable | Disable | Disable | Disable | Disable | Disable | Disable | Duty cycle stable<br>0 = Open<br>1 = Closed | 0x01 | Turn the duty cycle stabilizer on or off. |
| 0x0B | Clock frequency division (global) | Disable | Disable | Disable | Disable | Disable | Clock division ratio [2:0]<br>000 = 1 divider<br>001 = 2 divider<br>010 = 3-way divider<br>011 = 4-way divider<br>100 = 5 divider<br>101 = 6 divider<br>110 = 7 divider<br>111 = 8 divider | | | 0x00 | |
| 0x0C | Disable | Disable | Disable | Disable | Disable | Disable | Chopper Mode<br>0 = Off<br>1 = Open | Disable | Disable | 0x00 | Enable/Disable Chopper Mode |
| 0x0D | Test mode (Except for local PN sequence reset) | User input test mode<br>00 = Single<br>01 = Alternating<br>10 = a single time<br>11 = alternating once<br>(This only affects the user input test mode, bits [3:0]=1000) | | Generate a reset PN long sequenc e | Generate a reset PN short sequence | Output test mode [3:0] (partial)<br>0000 = Off (default)<br>0001 = Short sequence at intermediate level<br>0010 = Positive FS<br>0011 = Negative FS<br>0100 = Alternating chessboard pattern<br>0101 = PN 23 sequence<br>0110 = PN 9 sequence<br>0111 = 1/0 word reversed<br>1000 = User input<br>1001 = 1/0 bit reversal<br>1010 = 1x synchronization<br>1011 = 1 high level<br>1100 = Mixed bit frequency | | | | 0x00 | When set to 1, the test data will be placed on the output pin instead of the normal data. |

| Address (hexade-cimal) | Parameter name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default value (hexade-cimal) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x10 | Disharmony adjustment (local) | 8-bit device misalignment adjustment, bits [7:0] (local)<br>Offset adjustment is measured in LSBs, ranging from +127 to -128 (two's complement form). | | | | | | | | 0x00 | Device misalignment adjustment. |
| 0x14 | Output mode | Disable | LVDS-ANSI/LVDS-IEEE Options<br>0=LVDS-ANSI<br>1=LVDS-IEEE<br>Narrowing-Range Link (Global) | Disable | Disable | Disable | Output inverse (partial) | Disable | Output format<br>0 = offset binary<br>1 = Two's complement (global) | 0x01 | Configure the output and data format. |
| 0x15 | Output adjustment | Disable | Disable | Output driver terminated at [1:0]<br>00 = None<br>01 = 200Ω<br>10 = 100Ω<br>11 = 100Ω | | Disable | Disable | Disable | Output driver<br>0 = 1x driver<br>1 = 2x drive | 0x00 | Determine LVDS or other output attributes. |
| 0x16 | Output phase | Disable | Input clock phase adjustment [6:4]<br>(Value is the number of input clock cycles with phase delay) | | | Output clock phase adjustment [3:0]<br>(0000 to 1011) | | | | 0x03 | In devices that utilize global clock division, the decision is made regarding which phase of the divider output to provide the output clock. The internal latch remains unaffected. |
| 0x18 | $V_{REF}$ | Disable | Disable | Disable | Disable | Disable | $V_{REF}$ adjustment<br>Numerical scheme [2:0]<br>000 = 1.0Vp-p (1.3Vp-p)<br>001 = 1.14Vp-p (1.48Vp-p)<br>010 = 1.33Vp-p (1.73Vp-p)<br>011 = 1.6Vp-p (2.08Vp-p)<br>100 = 2.0Vp-p (2.6Vp-p) | | | 0x04 | Select the internal $V_{REF}$ display value for $V_{REF}$ = 1.0V (1.3V). |
| 0x19 | USER_PATT1_LSB (Global) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User-defined test code 1LSB. |
| 0x1A | USER_PATT1_MSB (Global) | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User-defined test code 1MSB |

| Address (hexade-cimal) | Parameter name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default value (hexade-cimal) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x1B | USER_PATT2_LSB (Global) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0x00 | User-defined test code 2LSB |
| 0x1C | USER_PATT2_MSB (Global) | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | 0x00 | User-defined test code 2MSB |
| 0x21 | Serial output data control (global) | LVDS output LSB priority | SDR/DDR single-channel/dual-channel, bit-by-bit/byte-by-byte [6:4]<br>000 = SDR dual-channel, bit-by-bit<br>001 = SDR dual-channel, byte-by-byte<br>010 = DDR dual-channel, bit-by-bit<br>011 = DDR dual-channel, byte-by-byte<br>100 = DDR single channel, word-by-word | | | Disable | Select 2x frames | Serial output bit depth<br>00 = 16 bits | | 0x30 | Serial stream control. The default is MSB priority, existing bit stream. |
| 0x22 | Serial channel status (local) | Disable | Disable | Disable | Disable | Disable | Disable | Channel output reset | Channel power failure | 0x00 | Used to shut down the various parts of the converter. |
| 0x100 | Sampling rate coverage | Disable | Sampling rate coverage enable | 0 | 0 | Disable | Sampling rate<br>000 = 20MSPS<br>001 = 40MSPS<br>010 = 50MSPS<br>011 = 65MSPS<br>100 = 80 MSPS<br>101 = 105 MSPS<br>110 = 125 MSPS | | | 0x00 | Sampling rate coverage (requires transfer register, 0xFF). |
| 0x101 | User I/O Control 2 | Disable | Disable | Disable | Disable | Disable | Disable | Disable | SDIO pulldown | 0x00 | Disable SDIO pull-down resistors. |
| 0x102 | User I/O Control 3 | Disable | Disable | Disable | Disable | VCM power failure | Disable | Disable | Disable | 0x00 | VCM control |
| 0x109 | synchronous | Disable | Disable | Disable | Disable | Disable | Disable | Synchronize only with the next synchronization pulse | Enable synchronization | 0x00 | User-defined test code 1LSB. |

## Memory-Mapped Register Description

### Device Index (Register 0x05)

For some characteristics in the mapping, each channel can be set independently, while other characteristics are globally applicable (depending on the context), regardless of which channel is selected. The first 4 bits of register 0x05 can be used to select which data channel is affected. The output clock channel can also be selected via register 0x05. This allows a small subset of independent characteristics to be applied to these devices.

### Transfer (Register 0xFF)

Except for register 0x100, all other registers are updated immediately upon being written. When bit 0 of this transfer register is set to 1, the sampling rate override register (address 0x100) is initialized.

### Power Consumption Mode (Register 0x08)

**Bit [7:6] - Disabled**

**Bit 5 - External power-down pin function**

If set, the external PDWN pin starts standby mode. If cleared, the external PDWN pin starts power-saving mode.

**Bit [4:2] - Disable**

**Bits [1:0] - Power Mode**

When operating normally (bits[1:0]=00), all ADC channels are enabled.

In power-down mode (bits[1:0]=01), the digital data path clock is disabled, the digital data path is reset, and the output is disabled.

In standby mode (bits [1:0] = 10), the digital data path clock and output are both disabled.

During a digital reset (bits[1:0]=11), all other digital data path clocks and outputs (where applicable) of the chip, except for the SPI port, are reset. Note that the SPI is always under user control and is never automatically disabled or reset (unless powered on).

### Clock (Register 0x09)

**Bit [7:1] - Disable**

**Bit 0 - Duty Cycle Stabilizer**

The default state is bit 0 = 1, and the duty cycle stabilizer is off.

Please note that the duty cycle stabilizer will be enabled when the device is not in SPI mode. See the " Configuration without SPI " section for details.

### Enhanced Control (Register 0x0C)

**Bit [7:3] - Disabled**

**Position 2 - Chopper Mode**

Some applications are sensitive to offset voltage and other low-frequency noise, such as null-difference or direct-conversion receivers. For these applications, bit 2 can be set to enable the chopping characteristics of the first stage of the ADCP9253E-125. In the frequency domain, chopping converts offset and other low-frequency noise into fCLK / 2, which can be filtered out by a filter.

**Bits [1:0] — Disable**

### Output Mode (Register 0x14)

**Bit 7 — Disable**

**Bit 6 — LVDS-ANSI/LVDS-IEEE option**

When this position is 1, select the LVDS-IEEE (narrowed range) option. The default setting is LVDS-ANSI. As shown in Table 20, when selecting the LVDS-ANSI or LVDS-IEEE narrowed range link, the user can select the driver termination. The device automatically selects the driver current to provide an appropriate output swing.

**Table 20: LVDS-ANSI/LVDS-IEEE Options**

| Output mode, 60 bits | Output mode | Output driver termination | Output driver current |
|---|---|---|---|
| 0 | LVDS-ANSI | User selectable | Automatically selects to provide appropriate swing amplitude |
| 1 | LVDS-IEEE Narrowing Link | User selectable | Automatically selects to provide appropriate swing amplitude |

**Bit [5:3] - Disable**

**Bit 2 - Output Inversion**

When this position is 1, the output bit stream is inverted.

**Bit 1 - Disabled**

**Bit 0 - Output Format**

By default, this position 1 transmits data output in binary complement format. If this bit is reset, the output mode changes to offset binary.

**Output Adjustment (Register 0x15)**

**Bit [7:6] - Disabled**

**Bit [5:4] - Output Driver Termination**

These bits allow users to select internal termination resistors.

**Bit [3:1] - Disable**

**Bit 0 - Output Driver**

0 of the output adjustment register controls only the drive strength of the LVDS drivers for the FCO and DCO outputs. The default value is 1 × drive, which can be increased to 2 × by setting the appropriate channel bit in register 0x05 and then setting bit 0 to 1. These features cannot be used with output driver termination selection. When both output driver termination and output drive are selected, termination selection takes precedence over the 2 × drive strength selection for the FCO and DCO .

## Output Phase (Register 0x16)

**Bit 7 - Disable**

**Bit [6:4] - Input Clock Phase Adjustment**

**Table 21: Input Clock Phase Adjustment Options**

| Input clock phase adjustment bits [6:4] | Phase delay of input clock cycles |
|---|---|
| 000 (Default) | 0 |
| 001 | 1 |
| 010 | 2 |
| 011 | 3 |
| 100 | 4 |
| 101 | 5 |
| 110 | 6 |
| 111 | 7 |

**Bits [3:0] - Output Clock Phase Adjustment**

**Table 22: Output Clock Phase Adjustment Options**

| Output Clock (DCO) Phase Adjustment Bits [3:0] | DCO phase adjustment (degrees relative to the D0±x/D1±x edge) |
|---|---|
| 0000 | 0 |
| 0001 | 60 |
| 0010 | 120 |
| 0011 (default) | 180 |
| 0100 | 240 |
| 0101 | 300 |
| 0111 | 420 |
| 1000 | 480 |
| 1001 | 540 |
| 1010 | 600 |
| 1011 | 660 |

## Serial Output Data Control (Register 0x21)

The serial output data control register is used to set various output data modes for the ADCP9253E-125, depending on the data capture scheme. Table 23 lists the various serialization options for the ADCP9253E-125.

## Sampling Rate Coverage (Register 0x100)

0 of the transfer register (register 0xFF) is written high.

## User I/O Control 2 (Register 0x101)

**Bit [7:1] - Disable**

**Bit 0 - SDIO Pulldown**

Bit 0 can be set to 1 to disable the 30 kΩ pull-down resistor built into the SDIO pin; it can be used to limit the load when many devices are connected to the SPI bus.

## User I/O Control 3 (Register 0x102)

**Bit [7:4] - Disabled**

**Position 3 - VCM Power Failure**

The internal VCM generator can be turned off by setting bit 3 high. Use this function when using an external reference voltage source.

**Bits [2:0] - Disable**

**Table 23: SPI Register Options**

| Contents of register 0x21 | Selected serialization option | | | DCO frequency multiplier | Time series diagram |
|---|---|---|---|---|---|
| | Serial output bit width (SONB) | Frame mode | Serial data mode | | |
| 0x30 | 16-bit | 1x | DDR dual-channel byte-by-byte | 4 x fs | Figure 2 (Default Settings) |
| 0x20 | 16-bit | 1x | DDR dual-channel bit-by-bit | 4 x fs | Figure 2 |
| 0x10 | 16-bit | 1x | SDR Dual Channel Byte-by-Byte | 8 x fs | Figure 2 |
| 0x00 | 16-bit | 1x | SDR Dual-Channel Bit-by-Bit | 8 x fs | Figure 2 |
| 0x34 | 16-bit | 2x | DDR dual-channel byte-by-byte | 4 x fs | Figure 3 |
| 0x24 | 16-bit | 2x | DDR dual-channel bit-by-bit | 4 x fs | Figure 3 |
| 0x14 | 16-bit | 2x | SDR Dual Channel Byte-by-Byte | 8 x fs | Figure 3 |
| 0x04 | 16-bit | 2x | SDR Dual-Channel Bit-by-Bit | 8 x fs | Figure 3 |
| 0x40 | 16-bit | 1x | DDR single-channel word | 8 x fs | Figure 4 |
| 0x32 | 12-digit | 1x | DDR dual-channel byte-by-byte | 3 x fs | |
| 0x22 | 12-digit | 1x | DDR dual-channel word | 3 x fs | |
| 0x12 | 12-digit | 1x | SDR Dual Channel Byte-by-Byte | 6 x fs | |
| 0x02 | 12-digit | 1x | SDR Dual Channel Word-by-Word | 6 x fs | |
| 0x36 | 12-digit | 2x | DDR dual-channel byte-by-byte | 3 x fs | |
| 0x26 | 12-digit | 2x | DDR dual-channel word | 3 x fs | |
| 0x16 | 12-digit | 2x | SDR Dual Channel Byte-by-Byte | 6 x fs | |
| 0x06 | 12-digit | 2x | SDR Dual Channel Word-by-Word | 6 x fs | |
| 0x42 | 12-digit | 1x | DDR single-channel word | 6 x fs | |

## Application Information

**Design Guidelines**

Before designing and placing the ADCP9253E-125 system, designers are advised to familiarize themselves with the following design guidelines, which describe the special circuit connections and layout routing requirements for certain pins.

**Power Supply and Grounding Recommendations**

When connecting power to the ADCP9253E-125, it is recommended to use two independent 1.8V power supplies: one for the analog output (AVDD) and the other for the digital output (DRVDD). For AVDD and DRVDD, several different decoupling capacitors should be used to support both high and low frequencies. These decoupling capacitors should be placed close to the PCB entry point and near the device pins, with trace lengths kept as short as possible. The ADCP9253E-125 requires only one PCB ground plane. Proper decoupling and clever separation of the PCB's analog, digital, and clock modules easily achieves optimal performance.

**Recommendations for Exposed Pad Heat Sinks**

To achieve optimal electrical and thermal performance of the ADCP9253E-125, the exposed pads on the bottom of the ADC must be connected to analog ground (AGND). The exposed continuous copper layer on the PCB should match the exposed pads (pin 0) of the ADCP9253E-125. Multiple vias should be present on the copper layer to provide the lowest possible thermal resistance path for heat dissipation through the bottom of the PCB. These vias should be filled with solder or have inserted pins. To maximize coverage and connection between the ADC and the PCB, a silkscreen layer should be applied to the PCB to divide the continuous copper plane on the PCB into multiple equal sections. This allows for multiple connection points between the ADC and the PCB during reflow soldering, whereas a continuous, undivided plane can only guarantee one connection point.

**VCM**

The VCM pin should be bypassed to ground via a 0.1μF capacitor.

**Reference Voltage Source Decoupling**

The $V_{REF}$ pin should be bypassed to ground via a parallel combination of an external 0.1 μF ceramic capacitor with low ESR and a 1.0 μF capacitor with low ESR.

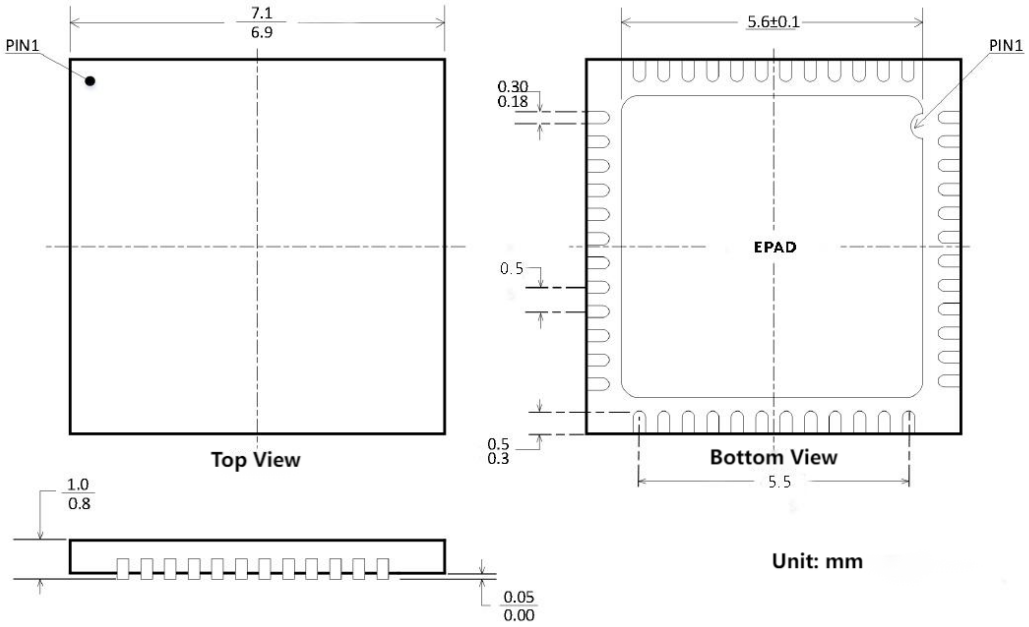
**SPI Port**

The SPI port should be disabled when the converter needs to fully utilize its dynamic performance. Typically, the SCLK, CSB, and SDIO signals are asynchronous with the ADC clock; therefore, noise in these signals can degrade converter performance. If other devices use the on-board SPI bus, a buffer may be needed between this bus and the ADCP9253E-125 to prevent these signals from changing at the converter input during critical sampling periods.

**Crosstalk Performance**

The ADCP9253E-125 is packaged in a 48-pin LFCSP with input pairs in every corner. Pin configuration is shown in Figure 9. To maximize crosstalk performance, ground-filled vias can be added between adjacent channels.

## Package Size and Structure




## Device Ordering Information List

| Product Model | Temperature Range | Packaging Type | Packaging Quantity | RoHS |
|---|---|---|---|---|
| ADCP9253E - 125QN | – 55°C to +125°C | QFN-48 | 260/reel | Y |
| ADCP9253E - 105QN | – 55°C to +125°C | QFN-48 | 260/reel | Y |
| ADCP9253E - 80QN | – 55°C to +125°C | QFN-48 | 260/reel | Y |