ADCP9245-20 14-Bit, 50MSPS, A/D Converter

1. Characteristics

- Analog power supply voltage: 3.0V ~ 3.3V
- Digital power supply voltage: 2.5V ~ 3.3V
- Maximum sampling rate: 50 MSPS
- SNR(Signal to Noise Ratio): ≥65 dB
- Differential linearity error: ±1.5 LSB
- Power consumption: ≤414mW
- Analog input range: 1V $_{PP}$ ~ 2V $_{PP}$
- Circuit interface: Parallel CMOS level interface
- ESD rating: 1000V

2. Applications

- High-end medical imaging equipment
- Intermediate frequency signal sampling of communication receiver
- Portable instrument
- Low-power digital oscilloscope

3. Overview

The ADCP9245-20 is a 14-bit, 50MSPS A/D converter manufactured using CMOS technology. This product employs a pipelined architecture, internally including a sample-and-hold amplifier, a pipelined ADC, a reference voltage, clock stabilization circuitry, and mode selection circuitry. It is packaged in a 32-lead plastic quad flat package (QFN32), with dimensions of 5.0mm (L) × 5.0mm (W) × 0.75mm (H). This product is a viable replacement for Analog Devices' AD9245.

4. Device packaging information

Model	Packaging Type	Package Size
ADCP9245-20	QFN32	5.0mm×5.0mm

5. Functional Block Diagram

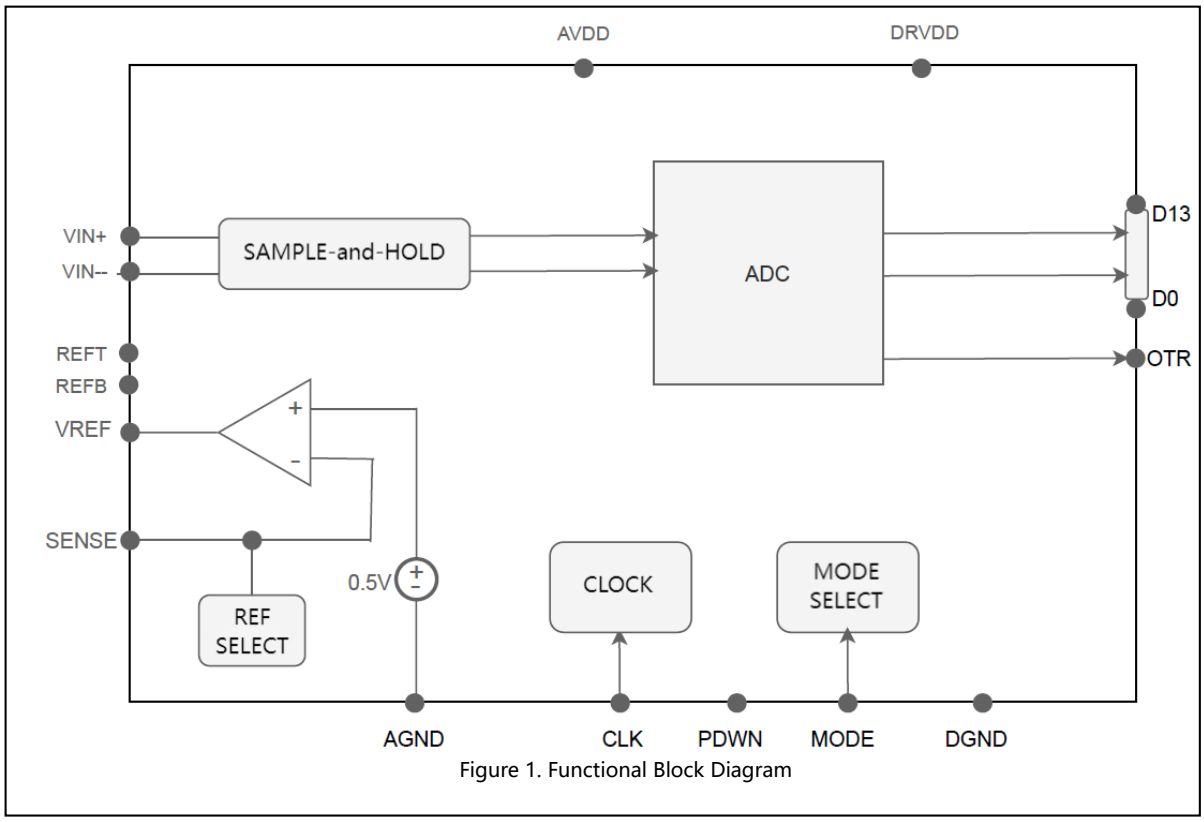

Figure 1. Functional Block Diagram

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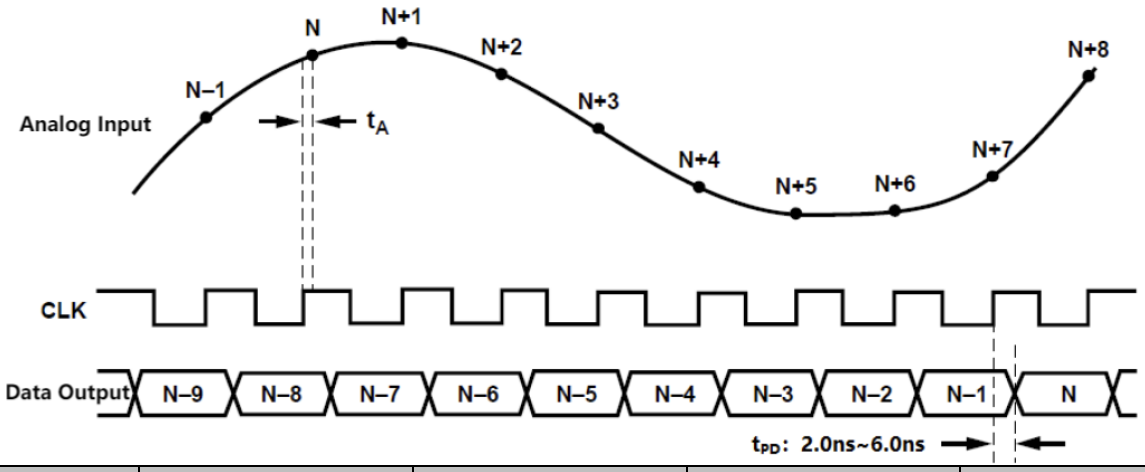
6. Work sequence



Parameter	Description	Min	Typ	Max
t_A	Aperture Delay	- -	1.4ns	- -
t_{PD}	Output delay	2.0ns	2.85ns	6.0ns
Latency	Pipeline delay	- -	7Cycles	- -

7. Specifications

- **Absolute maximum ratings**

Name	Value
Power supply voltage	3.9V
Storage temperature T_S	- 55℃～125℃
Junction temperature T_j	175℃
Soldering temperature resistance of lead wires T_H (10s)	300℃

- **Recommended working conditions**

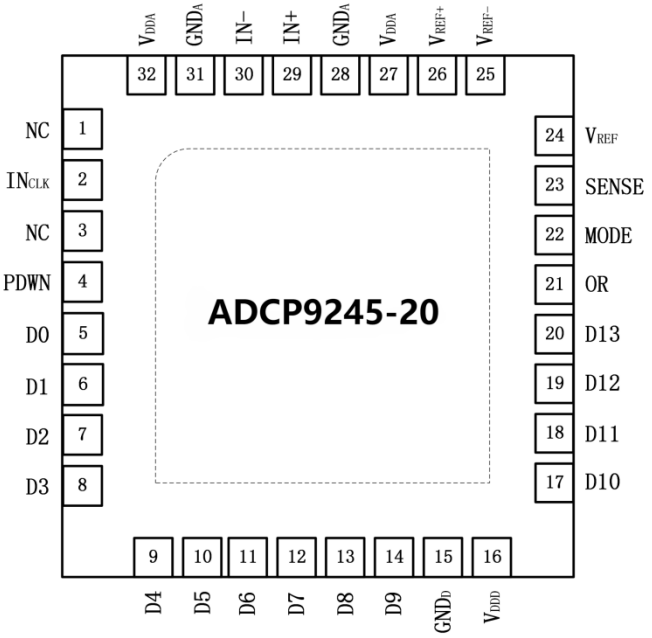
Name	Value
Analog power supply voltage	3.0V
Digital power supply voltage	2.5V
Differential analog input voltage Vp-p	1V/2V
Clock frequency range	1MHz～50MHz
Operating ambient temperature	- 45℃～85℃

8. Electrical characteristics

(Unless otherwise specified, V_{DDA} = 3V, V_{DDD} = 2.5V, f_{CLK} = 50MHz, GND_A = GND_D = 0V, f_{IN} = 0.97MHz, MODE = PDWN = SENSE = 0V, internal 1V reference, differential analog input range $2V_{PP}$, -40℃ ≤ T_A ≤ 85℃)

Symbol	Name	Condition	Min	Typ	Max	Unit
RES	Resolution	---		14		bit
E_L	Linear error	---	-7.5	±3.40	7.5	LSB
E_{DL}	Differential linearity error	---	-1.5	±0.90	1.5	LSB
E_O	Offset error	---	-1.2	±0.09	1.2	%FSR
E_G	Gain error	---	-4.16	±0.75	4.16	%FSR
V_{REF}	Reference output voltage	---	0.965	0.985	1.035	V
V_{OH}	Digital output high level voltage	---	2.4	2.5		V
VOL	Digital output low level voltage	---		0.003	0.1	V
I_{DDA}	Simulated power supply current	---		124	138	mA
I_{DDD}	Digital power supply current	---		6	10	mA
P_W	Power consumption	---		390	4 14	mW
SNR	Signal-to-noise ratio	---	65	67.8		dB
SINAD	Signal-to-noise ratio	---	64.5	67.5		dB
SFDR	Stray dynamic range	---	70	82		dB
S_R	Conversion rate	---	50			MSPS

9. Pin Configuration and Pin Functions



Pin Functions

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	NC	null	17	D10	Data output bit D10
2	IN $_{CLK}$	Clock input	18	D11	Data output bit D11
3	NC	null	19	D12	Data output bit D12
4	PDWN	Power saving function selection	20	D13	Data output bit D13 (MSB)
5	D0	Data output bit D0 (LSB)	21	OR	Over-range indication
6	D1	Data output bit D1	22	MODE	Data output mode selection
7	D2	Data output bit D2	23	SENSE	Reference mode selection
8	D3	Data output bit D3	24	V $_{REF}$	Reference voltage
9	D4	Data output bit D4	25	V $_{REF-}$	Differential reference negative terminal
10	D5	Data output bit D5	26	V $_{REF+}$	Differential reference positive terminal
11	D6	Data output bit D6	27	V $_{DDA}$	Analog power supply
12	D7	Data output bit D7	28	GND $_{A}$	Analog ground
13	D8	Data output bit D8	29	IN +	Differential input positive terminal
14	D9	Data output bit D9	30	IN-	Differential input negative terminal
15	GND $_{D}$	Digital	31	GND $_{A}$	Analog ground
16	V $_{DDD}$	Digital power supply	32	V $_{DDA}$	Analog power supply

10. Main characteristic curves (electrical characteristic test graphs)

- **FFT spectrum under simulated input of 1MHz**

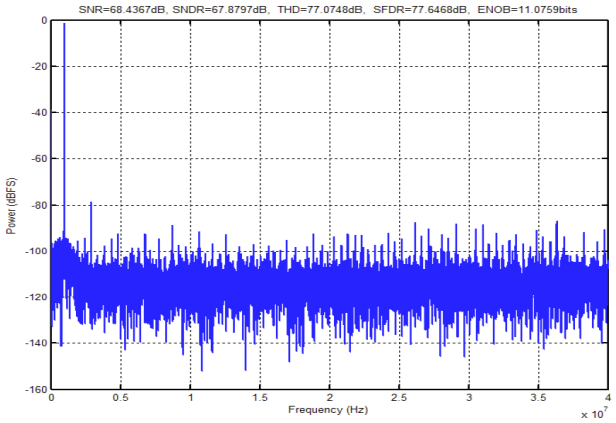


Figure 2. FFT spectrum at f_{CLK} = 50MHz and f_{in} = 1MHz

- **FFT spectrum under simulated input of 10MHz**

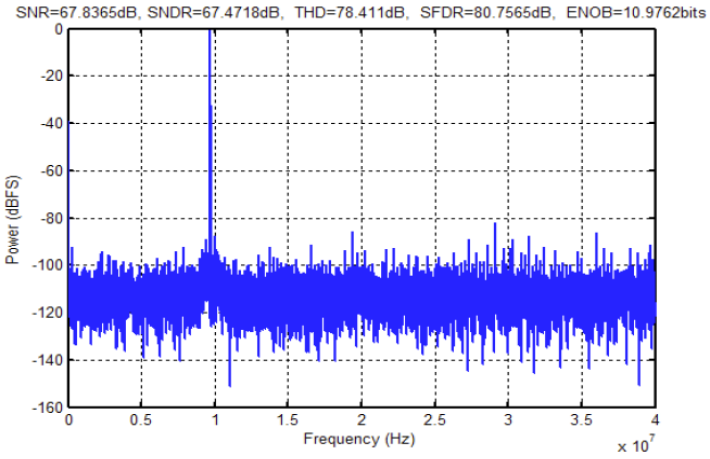


Figure 3. FFT spectrum at f_{CLK} = 50MHz and f_{in} = 10MHz

- **Differential error (E_{DL}) curve**

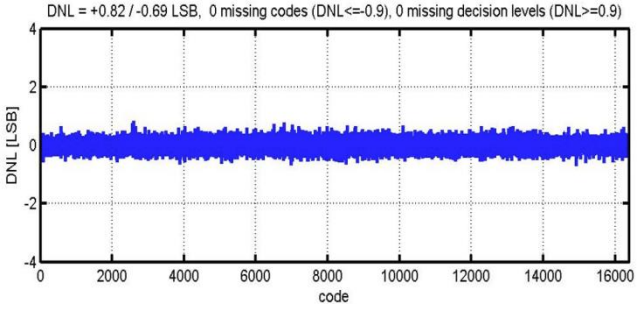


Figure 4. Differential error (E_{DL}) test curve

- **Linearity error (E_L) curve**

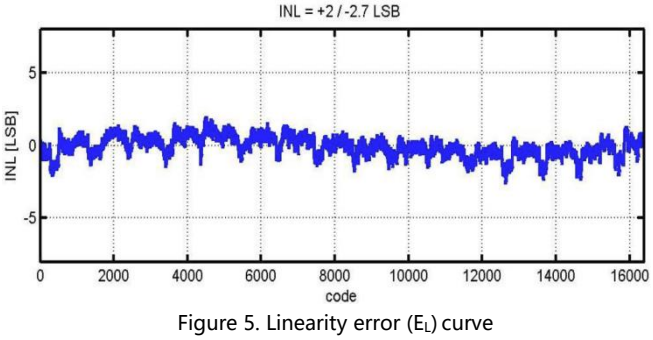


Figure 5. Linearity error (E_L) curve

11. Typical Applications

- **Analog input range and reference voltage selection**

The ADCP9245-20 has an analog input range of 1V $_{PP}$ to 2V $_{PP}$, and the reference voltage can be adjusted according to the analog input range. The circuit internally generates a stable and accurate reference voltage. An internal or external reference can be selected, and the reference voltage value can also be determined through programming (see Figure 6). The usage is controlled by the SENSE terminal for the reference voltage selection. The analog input range and reference voltage selection are shown in Table 1.

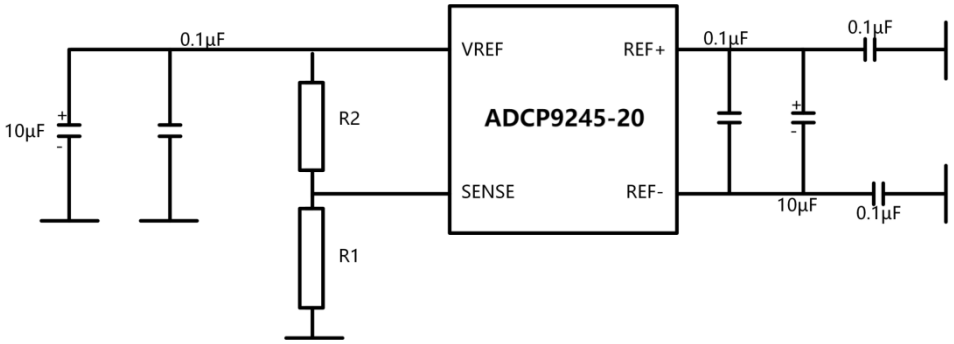


Figure 6. Connection diagram for programmable reference voltage.

Table 1. Connection Table for Analog Input Range and Reference Voltage Selection

Work mode	Induced voltage	Reference voltage output V $_{REF}$	Differential analog input peak voltage V_{PP}
External reference voltage	V $_{DDA}$	---	2×Applied Reference Voltage
Fixed internal reference voltage	V $_{REF}$	0.5V	1.0V
Programmable reference voltage (see Figure 6)	0.2V ~ V $_{REF}$	0.5V×(1+R2/R1)	2×V $_{REF}$
Fixed internal reference voltage	≤0.2V	1.0V	2.0V

- **Power saving mode**

This product features a power-saving mode control terminal PDWN. When PDWN is high, the circuit is in power-saving mode, consuming only 15mW, and all outputs are in a high-impedance state. When PDWN is low, the circuit is in normal operating mode. The power-saving mode control is shown in Table 2.

Table 2. ADCP9245-20 Power Saving Mode Control Table

PDWN	Function
H	Power saving mode
L	Normal work

Note: The PDWN control level is the CMOS level, and floating is low (L).

- **Output data format and clock stabilization function**

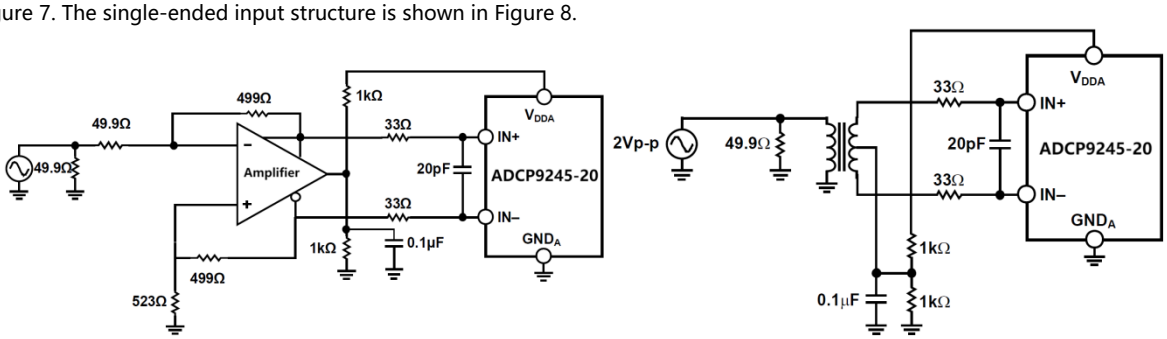
The ADCP9245-20 outputs data in two formats: binary two's complement and binary offset code. Users can control these formats via MODE as needed. The circuit also contains an internal clock stabilization circuit, which can also be selected via MODE, as shown in Table 3.

Table 3. Output Data Format and Clock Stabilization Function Control Table for ADCP9245-20

MODE	Output data format	Clock stabilization function
V $_{DDA}$	Binary two's complement	Off
2/3 V $_{DDA}$	Binary two's complement	Open
1/3 V $_{DDA}$	Binary offset code	Open
GND $_{A}$ (default value)	Binary offset code	Off

- **Analog Input**

The ADCP9245-20 analog input can be either differential or single-ended. Differential input can be driven by an amplifier or a transformer, as shown in Figure 7. The single-ended input structure is shown in Figure 8.



Amplifier drive Transformer drive

Figure 7. Differential Input Structure

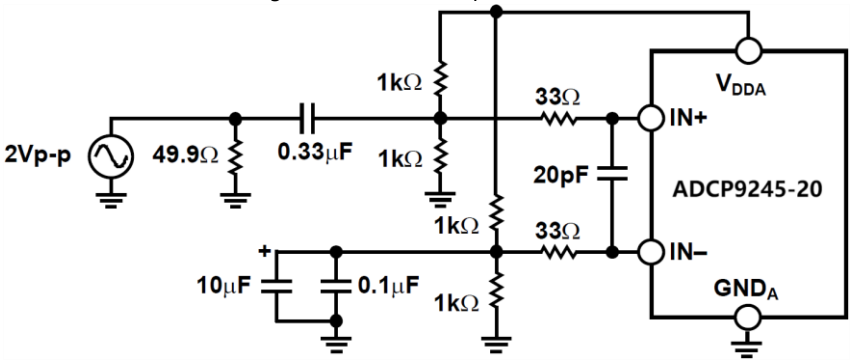


Figure 8. Single -ended input structure

12. Precautions

- **Product installation precautions:**

1) Please pay attention to the orientation of the components when soldering to avoid soldering them incorrectly.

2) All instruments and meters used for debugging circuits must have a good unified grounding. PCB board design must ensure good grounding and power decoupling.

3) Care should be taken not to reverse the power supply or short-circuit the input/output terminals with the power supply, as this can easily damage the circuit.

4) Electrical installation instructions:

a) This product has a moisture sensitivity rating of MSL3. The permissible time for the product to be exposed to the external environment after being removed from the moisture-proof bag, dried, or baked until reflow soldering is: ≤30℃/60RH%, 168h workshop life.

b) If the product is not dried and stored before assembly, it needs to be baked at 125℃ for 12~24 hours to remove internal moisture (Note: After the product is baked, the environment is particularly dry and static electricity is easily generated, so pay attention to ESD protection).

c) For board-level assembly, leaded reflow soldering (Sn63Pb37) is recommended. The recommended peak temperature range is 210℃~230℃, and the maximum peak temperature is not recommended to exceed 245℃. The dwell time within ±5℃ of the peak temperature should be ≤20s, and the dwell time above the liquidus line should be 60~90s. The heating rate should be ≤3℃/s, and the cooling rate should be ≤6℃/s.

d) If using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230℃~245℃, and the maximum peak temperature should not exceed 260℃. The dwell time within ±5℃ of the peak temperature should be ≤20s, and the dwell time above the liquidus line should be 60~90s. The heating rate should be ≤3℃/s, and the cooling rate should be ≤6℃/s.

e) The surface treatment of the welded ends of this product is electroplating with pure tin.

f) The side pads of this product are bare copper and do not have solder wettability. No soldering or tinning is required on the sides .

- **Product usage precautions:**

1) Power-on requirements: It is recommended to power on the analog power supply and the digital power supply simultaneously, or to power on the analog power supply first.

2) To ensure the dynamic performance of the circuit, it is recommended that the logic input high level of the logic input ports (IN_{CLK}, PDWN) be ≥2.8V and the logic input low level be ≤0.2V .

3) When using an operational amplifier in the ADCP9245-20 front end, the output swing of the operational amplifier must be greater than the analog input range of the ADCP9245-20 to ensure the integrity of the input signal.

4) The decoupling capacitors for the ADCP9245-20 reference output terminals (V_{REF}, V_{REF+}, V_{REF-}) should be capacitors with low ESR.

5) In applications, it is recommended to ground the PCB over a large area. This can eliminate potential differences that may exist due to different grounding points, and at the same time reduce the impact of capacitance generated by the circuit board on the circuit.

6) Each power supply pin needs to be connected to a 1μF or 0.1μF capacitor nearby.

7) For analog inputs, if differential inputs are used, the traces in the differential input section must be of equal length.

8) Digital power supplies and analog power supplies need to be separated.

9) Keep digital output traces as short as possible, and it is recommended to connect a digital driver to the output stage.

- **Product protection precautions:**

This product has an electrostatic discharge rating of 1C. During testing, handling, and storage, attention should be paid to electrostatic protection. The storage environment for this product is: temperature 10℃～25℃, relative humidity 25%～70%.

14. Packaging Information

External dimensions

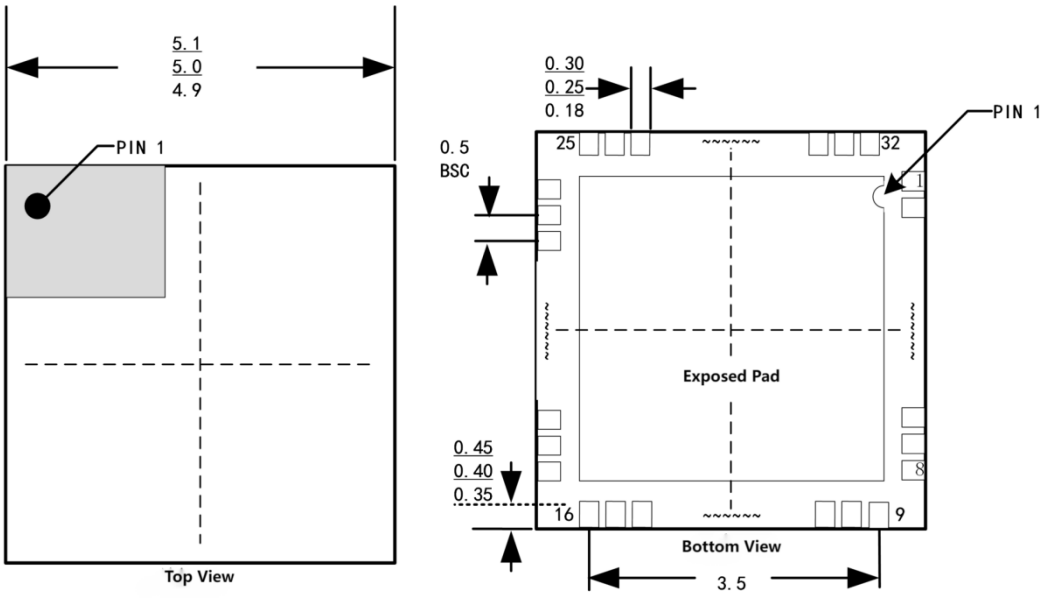


Figure 9. QFN32 Package dimensions

15. Ordering Guide

Model	Temperature range	Package Description	Package
ADCP9245-20	-45 °C to +85°C	QFN32	490/Reel