ADCP9230-210, 12-Bit, 210MSPS, 1.8V ADC

1. Features

- SNR =67 dBFS @ fIN =141MHz, -7.0dB @ 210MSPS
- ENOB = 10.84bit @ fIN =141MHz, -7.0dB @ 210MSPS
- SFDR = 86.83dBFS @ fIN =141MHz, -7.0dB @ 210MSPS
- Typical DNL values are +1.1/-0.91 LSB.
- Typical INL values are +0.85/-2.2 LSB.
- Provides a 250MSPS LVDS output interface (ANSI-644 level).
- 700MHz full power signal bandwidth
- Built-in reference level output
- Low power consumption
  703.8mW @ 210MSPS – LVDS SDR mode
  671.4mW @ 210MSPS – LVDS DDR Mode
- Configurable input signal range:
  From 0.98Vpp to 1.5Vpp, with a default value of 1.25Vpp.
- 1.8V power supply voltage for analog and digital circuits
- Operating temperature range: -40℃ to +85℃
- Configurable digital output formats, including binary offset code, binary two's complement, and Gray code.
- Internally integrated module for stabilizing clock duty cycle
- Internally integrated clock for sampling digital output signals
- QFN56 package

2. Applications

- Wireless and wired broadband communication systems
- Cable reflection path
- Communication system testing instruments
- Radar and satellite systems
- Power amplifier linearization

3. Overview

The ADCP9230-210 is a high-performance, low-power 12-bit analog-to-digital converter (ADC) with a maximum sampling rate of 250 MSPS, providing high dynamic performance for wideband signal sampling (SFDR = 86 dBFS @ (fin = 141 MHz, -7 dBFS, FCLK = 210 MSPS)). The chip is packaged in a 56-pin QFN package and integrates a voltage reference source, sampling clock, etc., providing a complete signal conversion solution. The ADCP9230-210 uses a 1.8V analog power supply and differential clock input. The digital output uses an LVDS (ANSI-664) interface, and the encoding can be binary two's complement, binary offset code, or Gray code. The chip also provides a clock signal for sampling the digital output signal. The ADCP9230-210's most significant feature is its excellent wideband dynamic performance (SFDR = 67 dBFS / SNR = 57 dBFS @ (fin = 491 MHz, -1 dBFS, FCLK = 210 MSPS). Furthermore, the chip uses an LVDS digital output interface and provides a clock output for digital signal sampling, making it easy to integrate with FPGAs. The chip operates on a 1.8V power supply and integrates an internal voltage reference source, making it easy for systems to use. Its operating mode can be configured via SPI, such as disabling the clock duty cycle stabilization module, adjusting the input signal range, and changing the digital output code, offering excellent flexibility.

4. Device packaging information

Product Model	Packaging Type	Package size
ADCP9230-210	QFN56	8mm×8mm

5. Functional Block Diagram

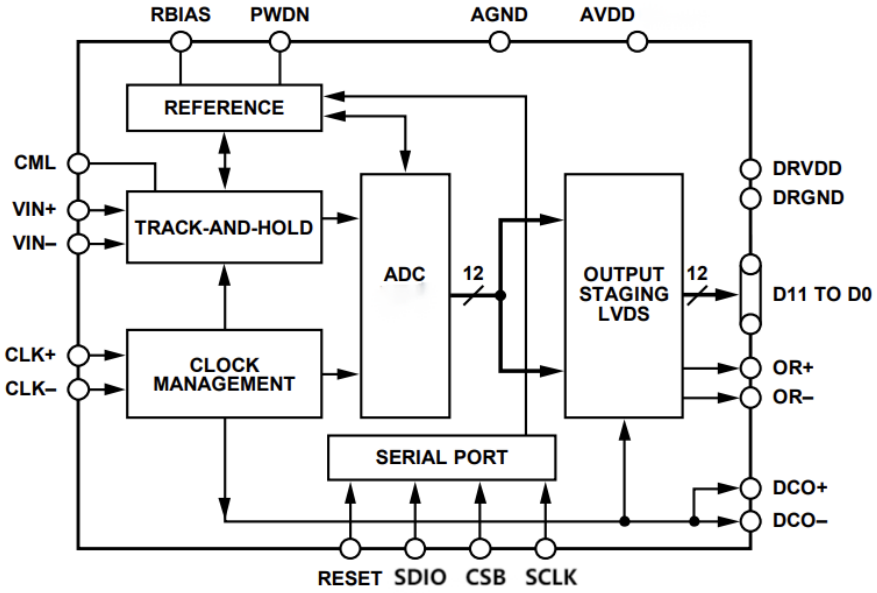

Figure 1. Functional Block Diagram

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6. Pin Configuration and Functions

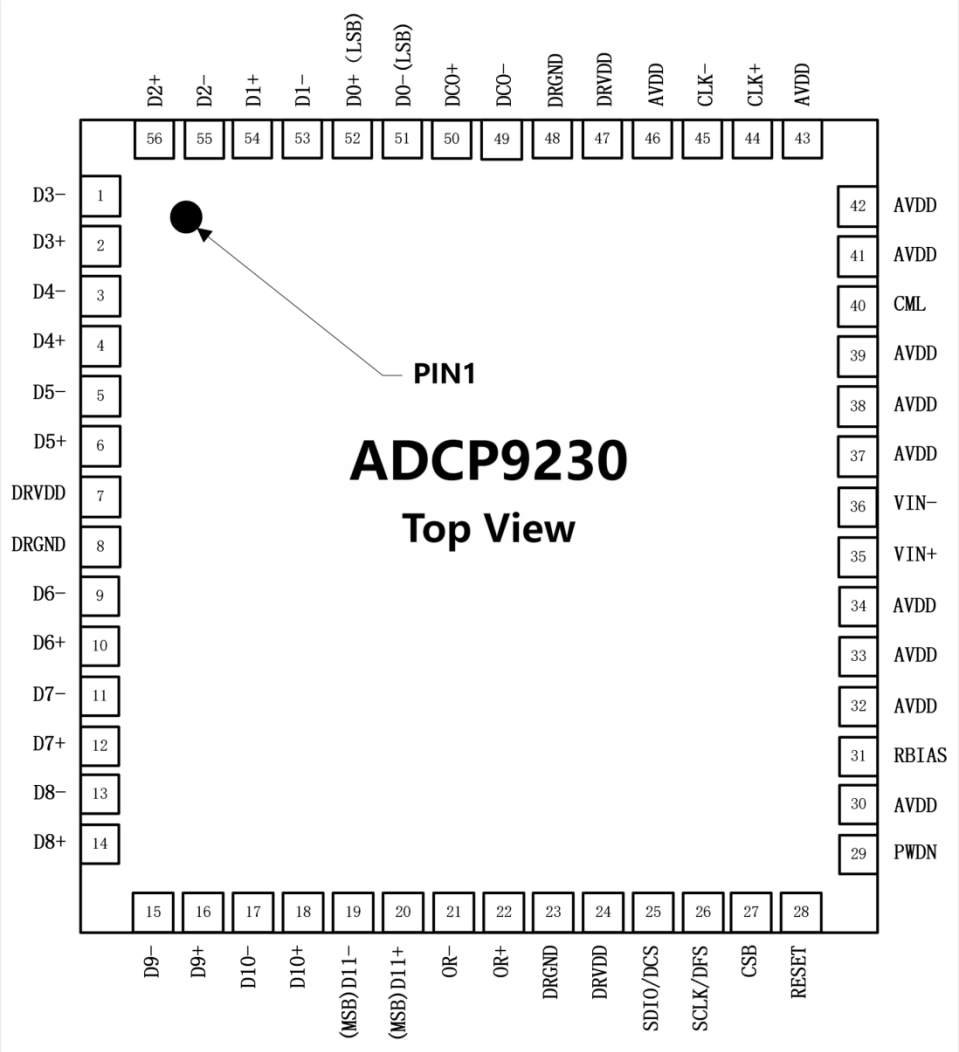


Figure 2. Single Data Rate (SDR) Mode Pin Configuration

Single data rate mode pin description

Pin name	Pin number	Description
AVDD	30, 32, 33, 34, 37, 38, 39, 41, 42, 43, 46	1.8V analog power supply
DRVDD	7, 24, 47	1.8V digital power supply
AGND	0	Analog
DRVDD	8, 23, 48	Digital
VIN+	35	Analog input positive terminal
VIN-	36	Analog input negative terminal
CML	40	The output common-mode pin, enabled via SPI control, provides a common-mode reference voltage for the input analog signal.
CLK+	44	Clock input positive terminal
CLK-	45	Clock input negative terminal
RBIAS	31	Chip bias current pin. (1% tolerance, 10kΩ resistor to ground) Typical voltage 0.5V.
RESET	28	Chip reset (active low)
SDIO/DCS	25	Serial port interface data input/output (serial port mode); Duty cycle stabilizer selection (external pin mode).
SCLK/DFS	26	Serial interface clock (serial port mode); data format selection pin (external pin mode).
CSB	27	Serial interface chip selection (active low)
PWDN	29	Chip sleep enable
DCO-	49	Data clock output negative terminal
DCO+	50	Data clock output positive terminal
D0-	51	D0 Output negative terminal
D0+	52	D0 Output positive terminal
D1-	53	D1 Output negative terminal
D1+	54	D1 Output positive terminal
D2-	55	D2 Output negative terminal
D2+	56	D2 Output positive terminal
D3-	1	D3 Output negative terminal
D3+	2	D3 Output positive terminal
D4-	3	D4 Output negative terminal
D4+	4	D4 Output positive terminal
D5-	5	D5 Output negative terminal
D5+	6	D5 Output positive terminal
D6-	9	D6 Output negative terminal
D6+	10	D6 Output positive terminal
D7-	11	D7 Output negative terminal
D7+	12	D7 Output positive terminal
D8-	13	D8 Output negative terminal
D8+	14	D8 Output positive terminal
D9-	15	D9 Output negative terminal
D9+	16	D9 Output positive terminal
D10-	17	D10 Output negative Terminal
D10+	18	D10 Output positive terminal
D11-	19	D11 Output negative terminal (most significant bit).
D11+	20	D11 Output positive terminal (most significant bit).
OR-	21	Output range overflow determination negative terminal
OR+	22	Output range overflow determination positive terminal

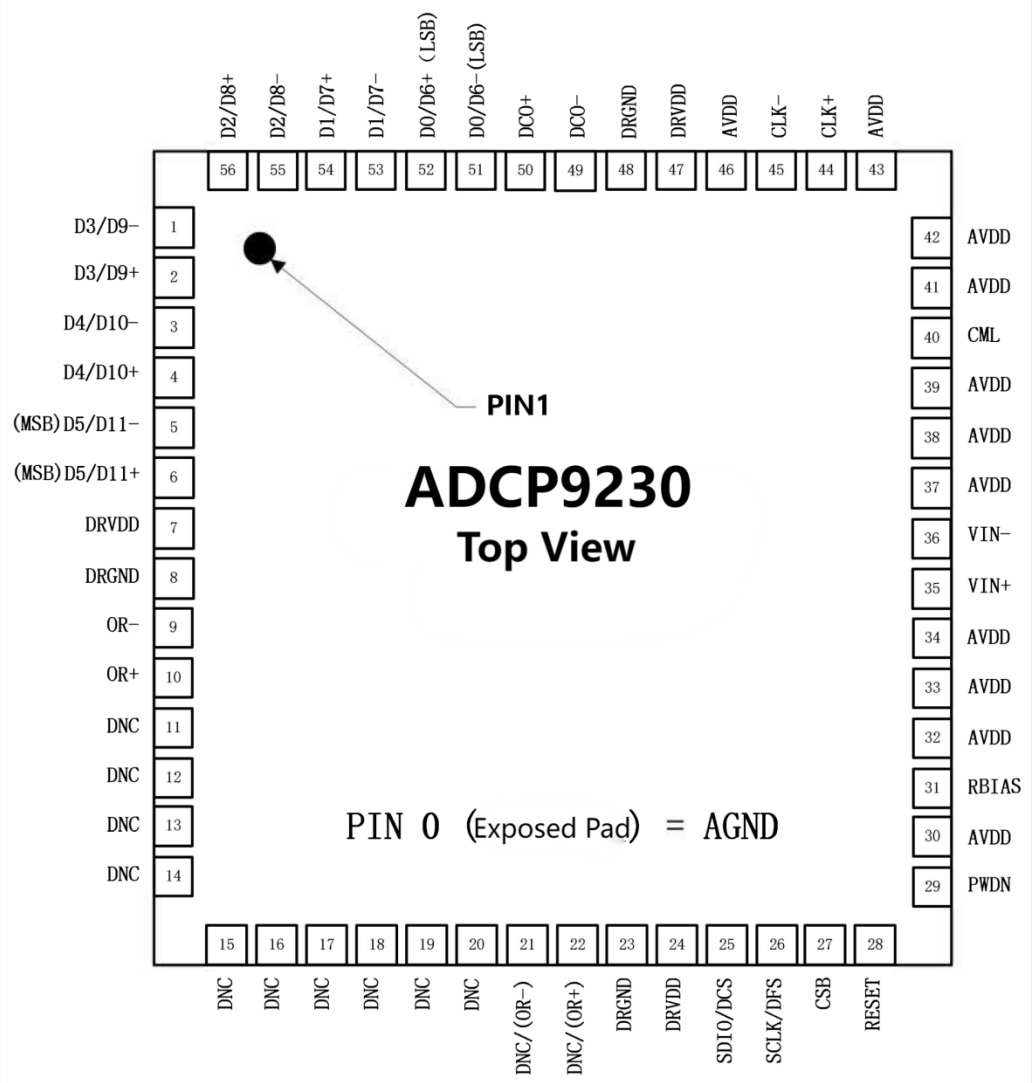


Figure 3. Pin configuration for Dual Data Rate (DDR) mode

Dual Data Rate Mode Pin Description

Pin name	Pin number	Description
AVDD	30, 32, 33, 34, 37, 38, 39, 41, 42, 43, 46	1.8V analog power supply
DRVDD	7, 24, 47	1.8V digital power supply
AGND	0	Analog
DRVDD	8, 23, 48	Digital
VIN+	35	Analog input positive terminal
VIN-	36	Analog input negative terminal
CML	40	The output common-mode pin, enabled via SPI control, provides a common-mode reference voltage for the input analog signal.
CLK+	44	Clock input positive terminal
CLK-	45	Clock input negative terminal
RBIAS	31	Chip bias current pin. (1% tolerance, 10kΩ resistor to ground) Typical voltage 0.5V.
RESET	28	Chip reset (active low)
SDIO/DCS	25	Serial port interface data input/output (serial port mode); Duty cycle stabilizer selection (external pin mode).
SCLK/DFS	26	Serial interface clock (serial port mode); data format selection pin (external pin mode).
CSB	27	Serial interface chip selection (active low)
PWDN	29	Chip sleep enable
DCO-	49	Data clock output negative terminal
DCO+	50	Data clock output positive terminal
D0/D6-	51	D0/D6 output negative terminals
D0/D6+	52	D0/D6 output positive terminals
D1/D7-	53	D1/D7 output negative terminal
D1/D7+	54	D1/D7 output positive terminals
D2/D8-	55	D2/D8 output negative terminal
D2/D8+	56	D2/D8 output positive terminals
D3/D9-	1	D3/D9 output negative terminal
D3/D9+	2	D3/D9 output positive terminals
D4/D10-	3	D4/D10 output negative terminal
D4/D10+	4	D4/D10 output positive terminal
D5/D11-	5	D5/D11 output negative terminal
D5/D11+	6	D5/D11 output positive terminal
OR-	9	Output range overflow determination negative terminal
OR+	10	Output range overflow determination positive terminal
DNC	1 to 20	Suspended and unconnected
DNC/(OR-)	21	Floating and unconnected (this pin can be configured via the serial port as the negative terminal for output range overflow determination)
DNC/(OR+)	22	Floating and unconnected (this pin can be configured via the serial port as the negative terminal for output range overflow determination)

7. Electrical Static Characteristics

AVDD=1.8V, DRVDD=1.8V, T_{MIN} = -40℃, T_{MAX} = +85℃, A_{IN} = -7.0dBFS, input signal range=1.5Vpp, DCS off, unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Resolution			12		Bits
Accuracy					
No error rate	Full temperature				
Offset Error	25℃				mV
	Full temperature				mV
Gain Error	25℃				%FS
	Full temperature				%FS
Differential Nonlinearity (DNL)	25℃	-0.91		1.1	LSB
	Full temperature				LSB
Integral nonlinearity (INL)	25℃	-2.2		0.85	LSB
	Full temperature				LSB
Temperature drift			35		Ppm
Offset Error	Full temperature				μV/℃
Gain Error	Full temperature				%/℃
Analog Input					
Differential input voltage range [1]	Full temperature	0.98		1.5	Vp-p
Input common mode voltage	Full temperature		1.0		V
Differential input impedance	Full temperature		2		kΩ
Input capacitor	25℃		6		pF
Power consumption characteristics					
Analog power supply voltage (AVDD)	Full temperature	1.7	1.8	1.9	V
Digital power supply voltage (DRVDD)	Full temperature	1.7	1.8	1.9	V
Analog power supply current (I_{AVDD}) [2]	Full temperature		312		mA
Digital power supply current (I_{DRVDD}) [2] Single Data Rate (SDR) Mode [3]	Full temperature		79		mA
Digital power supply current (I_{DRVDD}) [2] Dual Data Rate (DDR) Mode [4]	Full temperature		60		mA
Chip Power Consumption/Single Data Rate (SDR) Mode [3]	Full temperature		703.8		mW
Chip power consumption/Dual data rate (DDR) mode [4]	Full temperature		671.4		mW

1. The differential input voltage range can be configured via SPI, with a default value of 1.25Vp-p.
2. Analog and digital power supply currents were tested at -1dBFS and a 10.3MHz input signal.
3. The single data rate mode is the default configuration of ADCP9230QN.
4. Dual data rate mode is a user-selectable mode that can be configured via SPI.

8. Electrical Dynamic Characteristics

AVDD=1.8V, DRVDD=1.8V, T_{MIN} = -40℃, T_{MAX} = +85℃, A_{IN} = -7.0dBFS, input signal range=1.5Vpp, DCS off, unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Signal-to-noise ratio (SNR)					
f_{IN} = 16MHz	25℃				dBFS
	Full temperature				dBFS
f_{IN} = 80MHz	25℃				dBFS
	Full temperature				dBFS
f_{IN} = 141MHz	25℃		67		dBFS
f_{IN} = 160MHz	25℃				dBFS
f_{IN} = 220MHz	25℃				dBFS
Signal-to-noise ratio (SINAD)					
f_{IN} = 16MHz	25℃				dBFS
	Full temperature				dBFS
f_{IN} = 80MHz	25℃				dBFS
	Full temperature				dBFS
f_{IN} = 141MHz	25℃		61.8		dBFS
f_{IN} = 160MHz	25℃				dBFS
f_{IN} = 220MHz	25℃				dBFS
Significant digits (ENOB)					
f_{IN} = 16MHz	25℃				Bits
	Full temperature				Bits
f_{IN} = 80MHz	25℃				Bits
	Full temperature				Bits
f_{IN} = 141MHz	25℃		10.84		Bits
f_{IN} = 160MHz	25℃				Bits
f_{IN} = 220MHz	25℃				Bits
Worst harmonic (second or third order)					
f_{IN} = 16MHz	25℃				dBFS
	Full temperature				dBFS
f_{IN} = 80MHz	25℃				dBFS
	Full temperature				dBFS
F_{IN} = 141MHz	25℃		86		dBFS
f_{IN} = 160MHz	25℃				dBFS
f_{IN} = 220MHz	25℃				dBFS
Worst of all (noise other than HD2 and HD3)					
f_{IN} = 16MHz	25℃				dBFS
	Full temperature				dBFS
f_{IN} = 80MHz	25℃				dBFS
	Full temperature				dBFS
f_{IN} = 141MHz	25℃		87.8		dBFS
f_{IN} = 160MHz	25℃				dBFS
f_{IN} = 220MHz	25℃				dBFS
Two-Tone IMD					
140.2MHz/141.3MHz@-7dBFS	25℃		72		dBFS
170.2MHz/171.3MHz@-7dBFS	25℃		68		dBFS
Front-end analog input bandwidth			700		MHz

9. Digital Characteristics

AVDD=1.8V, DRVDD=1.8V, T_{MIN} = -40℃, T_{MAX} = +85℃, A_{IN} = -7.0dBFS, input signal range=1.5Vpp, DCS off, unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Clock input					
Logical compatibility	Full temperature	CMOS/LVDS/LVPECL			
Internal common-mode bias	Full temperature		1.2		V
Differential input voltage	Full temperature		0.2		Vp-p
Input voltage range	Full temperature	AVSS		AVDD	
Input common mode range	Full temperature	1		AVDD	V
High-level input voltage (V_{IH})	Full temperature	1.2		AVDD	V
Low-level input voltage (V_{IL})	Full temperature	0		0.8	V
High-level input current (I_H)	Full temperature	-10		+10	μA
Low-level input current (I_L)	Full temperature	-10		+10	μA
Differential input impedance	Full temperature		1 8		kΩ
Input capacitor	Full temperature		4		pF
Logical input					
Logic 1 voltage	Full temperature	0.8xVDD			V
Logic 0 voltage	Full temperature			0.2xAVDD	V
Logic 1 Input Current (SDIO)	Full temperature		0		μA
Logic 0 Input Current (SDIO)	Full temperature		- 60		μA
Logic 1 input current (SCLK,PDWN,CSB,RESET)	Full temperature		55		μA
Logic 0 input current (SCLK, PDWN, CSB, RESET)	Full temperature		0		μA
Input capacitor	25℃		4		pF
Logical output					
V_{OD} differential output voltage	Full temperature	247		454	mV
V_{OS} output DC offset voltage	Full temperature	1.125		1.375	V
Output encoding method	Two's complement, Gray code, offset binary code (default)				

10. Switching Characteristics

AVDD=1.8V, DRVDD=1.8V, T_{MIN} = -40℃, T_{MAX} = +85℃, A_{IN} = -7.0dBFS, input signal range=1.5Vpp, DCS off, unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Maximum conversion rate	Full temperature	2 10			MSPS
Minimum conversion rate	Full temperature			100	MSPS
CLK+ High Pulse Width (t_{CH})	Full temperature	2.15	2.4		ns
CLK+ Low pulse width (t_{CL})	Full temperature	2.15	2.4		ns
Output (LVDS – SDR mode)					
Data transmission delay (t_{PD})	Full temperature		4.1		ns
Rise time (t_R) (20% ~ 80%)	25℃		0.2		ns
Fall time (t_F) (20% ~ 80%)	25℃		0.2		ns
DCO transmission delay (t_{CPD})	Full temperature		4.1		ns
Offset of data to DCO (t_{SKEW})	Full temperature	-0.3	0.1	0.5	ns
Waiting time	Full temperature				Cycles
Output (LVDS – DDR mode)					
Data transmission delay (t_{PD})	Full temperature		4.1		ns
Rise time (t_R) (20% ~ 80%)	25℃		0.2		ns
Fall time (t_F) (20% ~ 80%)	25℃		0.2		ns
DCO transmission delay (t_{CPD})	Full temperature		4.1		ns
Offset of data to DCO (t_{SKEW})	Full temperature	-0.3	0.1	0.5	ns
Waiting time	Full temperature				Cycles
Clock jitter (t_J)	25℃		0.3		ps rms

11. Timing Diagram

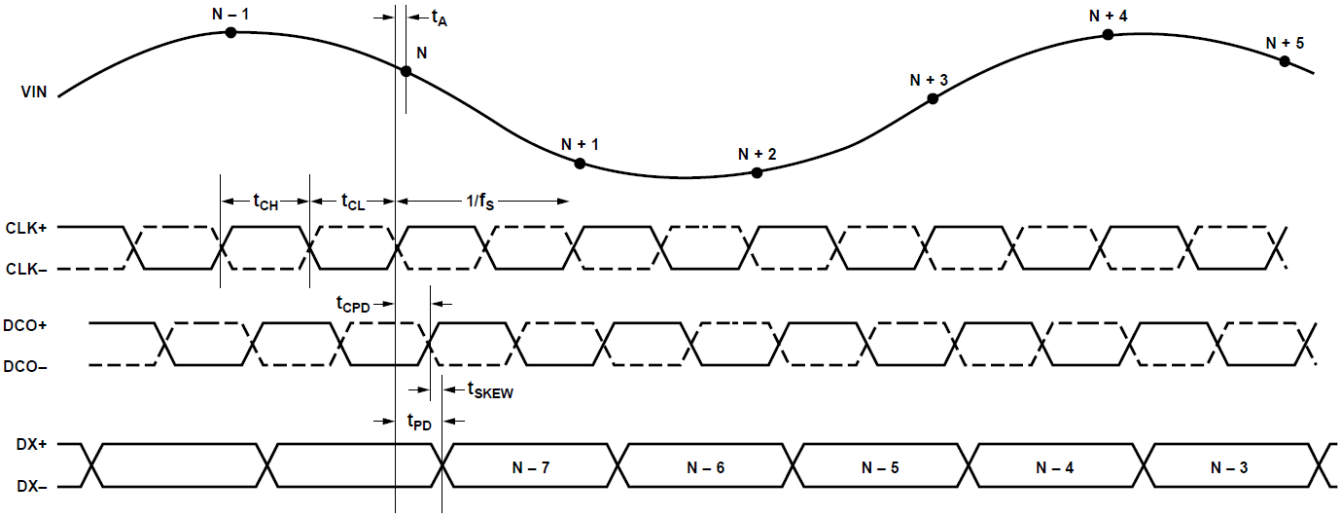


Figure 4. Single Data Rate Mode (SDR Mode)

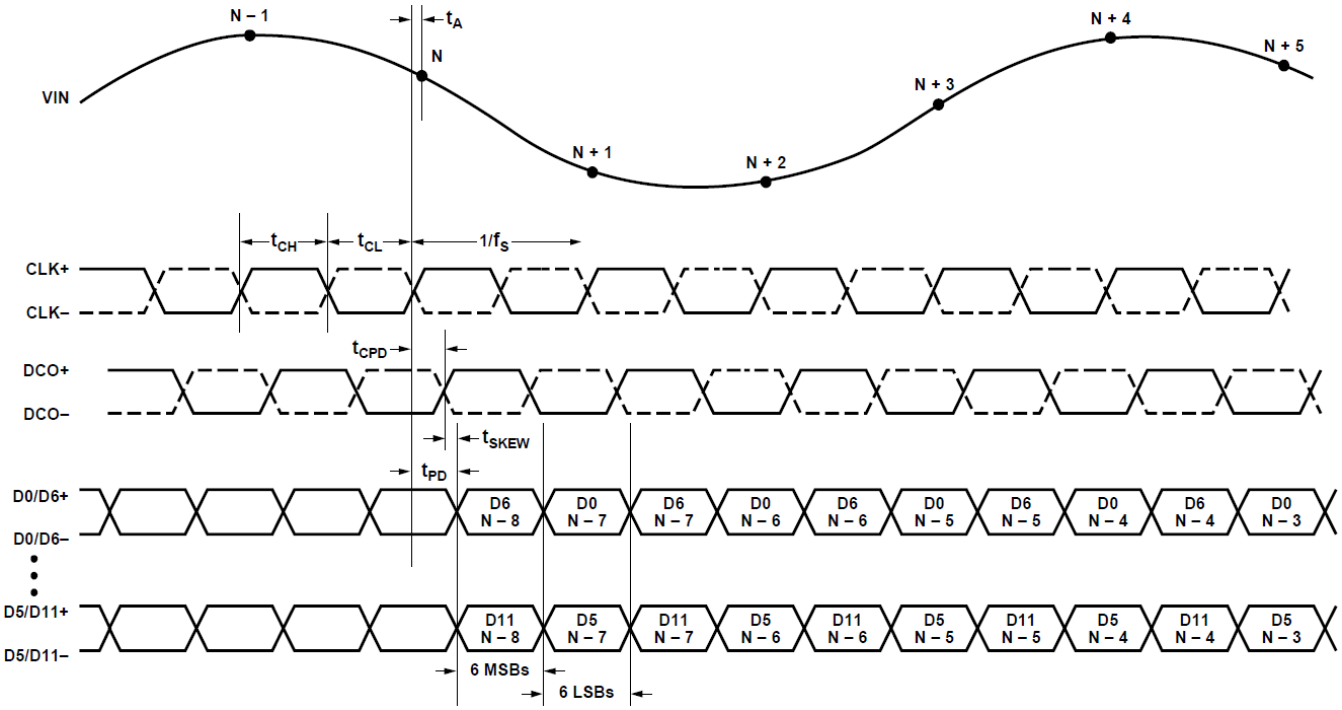


Figure 5. Dual Data Rate Mode (DDR Mode)

12. Functional Description

- **Serial interface description**

The three-wire serial interface at the input is timing compatible with the AD9230, and its clock frequency can reach up to 40MHz. The detailed interface timing is shown in Figure 6.

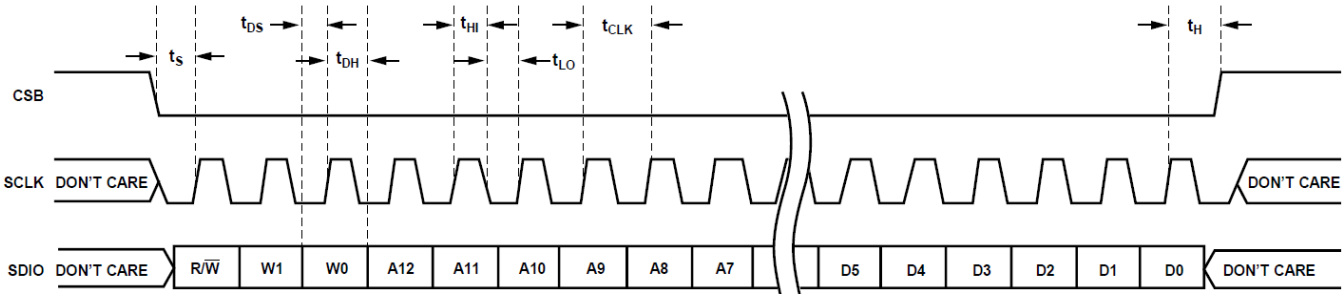


Figure 6. Serial interface timing

- **Output data encoding**

Analog input (V)	Condition(V)	Binary offset code (D11 ~ D0)	Binary two's complement (Two's Complement)	Gray Code	Overflow flag (OR)
VIN+ - VIN-	<-0.62	0000 0000 0000	1000 0000 0000	1000 0000 0000	1
VIN+ - VIN-	-0.62	0000 0000 0000	1000 0000 0000	1000 0000 0000	0
VIN+ - VIN-	0	1000 0000 0000	0000 0000 0000	0000 0000 0000	0
VIN+ - VIN-	0.62	1111 1111 1111	0111 1111 1111	0100 0000 0000	0
VIN+ - VIN-	>0.62+0.5LSB	1111 1111 1111	0111 1111 1111	0100 0000 0000	1

13. Register - related

- **Register configuration**

Note: The following register configurations differ from the default values. The following registers need to be configured during chip initialization.

ADDR	Value	Note
0x0F	0x02	CML Enable

- **Register table**

Address: 0x00, Default: 0x18

Bit	Symbol	Default	Functional Description
7:6		0x00	
5		0	Software reset When this bit is set to "1", all programmable bits, except for the COMM register bit which is unaffected by the software reset, will return to their power-on state. The software reset will remain active until this bit is cleared to 0 (inactive). 0: Not activated 1: Software reset activation
4:0		0x18	

Table 1. Chip Port Configuration (chip_port_config) Register

Address: 0x01, Default: 0x50

Bit	Symbol	Default	Functional Description
7:0	Chip_id	0x50	Unique ID

Table 2. Chip ID (Chip_ID) Register

Address: 0x02, Default: 0x00

Bit	Symbol	Default	Functional Description
7:5		0x00	
4:3	speed_grade	00	00=250MSPS ; 01=210MSPS ; 10=170MSPS
2:0		0x00	

Table 3. Chip-level (chip_grade) registers

Address: 0xFF, Default: 0x00

Bit	Symbol	Default	Functional Description
7:1		0x00	
0	reg_transfer	0	0: unused 1: Transfer register data from the master shift register to the slave register. Once the transfer is complete, the transfer register is automatically cleared.

Table 4. Device Update Registration (Contoso update)

Address: 0x08, Default: 0x00

Bit	Symbol	Default	Functional Description
7:3		0x00	
2:0	int_pwdn_mode	0x00	000 : Normal power on ; 001 : Power off ; 010 : Standby ; 011 : Reserved

Table 5. Modes Register

Address: 0x09, Default: 0x01

Bit	Symbol	Default	Functional Description
7:1		0x00	
0	dcs_ctrl	1	Duty cycle stabilizer (DCS bypassb): 0 : Enabled (default) ; 1 : Disabled

Table 6. Clock Register

Address: 0x0D, Default: 0x00

Bit	Symbol	Default	Functional Description
7:6		0x00	
5	rst_pn23	0	1: on 0: off
4	rst_pn9	0	1: on 0: off
3:0	output_test_mode	0x00	0001: midscale short 0010: Output all 1s, overflow=0 0011: Output all zeros, overflow=0 0100: Checker board output 0101: overflow=0, dout is PN23 0110: overflow=0, dout is PN9 0111: Output all 1s/all 0s inverted signal 1000~1110: unused 1111: Ramp Output

Table 7. Test I/O (test_io) Register

Address: 0x0F, Default: 0x00

Bit	Symbol	Default	Functional Description
7:2		0x00	
1	cml_en	0	1: cml enable ; 0: cml disable (default)
0		0	

Table 8. Analog Input Configuration (AIN_config) Register

Address: 0x14, Default: 0x00

Bit	Symbol	Default	Functional Description
7:5	Reserved	0x00	
4	output_en	0	Output: 0: Output is enabled (default) 1: Output is disabled.
3	ddr_enable	0	DDR control: 1: Enable DDR output mode 0: Disable DDR output mode (default)
2	output_invert	0	Output inversion control: 0: Off, outputs normal data (default) 1: On, outputs reversed data.
1: 0	data_format	0 0	Output format selection: 00: Output offset in binary (default) 01: 2's complement 10: Graymall 11: Undefined

Table 9. Output Mode Control (output_mode) Register

Address: 0x15, Default: 0x00

Bit	Symbol	Default	Functional Description
7:3		0x00	
2:0	lvdsfine_adj	000	LVDS fine current regulation: 000: Default 3.5mA 001: 3.5mA 010: 3.25mA 011: 3mA 100: 2.75mA 101: 2.5mA 110: 2.25mA 111: 2mA

Table 10. Output Adjustment Register

Address: 0x16, Default: 0x03

Bit	Symbol	Default	Functional Description
7	output_clk_polarity	0	
6:0		0x00	Output clock polarity control 1: Inverting clock output 0: Non-inverting clock output (default)

Table 11. Output Phase Register

Address: 0x17, Default: 0x00

Bit	Symbol	Default	Functional Description
7	output_delay_en	0	`output` default values: 0: Enabled (default) ; 1: Disabled.
6:5		0x00	
4:0		0x00	Output clock delay : 00000: 0.1ns 00001: 0.2ns ... 11110: 3.1ns 11111: 3.2ns

Table 12. Output Delay Control (FLEX_output_delay) Register

Address: 0x18, Default: 0x00

Bit	Symbol	Default	Functional Description
7:6		0x00	` output` default values: 0: Enabled (default) ; 1: Disabled.
5:0	ref_range	011000	Reference range adjustment: 10000: 0.98V 10001: 1.00V 10010: 1.02V 10011: 1.04V ... 11111: 1.23V 00000: 1.25V 00001: 1.27V ... 01110: 1.48V 01111: 1.50V

Table 13. Reference Range Control (REF_range_CTRL) Register

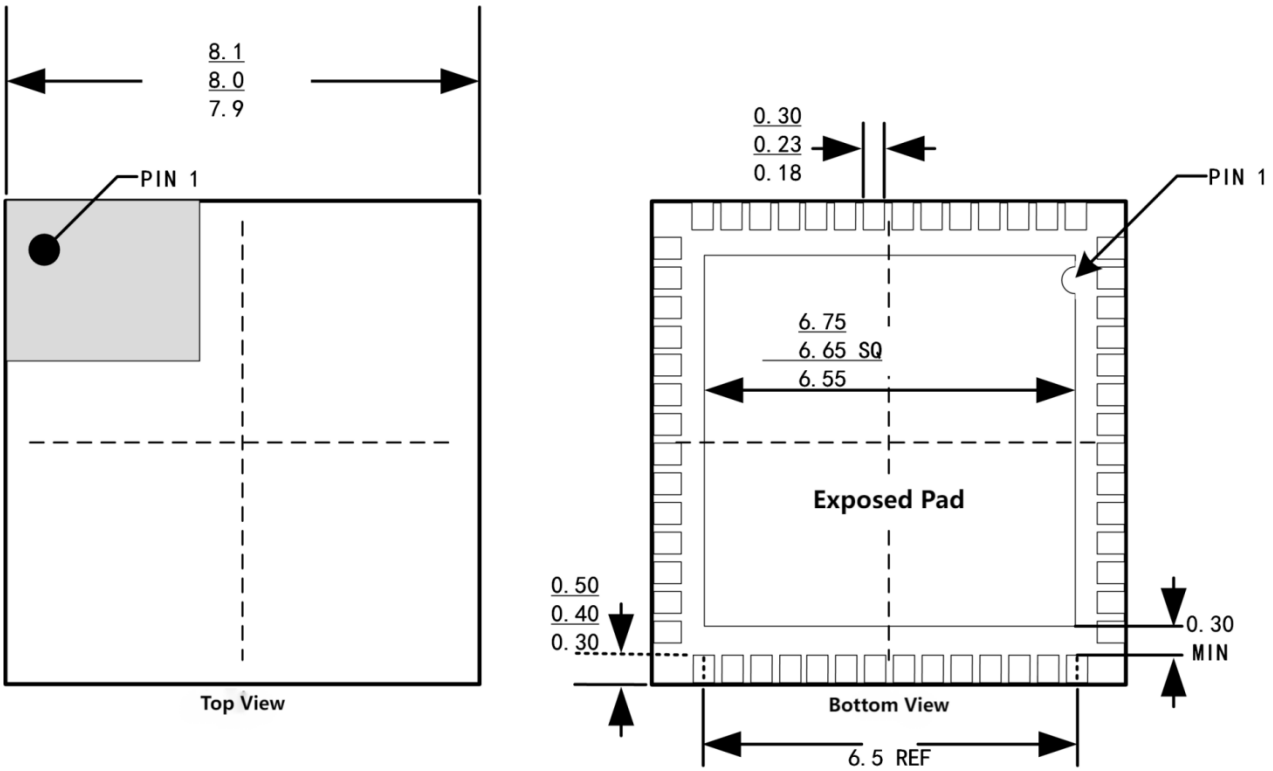
Address: 0x2A, Default: 0x01

Bit	Symbol	Default	Functional Description
7:2		0x00	` output` default values: 0: Enabled (default) ; 1: Disabled.
1	ovr_position	0	Overflow location (DDR mode only): 0 = pin 9, pin 10 1 = Pin 21, Pin 22
0	overrange_enable	1	overrange bit control1: 1: By default, out-of-range bits are enabled. 0: Disable out-of-range bit output

Table 14. Overrange Control (OVERRANGE_CTRL) Register

14. Packaging Dimensions and Structure

QFN56 package



15. Device Ordering Information

Model	Temperature Range	Packaging Type	Package Quantity
ADCP9230-210	-40 ℃ ~ 85 ℃	QFN56	260/reel