ADCP9230-200, 14-Bit, 200MSPS, 1.8V ADC

1. Features

- SNR =70 dBFS @ fIN =141MHz, -10.0dB @ 200MSPS
- SFDR = 82.00dBFS @ fIN =141MHz, -10.0dB @ 200MSPS
- Provides a 250MSPS LVDS output interface (ANSI-644 level).
- 700MHz full power signal bandwidth
- Built-in reference level output
- Low power consumption
  671.4mW @ 200MSPS – LVDS DDR Mode
- Configurable input signal range :
  From 1.3Vpp to 2.0Vpp
- 1.8V power supply voltage for analog and digital circuits
- Operating temperature range: -40℃ to +85℃
- Configurable digital output formats, including binary offset code, binary two's complement, and Gray code
- Internally integrated module for stabilizing clock duty cycle
- Internally integrated clock for sampling digital output signals
- QFN56 package

2. Applications

- Wireless and wired broadband communication systems
- Cable reflection path
- Communication system testing instruments
- Radar and satellite systems
- Power amplifier linearization

3. Overview

The ADCP9230-200 is a high-performance, low-power 14-bit analog-to-digital converter (ADC) with a maximum sampling rate of 200 MSPS, providing high dynamic performance for wideband signal sampling (SFDR = 82 dBFS @ (fin = 141 MHz, -10 dBFS, FCLK = 200 MSPS). The chip is packaged in a 56-pin QFN package and integrates a voltage reference source and sampling clock, providing a complete signal conversion solution. The ADCP9230-200 uses a 1.8V analog power supply and differential clock input. The digital output uses an LVDS (ANSI-664) interface, and the encoding can be binary two's complement, binary offset code, or Gray code. The chip also provides a clock signal for sampling the digital output signal. The ADCP9230-200 uses an LVDS digital output interface and provides a clock output for digital signal sampling, making it easy to integrate with FPGAs. The chip operates on a 1.8V power supply and integrates an internal voltage reference source, making it easy to use in systems. The chip's operating mode can be configured via SPI™ , such as disabling the clock duty cycle stabilization module, adjusting the input signal range, and changing the digital output code, providing excellent flexibility.

4. Device Packaging Information

Product Model	Packaging Type	Package Size
ADCP9230-200	QFN56	8mm×8mm

5. Functional Block Diagram

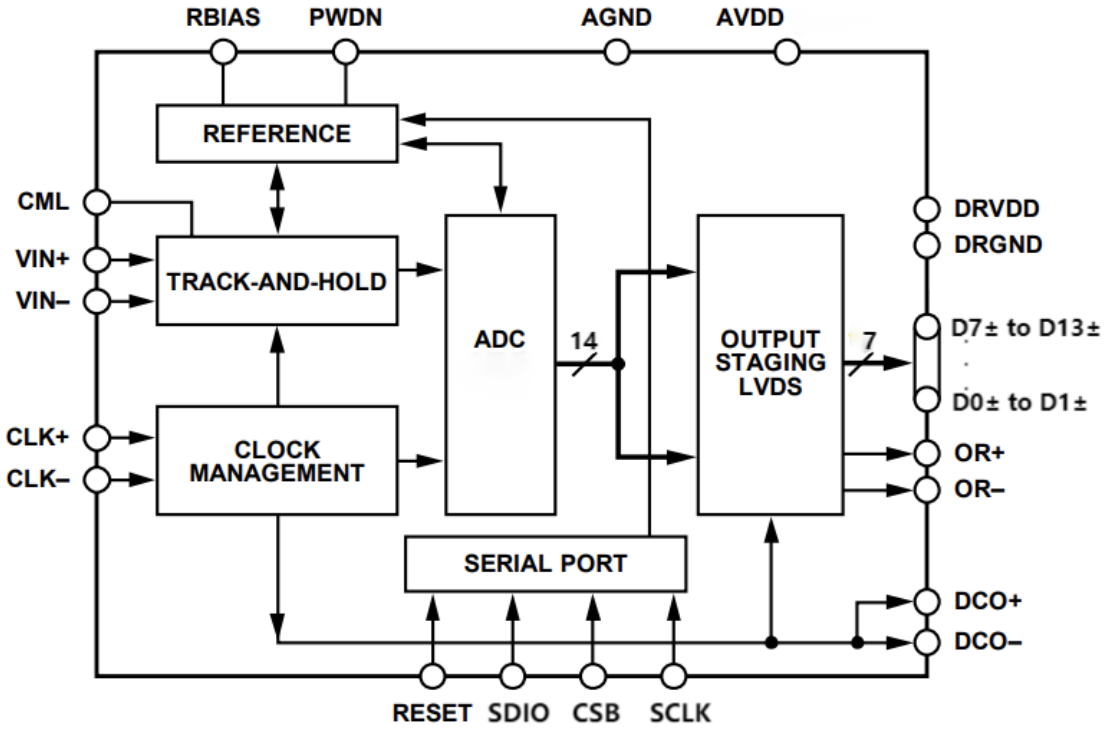

Figure 1. Functional Block Diagram

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6. Pin Configuration and Functions

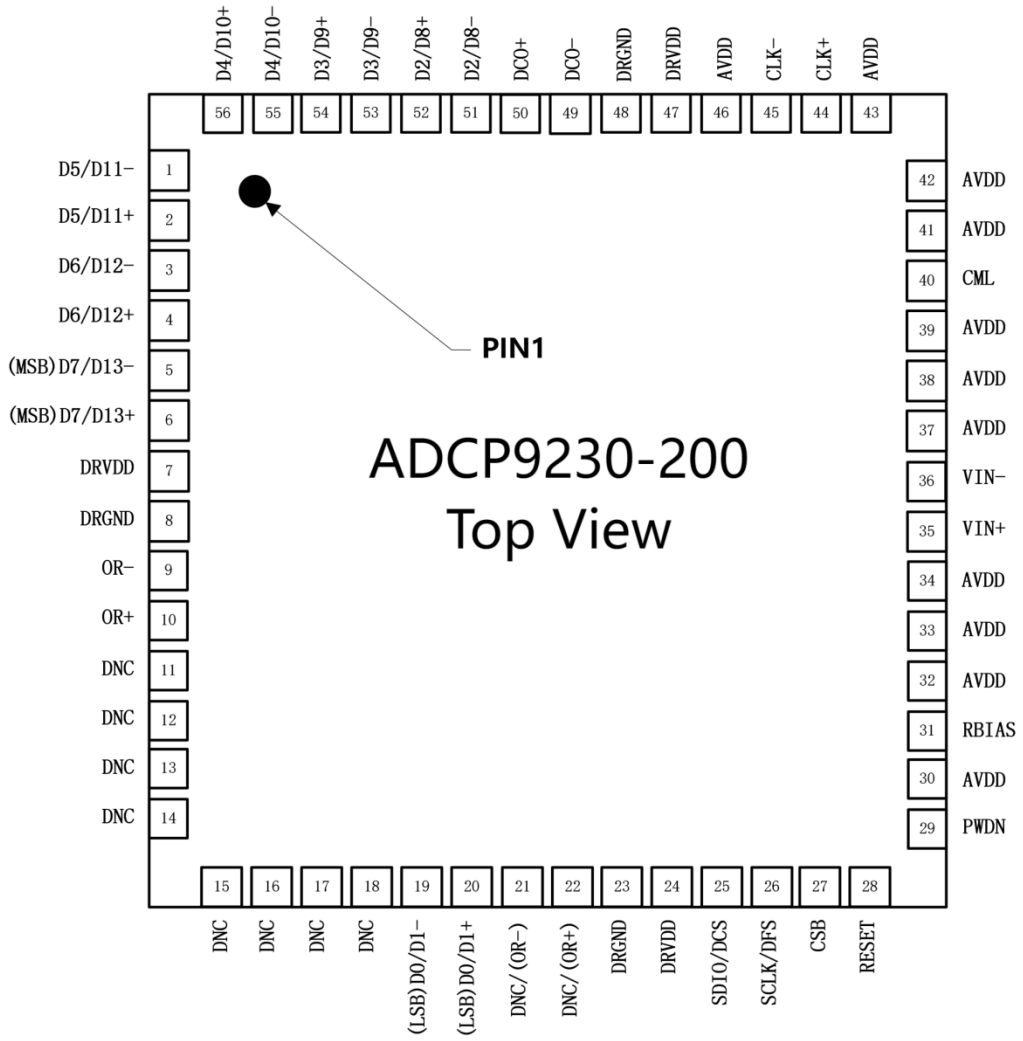


Figure 2. Pin configuration for Dual Data Rate (DDR) mode

Dual Data Rate Mode Pin Description

Pin Name	Pin No.	Description
AVDD	30, 32, 33, 34, 37, 38, 39, 41, 42, 43, 46	1.8V analog power supply
DRVDD	7, 24, 47	1.8V digital power supply
AGND	0	Analog
DRVDD	8, 23, 48	Digital
VIN+	35	Analog input positive terminal
VIN-	36	Analog input negative terminal
CML	40	The output common-mode pin, enabled via SPI control, provides a common-mode reference voltage for the input analog signal.
CLK+	44	Clock input positive terminal
CLK-	45	Clock input negative terminal
RBIAS	31	Chip bias current pin (with an external 10kΩ resistor to ground with 1% tolerance)
RESET	28	Chip reset (active low)
SDIO/DCS	25	Serial port interface data input/output (serial port mode); Duty cycle stabilizer selection (external pin mode).
SCLK/DFS	26	Serial interface clock (serial port mode); data format selection pin (external pin mode).
CSB	27	Serial interface chip selection (active low)
PWDN	29	Chip sleep enable
DCO-	49	Data clock output negative terminal
DCO+	50	Data clock output positive terminal
D2/D8-	51	D2/D8 output negative terminal
D2/D8+	52	D2/D8 output positive terminal
D3/D9-	53	D3/D9 output negative terminal
D3/D9+	54	D3/D9 output positive terminal
D4/D10-	55	D4/D10 output negative terminal
D4/D10+	56	D4/D10 output positive terminal
D5/D11-	1	D5/D11 output negative terminal
D5/D11+	2	D5/D11 output positive terminal
D6/D12-	3	D6/D12 output negative terminal
D6/D12+	4	D6/D12 output positive terminal
D7/D13-	5	D7/D13 output negative terminal
D7/D13+	6	D7/D13 output positive terminal
OR-	9	Output range overflow determination negative terminal
OR+	10	Output range overflow determination positive terminal
D NC	1 to 18	Suspended and unconnected
D0/D1-	19	D0/D1 output negative terminal
D0/D1+	20	D0/D1 output positive terminal
DNC/(OR-)	21	Floating and unconnected (this pin can be configured via the serial port as the negative terminal for output range overflow determination)
DNC/(OR+)	22	Floating and unconnected (this pin can be configured via serial port as the positive terminal for output range overflow detection)

7. Electrical Static Characteristics

AVDD=1.8V, DRVDD=1.8V, T_{MIN} = -40℃, T_{MAX} = +85℃, A_{IN} = -10.0dBFS, 200MSPS, input signal range=2.0Vpp, DCS off, unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Resolution			14		Bits
Accuracy					
No error rate	Full temperature		Guaranteed		
Offset Error	25℃		8.1		mV
	Full temperature				mV
Gain Error	25℃				%FS
	Full temperature				%FS
Differential Nonlinearity (DNL)	25℃		±1		LSB
	Full temperature				LSB
Integral nonlinearity (INL)	25℃		±3		LSB
	Full temperature				LSB
Analog Input					
Differential input voltage range [1]	Full temperature	0.98		1.5	Vp-p
Input common mode voltage	Full temperature		1.0		V
Differential input impedance	Full temperature		2		kΩ
Input capacitor	25℃		6		pF
Power consumption characteristics					
Analog power supply voltage (AVDD)	Full temperature	1.7	1.8	1.9	V
Digital power supply voltage (DRVDD)	Full temperature	1.7	1.8	1.9	V
Analog power supply current (I_{AVDD}) [2]	Full temperature		312		mA
Digital power supply current (I_{DRVDD}) [2] Dual Data Rate (DDR) Mode [3]	Full temperature		60		mA
Chip power consumption/Dual data rate (DDR) mode	Full temperature		671.4		mW

1. The differential input voltage range can be configured via SPI, with a default value of 1.25Vp-p.
2. Analog and digital power supply currents were tested at -1dBFS and a 10.3MHz input signal.
3. Dual data rate mode is a user-selectable mode that can be configured via SPI.

8. Electrical Dynamic Characteristics

AVDD=1.8V, DRVDD=1.8V, T_{MIN} = -40℃, T_{MAX} =- +85℃, A_{IN} = -10.0dBFS, 200MSPS, input signal range=2.0Vpp, DCS off, unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Unit
Signal-to-noise ratio (SNR)					
f_{IN} = 16MHz	25℃		71		dBFS
	Full temperature				dBFS
f_{IN} = 80MHz	25℃		70.5		dBFS
	Full temperature				dBFS
f_{IN} = 141MHz	25℃		70		dBFS
f_{IN} = 160MHz	25℃		69		dBFS
f_{IN} = 220MHz	25℃		69		dBFS
Signal-to-noise ratio (SINAD)					
f_{IN} = 16MHz	25℃		70		dBFS
	Full temperature				dBFS
f_{IN} = 80MHz	25℃		70		dBFS
	Full temperature				dBFS
f_{IN} = 141MHz	25℃		69		dBFS
f_{IN} = 160MHz	25℃		68		dBFS
f_{IN} = 220MHz	25℃		68		dBFS
Significant digits (ENOB)					
f_{IN} = 16MHz	25℃		11.3		Bits
	Full temperature				Bits
f_{IN} = 80MHz	25℃		11.3		Bits
	Full temperature				Bits
f_{IN} = 141MHz	25℃		11.2		Bits
f_{IN} = 160MHz	25℃		11.0		Bits
f_{IN} = 220MHz	25℃		11.0		Bits
Worst harmonic (second or third order)					
f_{IN} = 16MHz	25℃		-80		dBc
	Full temperature				dBc
f_{IN} = 80MHz	25℃		-75		dBc
	Full temperature				dBc
f_{IN} = 141MHz	25℃		-75		dBc
f_{IN} = 160MHz	25℃		-75		dBc
f_{IN} = 220MHz	25℃		-75		dBc
Worst of all (noise other than HD2 and HD3)					
f_{IN} = 16MHz	25℃		-77		dBc
	Full temperature				dBc
f_{IN} = 80MHz	25℃		-75		dBc
	Full temperature				dBc
f_{IN} = 141MHz	25℃		-75		dBc
f_{IN} = 160MHz	25℃		-76		dBc
f_{IN} = 220MHz	25℃		-76		dBc
Front-end analog input bandwidth			200		MHz

9. Digital Characteristics

AVDD=1.8V, DRVDD=1.8V, T_{MIN}=-40℃, T_{MAX}=+85℃, A_{IN}= -10.0dBFS, 200MSPS, input signal range=2.0Vpp, DCS off, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit
Clock input					
Logical compatibility	Full temperature	CMOS/LVDS/LVPECL			
Internal common-mode bias	Full temperature		1.2		V
Differential input voltage	Full temperature		0.2		Vp-p
Input voltage range	Full temperature	AVSS		AVDD	V
		0.3		1.6	
Input common mode range	Full temperature	1		AVDD	V
High-level input voltage (V_{IH})	Full temperature	1.2		AVDD	V
Low-level input voltage (V_{IL})	Full temperature	0		0.8	V
High-level input current (I_H)	Full temperature	-10		+10	μA
Low-level input current (I_L)	Full temperature	-10		+10	μA
Differential input impedance	Full temperature		1 8		kΩ
Input capacitor	Full temperature		4		pF
Logical input					
Logic 1 voltage	Full temperature	0.8xVDD			V
Logic 0 voltage	Full temperature			0.2xAVDD	V
Logic 1 Input Current (SDIO)	Full temperature		0		μA
Logic 0 Input Current (SDIO)	Full temperature		- 60		μA
Logic 1 input current (SCLK,PDWN,CSB,RESET)	Full temperature		55		μA
Logic 0 input current (SCLK, PDWN, CSB, RESET)	Full temperature		0		μA
Input capacitor	25℃		4		pF
Logical output					
V_{OD} differential output voltage	Full temperature	247		454	mV
V_{OS} output DC offset voltage	Full temperature	1.125		1.375	V
Output encoding method	Two's complement, Gray code, offset binary code (default)				

10. Switching Characteristics

AVDD=1.8V, DRVDD=1.8V, T_{MIN}=-40℃, T_{MAX}=+85℃, A_{IN} = -10.0dBFS, 200MSPS, input signal range=2.0Vpp, DCS off, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit
Maximum conversion rate	Full temperature	2 00			MSPS
Minimum conversion rate	Full temperature			100	MSPS
CLK+ High Pulse Width (t_{CH})	Full temperature	2.15	2.4		ns
CLK+ Low pulse width (t_{CL})	Full temperature	2.15	2.4		ns
Output (LVDS – SDR mode)					
Data transmission delay (t_{PD})	Full temperature		4.1		ns
Rise time (t_R) (20% ~ 80%)	25℃		0.2		ns
Fall time (t_F) (20% ~ 80%)	25℃		0.2		ns
DCO transmission delay (t_{CPD})	Full temperature		4.1		ns
Offset of data to DCO (t_{SKEW})	Full temperature	-0.3	0.1	0.5	ns
Waiting time	Full temperature				Cycles
Output (LVDS – DDR mode)					
Data transmission delay (t_{PD})	Full temperature		4.1		ns
Rise time (tR) (20% ~ 80%)	25℃		0.2		ns
Fall time (tF) (20% ~ 80%)	25℃		0.2		ns
DCO transmission delay (t_{CPD})	Full temperature		4.1		ns
Offset of data to DCO (t_{SKEW})	Full temperature	-0.3	0.1	0.5	ns
Waiting time	Full temperature				Cycles
Clock jitter (tJ)	25℃		0.3		ps rms

11. Timing Diagram

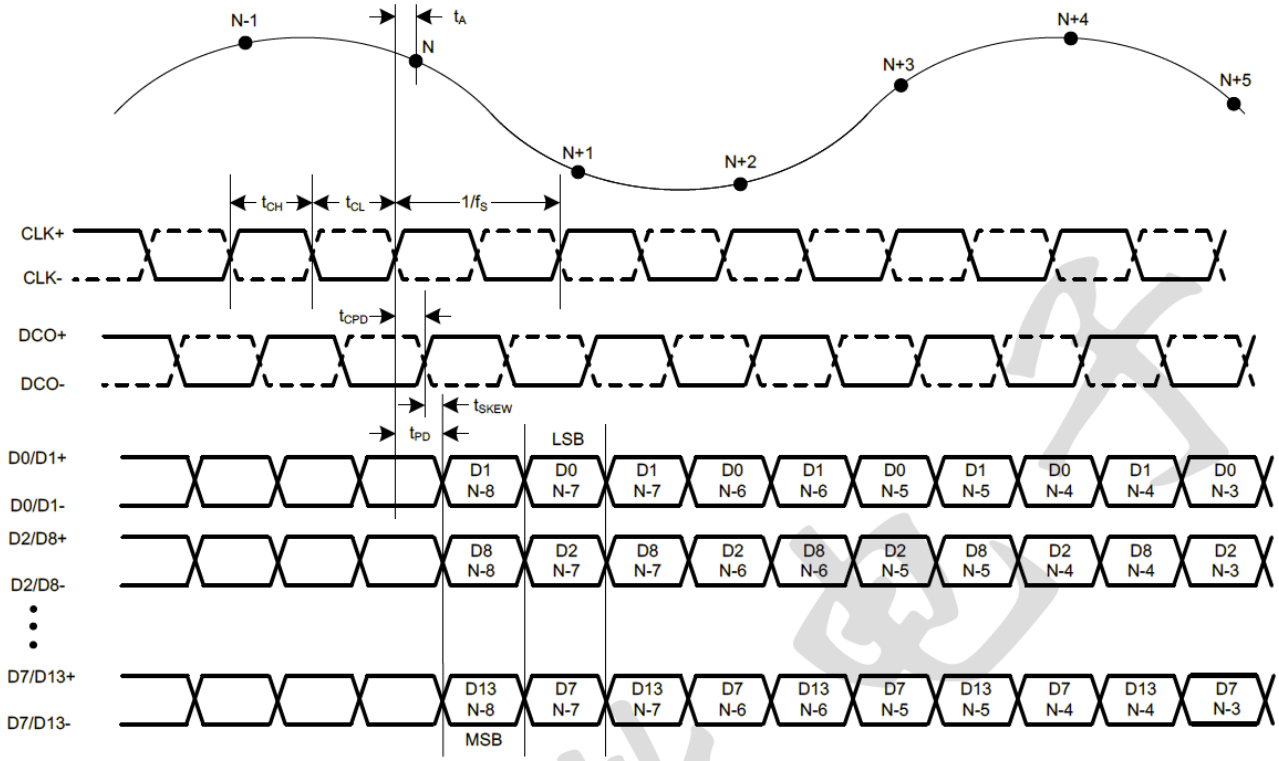


Figure 3. Dual Data Rate Mode (DDR Mode)

12. Absolute Maximum Ratings

Parameter		Rating
Electrical parameters		
AVDD	AGND	-0.3V to 2.0V
DRVDD	DRGND	-0.3V to 2.0V
AGND	DRGND	-0.3V to 0.3V
AVDD	DRGND	-2.0V to 2.0V
Digital output (DCO, OR, Dx+/Dx-)	DRGND	-0.3V to DRVDD + 0.3V
CLK+,CLK	AGND	-0.3V to 3.9V
VIN+, VIN-	AGND	-0.3V to AVDD + 0.2V
SDIO/DCS	DRGND	-0.3V to DRVDD + 0.3V
PDWN	AGND	-0.3V to 3.9V
CSB	AGND	-0.3V to 3.9V
SCLK/DFS	AGND	-0.3V to 3.9V
Environmental parameters		
Storage temperature range		-65℃ to +125℃
Operating temperature range		-40℃ to +85℃
Pin temperature (soldering, 10 seconds)		300℃
Maximum junction temperature		150℃

Note: Exceeding the above absolute maximum ratings may result in permanent damage to the device. These are only the rated limits and do not guarantee that the device will function properly under these conditions or under any other conditions exceeding the specifications shown in the Operation section of this Technical Specification. Prolonged operation at absolute maximum ratings will affect the reliability of the device.

- **Thermal resistance**

The exposed bottom pads of a QFN package must be soldered to the PCB ground plane. Soldering the exposed bottom pads to the customer's circuit board helps increase pad connection reliability and maximizes the package's thermal conductivity.

Encapsulation type	θ_{JA}	θ_{JC}	unit
QFN-56 (8x8x0.75mm)	27.9	6.6	℃/W

Note: The θ_{JA} and θ_{JC} values shown in the table above are typical values for a 4-layer PCB in a still air environment. Airflow improves heat dissipation and significantly reduces the θ_{JA} value. Furthermore, direct contact between metal and package pads, such as through metal traces or vias connecting to ground or power planes, reduces the θ_{JA} value .

- **ESD Warning**

ESD (Electrostatic Discharge) sensitive devices and circuit boards may discharge imperceptibly. Although this product has patented or proprietary protection circuitry, devices may be damaged upon exposure to high-energy ESD. Therefore, appropriate ESD precautions should be taken to avoid performance degradation or malfunction.

ESD-HBM	+/-5000V
ESD-CDM	+/-1000V

13. Functional Description

- **Serial interface description**

The three-wire serial interface at the input is timing compatible with the AD9230, and its clock frequency can reach up to 40MHz. The detailed interface timing is shown in Figure 4.

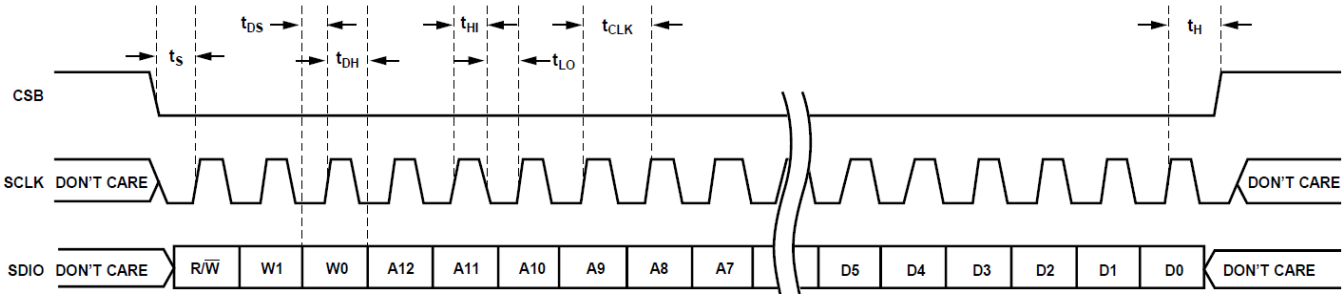


Figure 4. Serial interface timing

- **Output data encoding**

Analog Input (V)	Condition(V)	Binary Offset Code (D13 ~ D0)	Two's Complement	Gray Code	Overflow Flag (OR)
VIN+ - VIN-	<-FS	00 0000 0000 0000	10 0000 0000 0000	10 0000 0000 0000	1
VIN+ - VIN-	-FS	00 0000 0000 0000	10 0000 0000 0000	10 0000 0000 0000	0
VIN+ - VIN-	0	10 0000 0000 0000	00 0000 0000 0000	00 0000 0000 0000	0
VIN+ - VIN-	FS	11 1111 1111 1111	01 1111 1111 1111	01 0000 0000 0000	0
VIN+ - VIN-	FS+0.5LSB	11 1111 1111 1111	01 1111 1111 1111	01 0000 0000 0000	1

14. Register

- **Register configuration**

Note: The following register configurations differ from the default values. The following registers need to be configured during chip initialization.

ADDR	Value	Note
0x0F	0x02	CML Enable
0x18	0x0F	Input Span = 1.5Vpp
0x14	0x28	Output = 14b, DDR mode
0xFF	0x01	The register data is transferred from the master shift register to the slave register. After the transfer is complete, the transfer register is automatically cleared.

- **Register table**

Address: 0x00, Default: 0x18

Bit	Symbol	Default	Functional Description
7:6		0x00	
5		0	Software reset When this bit is set to "1", all programmable bits, except for the COMM register bit which is unaffected by the software reset, will return to their power-on state. The software reset will remain active until this bit is cleared to 0 (inactive). 0: Not activated 1: Software reset activation
4:0		0x18	

Table 1. Chip Port Configuration (chip_port_config) Register

Address: 0x01, Default: 0x0C

Bit	Symbol	Default	Functional Description
7:0	Chip_id	0x0C	Unique ID (Read Only)

Table 2. Chip ID (Chip_ID) Register

Address: 0x02, Default: 0x00

Bit	Symbol	Default	Functional Description
7:5		0x00	
4:3	speed_grade	0 0	00=250MSPS ; 01=210MSPS ; 10=170MSPS
2:0		0x00	

Table 3. Chip-level (chip_grade) registers

Address: 0xFF, Default: 0x00

Bit	Symbol	Default	Functional Description
7:1		0x00	
0	reg_transfer	0	0: unused 1: Transfer register data from the master shift register to the slave register. Once the transfer is complete, the transfer register is automatically cleared.

Table 4. Device Update Registration (Contoso update)

Address: 0x08, Default: 0x00

Bit	Symbol	Default	Functional Description
7:3		0x00	
2:0	int_pwdn_mode	0x00	000 : Normal power on ; 001 : Power off ; 010 : Standby ; 011 : Reserved

Table 5. Modes Register

Address: 0x09, Default: 0x01

Bit	Symbol	Default	Functional Description
7:1		0x00	
0	dcs_ctrl	1	Duty cycle stabilizer (DCS bypassb): 0 : Enabled (default) ; 1 : Disabled

Table 6. Clock Register

Address: 0x0D, Default: 0x00

Bit	Symbol	Default	Functional Description
7:6		0x00	
5	rst_pn23	0	1: on 0: off
4	rst_pn9	0	1: on 0: off
3:0	output_test_mode	0x00	0001: midscale short 0010: Output all 1s, overflow=0 0011: Output all zeros, overflow=0 0100: Checker board output 0101: overflow=0, dout is PN23 0110: overflow=0, dout is PN9 0111: Output all 1s/all 0s inverted signal 1000~1110: unused 1111: Ramp Output

Table 7. Test I/O (test_io) Register

Address: 0x0F, Default: 0x00

Bit	Symbol	Default	Functional Description
7:2		0x00	
1	cml_en	0	1: cml enable ; 0: cml disable (default)
0		0	

Table 8. Analog Input Configuration (AIN_config) Register

Address: 0x14, Default: 0x00

Bit	Symbol	Default	Functional Description
7:5	reserved	0x00	
4	output_en	0	Output: 0: Output is enabled (default) ; 1: Output is disabled.
3	ddr_enable	0	DDR control: 1: Enable DDR output mode ; 0: Disable DDR output mode (default)
2	output_invert	0	Output inversion control: 0: Off, outputs normal data (default) ; 1: On, outputs reversed data.
1:0	data_format	0 0	Output format selection: 00: Output offset in binary (default) 01: 2's complement 10: Graymall 11: Undefined

Table 9. Output Mode Control (output_mode) Register

Address: 0x15, Default: 0x00

Bit	Symbol	Default	Functional Description
7:3		0x00	
2:0	lvdsfine_adj	000	LVDS fine current regulation: 000 : Default 3.5mA ; 001 : 3.5mA ; 010: 3.25mA ; 011: 3mA ; 100: 2.75mA ; 101:2.5mA ; 110:2.25mA ; 111:2mA

Table 10. Output Adjustment Register

Address: 0x16, Default: 0x03

Bit	Symbol	Default	Functional Description
7	output_clk_polarity	0	
6:0		0x00	Output clock polarity control 1: Inverting clock output ; 0: Non-inverting clock output (default)

Table 11. Output Phase Register

Address: 0x17, Default: 0x00

Bit	Symbol	Default	Functional Description
7	output_delay_en	0	output default values: 0: Enabled (default) ; 1: Disabled.
6:5		0x00	
4:0		0x00	Output clock delay : 00000: 0.1ns 00001: 0.2ns ... 11110: 3.1ns 11111: 3.2ns

Table 12. Output Delay Control (FLEX_output_delay) Register

Address: 0x18, Default: 0x00

Bit	Symbol	Default	Functional Description
7:6		0x00	
5:0	ref_range	011000	Reference range adjustment: 10000: 1.3V 10001: 1.33V … … 11111: 1.64V 00000: 1.67V 00001: 1.69V … … 01110: 1.97V 01111: 1.50V

Table 13. Reference Range Control (REF_range_CTRL) Register

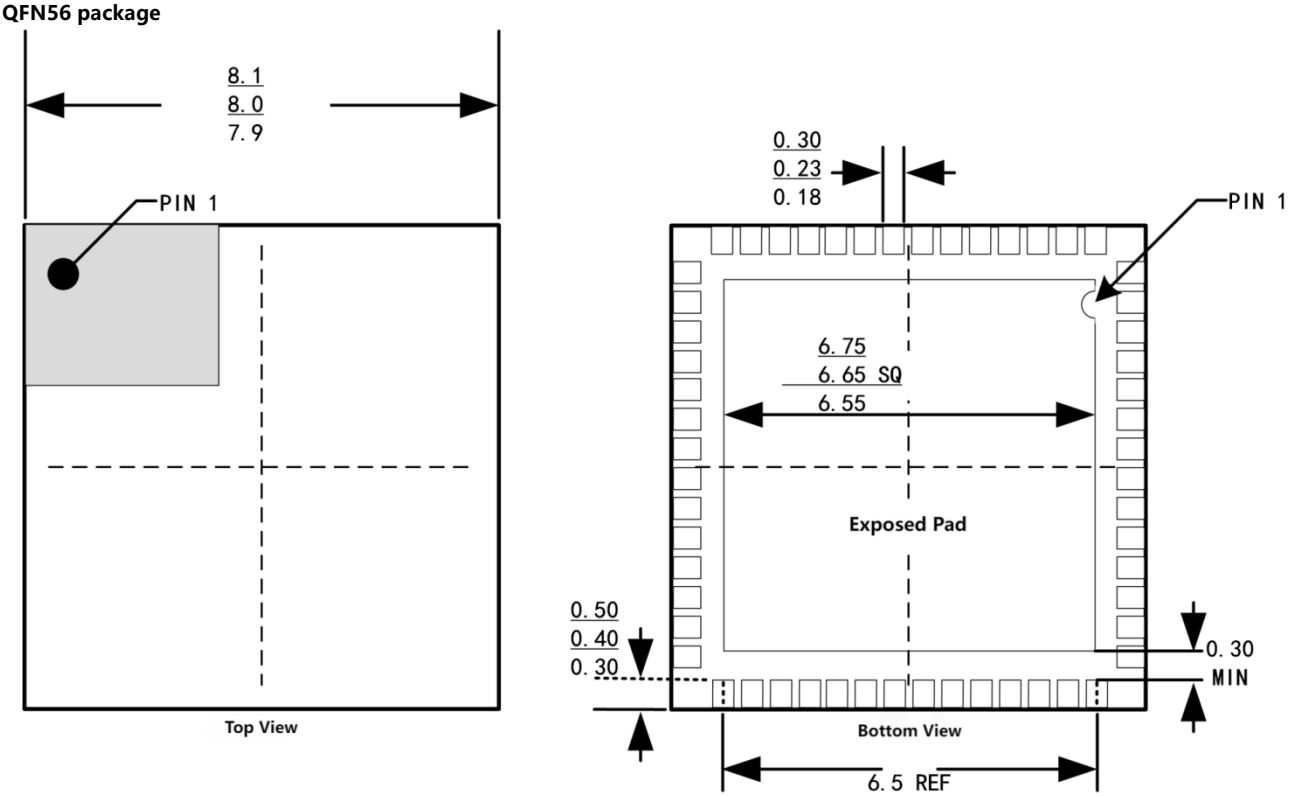
Address: 0x2A, Default: 0x01

Bit	Symbol	Default	Functional Description
7:2		0x00	
1	ovr_position	0	Overflow location (DDR mode only): 0 = pin 9, pin 10 1 = Pin 21, Pin 22
0	overrange_enable	1	overrange bit control1: 1: By default, out-of-range bits are enabled. 0: Disable out-of-range bit output

Table 14. Overrange Control (OVERRANGE_CTRL) Register

14. Packaging Dimensions and Structure

QFN56 package



15. Device Ordering Information

Model	Temperature Range	Packaging Type	Package
ADCP9230-200	-40 ℃ ~85 ℃	QFN56	260/reel