AD9467-250 16-Bit, Single-Channel, 250 MSPS ADC

1. Features

- Resolution: 16-bit
- Power supply voltage: 3.3V/1.8V
- Maximum sampling rate 250 MSPS
- SNR: 72dBFS (170 MHz @ 250 MSPS)
- SFDR: 89dBc(170 MHz @ 250 MSPS)
- 60 fs rms jitter
- Differential nonlinearity DNL = ±0.5 LSB (typical)
- Integral nonlinearity INL = ±3.5 LSB (typical)
- Differential analog input range ≤ 2.5VPP
- SPI Function
- DDR LVDS output (ANSI-644 compatible)
- The built-in clock has a stable duty cycle and provides clock output
- QFN72 package

2. Applications

- Communication
- Receiver
- Base station
- Spectral analysis
- Broadband Wireless
- Radar
- Infrared imaging
- Power amplifier linearization
- Image processing

3. Overview

The AD9467-250 is a 16-bit monolithic intermediate frequency sampling analog-to-digital converter (ADC). It is optimized for wideband performance and ease of use. Operating at a conversion rate of 250 MSPS, it is designed for wireless receivers, instruments, and test equipment requiring high dynamic range. The ADC requires 1.8V and 3.3V power supplies and a low-voltage differential input clock for full-performance operation. Many applications do not require external references or driver components. The data output is LVDS-compliant (ANSI-644 compliant) and includes methods to reduce the total current required for short tracking distances. A Data Clock Output (DCO) is provided for capturing data on the output and for signaling new output bits. Internal power-down functionality, supported via SPI, typically consumes less than 5 mW when disabled. Optional features allow users to implement a variety of selectable operating conditions, including input range, data format selection, and output data test modes. The AD9467-250 operates over an industrial temperature range of 40°C to +85°C.

4. Device Packaging Information

Product Model	Packaging Type	Package Size
AD9467-250	QFN72	10mm × 10mm

5. Functional Block Diagram

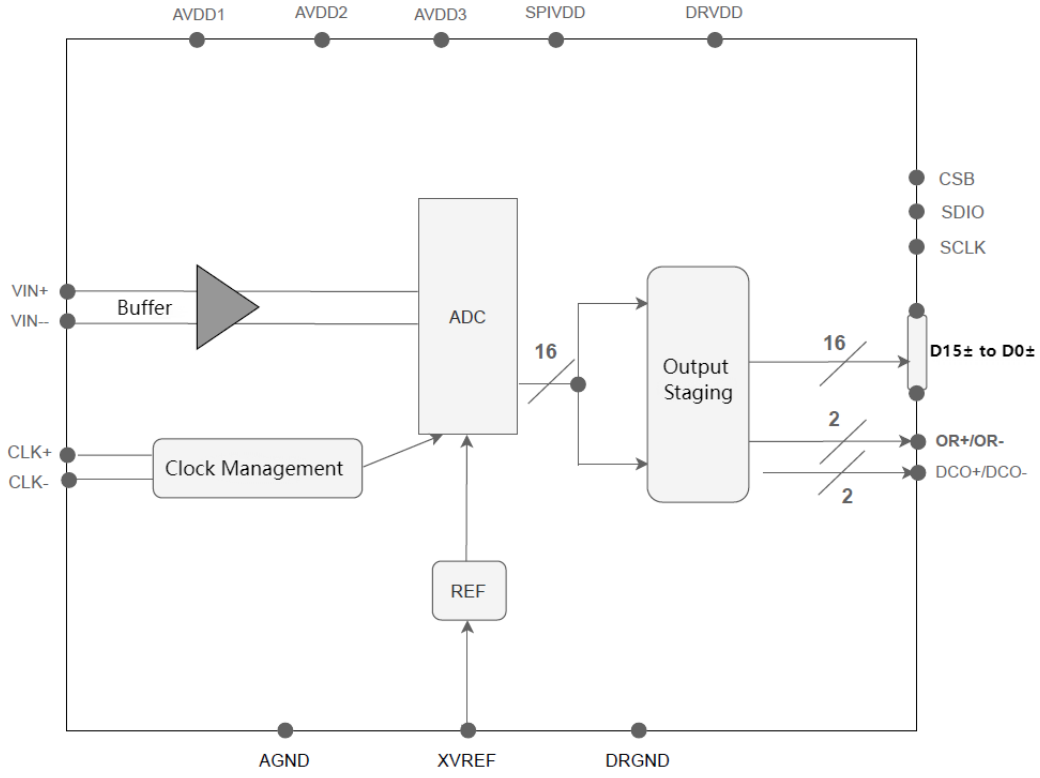


Figure 1. Functional Block Diagram

www.dsown.com
Email：info@dsown.com

Basic Timing Parameter Table

Electrical parameters	Symbol	Condition	Min	Typ	Max	Unit
Conversion rate	f_s		50		250	MSPS
High-level width of the clock	t_{CH}	Design Guarantee		2.0		ns
High-level width of the clock	t_{CL}	Design Guarantee		2.0		ns
Aperture Delay	t_A	Design Guarantee		1.2		ns
Transmission delay	t_{PD}	Design Guarantee		3		ns
DCO transmission delay	t_{CPD}	Design Guarantee		3		ns
DCO and Data Offset	t_{SKEW}	Design Guarantee	-200		+200	ps
Pipeline delay	---	Design Guarantee		1 6		Cycles

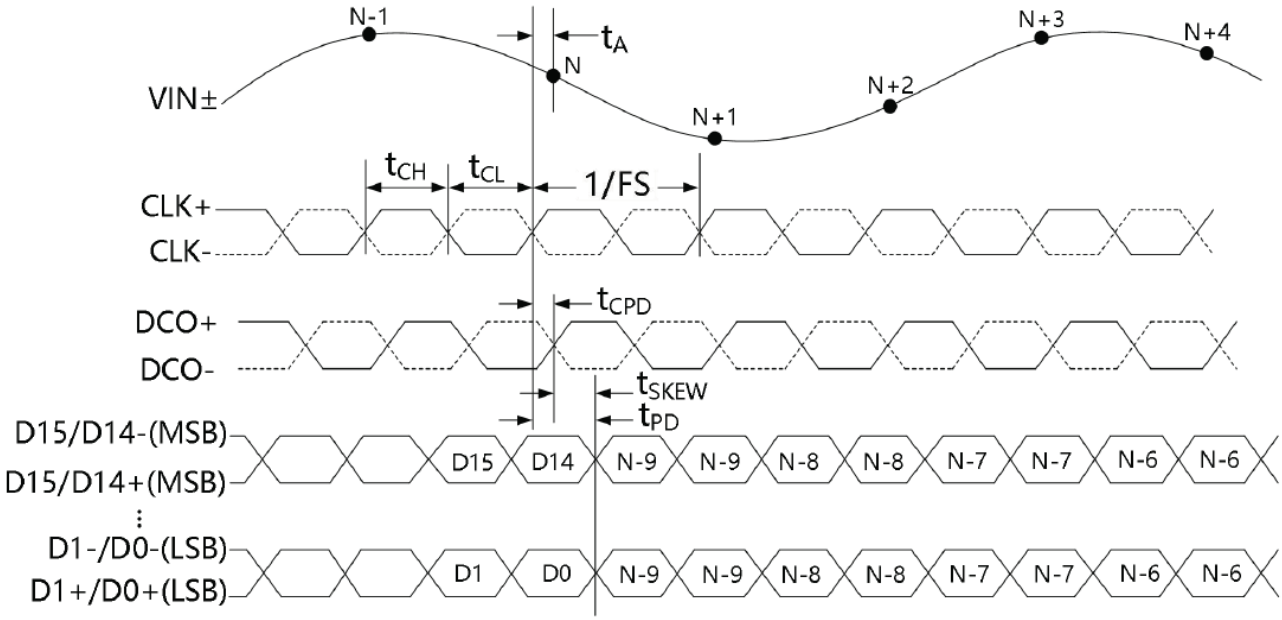


Figure 2. Work sequence diagram

6. Pin Configuration and Functions

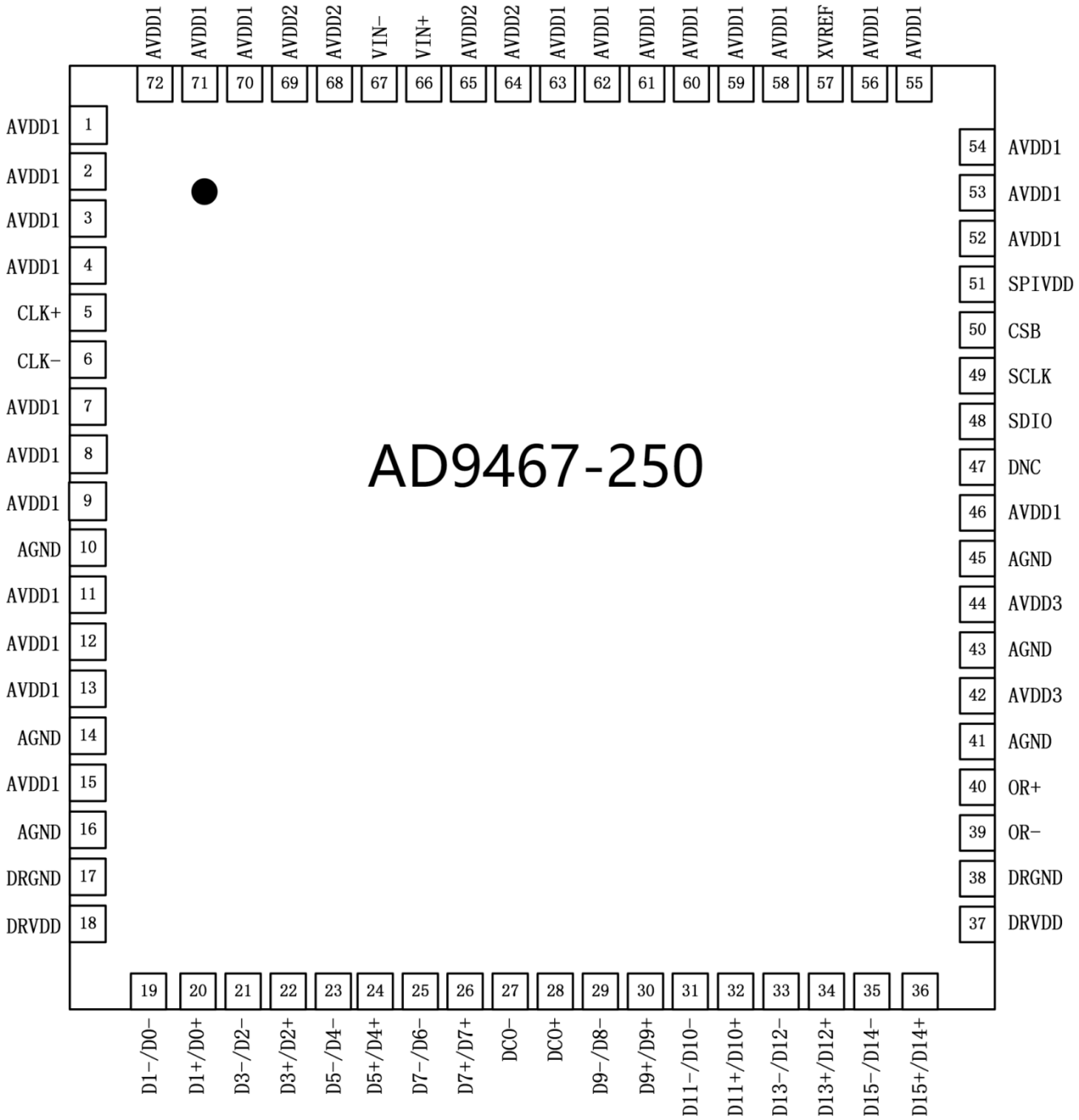


Figure 3. QFN72 pin diagram

Pin Functions

Pin number	Symbol	Function
10 , 14 , 16, 41, 43, 45	AGND	Analog
1, 2, 3, 4, 7, 8, 9, 11, 12, 13, 15, 46, 52, 53, 54, 55, 56, 58, 59, 60, 61, 62, 63, 70, 71, 72	AVDD1	1.8V analog power supply
64, 65, 68, 69	AVDD2	3.3V analog power supply
42, 44	AVDD3	1.8V analog power supply
51	SPIVDD	1.8V or 3.3V SPI power supply
17, 38	DRGND	Digital output driven ground
18, 37	DRVDD	1.8V digital output driver power supply
67	VIN-	Analog input negative terminal
66	VIN+	Analog input positive terminal
6	CLK-	Clock input negative terminal
5	CLK+	Clock input positive terminal
19	D1-/D0-	Negative terminals of D1 and D0 digital outputs
20	D1+/D0+	D1 and D0 are the positive terminals of the digital outputs
21	D3-/D2-	Negative terminals of D3 and D2 digital outputs
22	D3+/D2+	D3 and D2 digital output positive terminals
23	D5-/D4-	Negative terminals of D5 and D4 digital outputs
24	D5+/D4+	D5 and D4 are the positive terminals of the digital outputs
25	D7-/D6-	Negative terminals of D7 and D6 digital outputs
26	D7+/D6+	D7 and D6 are the positive terminals of the digital outputs
29	D9-/D8-	Negative terminals of D9 and D8 digital outputs
30	D9+/D8+	D9 and D8 digital output positive terminals
31	D11-/D10-	Negative terminals of D11 and D10 digital outputs
32	D11+/D10+	D11 and D10 digital output positive terminals
33	D13-/D12-	D13 and D12 digital outputs output negative terminal
34	D13+/D12+	Positive terminals of D13 and D12 digital outputs
35	D15-/D14-	D15 (MSB) and D14 digital output negative terminals
36	D15+/D14+	D15 (MSB) and D14 digital output positive terminals
27	DCO-	Data clock digital output negative terminal
28	DCO+	Data clock digital output positive terminal
39	OR-	Out-of-range digital output negative terminal
40	OR+	Out-of-range digital output positive terminal
47	DNC	Not connected (pin left floating)
48	SDIO	Serial data input/output
49	SCLK	Serial clock
50	CSB	Chip selection bar
57	XVREF	External VREF options

7. Absolute Maximum Ratings

Parameter	Value
AVDD to AGND	-0.3V to +2.0V
DRVDD to DRGND	-0.3V to +2.0V
AGND to DRGND	-0.3V to +0.3V
AVDD to DRVDD	-2.0V to +2.0V
D0+/D0− Through D11+/D11− to DRGND	-0.3V to DRVDD +0.2V
DCO+, DCO− to DRGND	-0.3V to DRVDD +0.2V
OR+, OR− to DRGND	-0.3V to DRVDD +0.2V
CLK+ to AGND	-0.3V to AVDD +0.2V
CLK - to AGND	-0.3V to AVDD +0.4V
VIN+ to AGND	-0.3V to AVDD +0.4V
VIN- to AGND	-0.3V to AVDD +0.2V
CML to AGND	-0.3V to AVDD +0.2V
VREF to AGND	-0.3V to AVDD +0.2V
SDIO to DRGND	-0.3V to DRVDD +0.2V
PDWN to AGND	-0.3V to DRVDD +0.2V
CSB to AGND	-0.3V to DRVDD +0.2V
SCLK/DFS to AGND	-0.3V to DRVDD +0.2V
Operating temperature	-40℃ to +85℃
Pin temperature (soldering, 10s)	300℃
Junction temperature	150℃
Storage temperature range	-65℃ to +125℃

8. Electrical Parameters

Unless otherwise specified, the maximum peak-to-peak value of the analog input is 2.5V, V_{DDA1} = 1.8V, V_{DDA3} = 1.8V, V_{DDD} = 1.8V, V_{DDA2} = 3.3V, GND $_A$ = GND $_D$ = 0, and -40℃ ≤ T_A ≤ 85℃.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution				16		Bits
Integral linearity error	E_L	f_{IN} = 10MHz	-16	±3.5	16	LSB
Differential linearity error	E_{DL}	f_{IN} = 10MHz	-1	±0.5	1.5	LSB
Offset voltage error	E_O		-250	-5	250	LSB
Gain error	E_G		-8	-1.8	8	%FSR
Full power bandwidth	FPBW			900		MHz
Phase noise jitter	AUJ			60		fs rms
Power consumption	P_W			1.295	1.8	W
Signal-to-noise ratio	SNR	f_{IN} = 70MHz @ A_{IN} = −1dB	70	74.42		dBFS
		f_{IN} = 140MHz @ A_{IN} = −1dB	69	72.75		
		f_{IN} = 170MHz @ A_{IN} = −1dB	69	72.03		
Signal-to-noise ratio	SINAD	f_{IN} = 70MHz @ A_{IN} = −1dB	70	74.24		dBFS
		f_{IN} = 140MHz @ A_{IN} = −1dB	69	72.55		
		f_{IN} = 170MHz @ A_{IN} = −1dB	69	71.87		
Significant digits	ENOB	f_{IN} = 70MHz @ A_{IN} = −1dB	11.2	12.04		Bits
		f_{IN} = 140MHz @ A_{IN} = −1dB	11	11.76		
		f_{IN} = 170MHz @ A_{IN} = −1dB	11	11.65		
Stray dynamic range	SFDR	f_{IN} = 70MHz @ A_{IN} = −1dB	77	91.31		dBFS
		f_{IN} = 140MHz @ A_{IN} = −1dB	75	89.04		
		f_{IN} = 170MHz @ A_{IN} = −1dB	75	89.05		
Sampling rate	SR		50		250	MSPS

9. SPI Register

	Name	Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit 1	Bit0 (LSB)	Default	Remark
08	Model							Internal shutdown mode 00 = Working (default) 01 = Full chip shutdown		0X00	Determines the general operating mode of the chip
09	Clock								1=DCS	0X01	
0C	Enhanced mode								1 = Random mode	0X01	Enable random mode
0D	Output test mode			Generate a reset long PN sequence (Default: 1 = On, 0 = Off)	Generate a reset long PN sequence (Default: 1 = On, 0 = Off)		Output test mode 0000=off (default) 0001=midscale short 0010=+FS short 0011=-FS short 0100=checker-boardoutput 0101=PN23 sequence 0110=PN9 sequence 0111=1/0 word toggle			0X00	When a configuration other than the default value is used, test mode data is used instead of normal data output.
0E	BIST						BIST Startup		BIST Enabled	0X00	BIST mode configuration
0F	ADC input	XVREF 0 = off (default) 1=on					Analog shutdown : 0 = off (default) 1 = on			0X00	Analog input function
10	Offset									0X00	Offset adjustment; will combine 01A0 and 01A1 registers.
14	Output mode		0		Output shutdown 1 =on 0 = off (default)	1=DDR Enable	Output data format 00 = Offset binary (default) 01 = two's complement 10 = Gray code			0X00	Offset adjustment; will combine 01A0 and 01A1 registers.

15	Output adjustment					Coarse adjustment: 0 = 3.0 mA ; 1 = 1.71 mA	Output drive current adjustment: 001 = 3.0mA (default) 010 = 2.79mA 011 = 2.57mA 100 = 2.35mA 101 = 2.14mA 110 = 1.93mA 111 = 1.71mA			0X00	Determine LVD or other output attributes.
16	Output phase	DCO output is reversed : 1 = on , 0 = off								0X00	Determine the digital output clock phase
17	Output delay	Enable 1 = on , 0 = off			Delay adjustment					0X00	Adjust the output clock delay
18	Vref					Input full scale range adjustment 0000 = 2.0V $_{pp}$ 0110 = 2.1V $_{pp}$ 0111 = 2.2V $_{pp}$ 1000 = 2.3V $_{pp}$ 1001 = 2.4V $_{pp}$ 1010 = 2.5V $_{pp}$ (default)				0X0A	Adjust Vref
2C	Analog Input						Input coupling mode default: 0=ac, 1=dc			0X00	Determine the input coupling mode
36	Buffer current adjust-ment 1	001000 = +80%						1	0	0X22	
107	Buffer current adjust-ment 2	001000 = +80% (default)								0X20	

10. Signal Input

The analog input front-end of the A/D converter is a differential buffer. To obtain the best dynamic performance, the source impedance of the differential analog terminals should be matched. It is best to connect a small resistor in series at the input to reduce the transient current peak of the driver's output stage. Simultaneously, placing a low-Q inductor or ferrite bead on each input reduces the differential capacitance of the analog input, thereby maximizing the A/D converter bandwidth. At high IF frequencies, the use of low-Q inductors or ferrite beads is essential when driving the converter's front-end. Placing a parallel capacitor or two single-ended capacitors at the input provides a matched passive network, ultimately generating a low-pass filter at the input to filter out out-of-band noise. A recommended input network is shown in the figure.

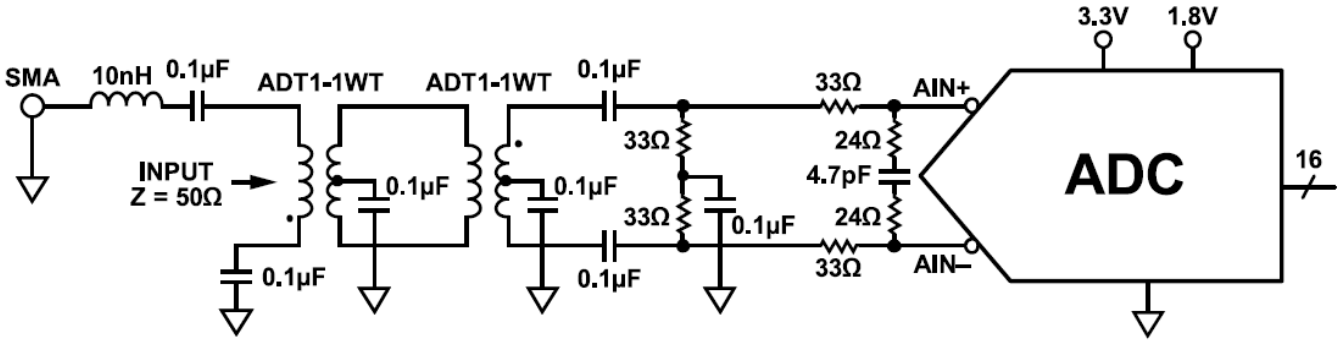


Figure 4. Low -frequency input front-end network (~150MHz)

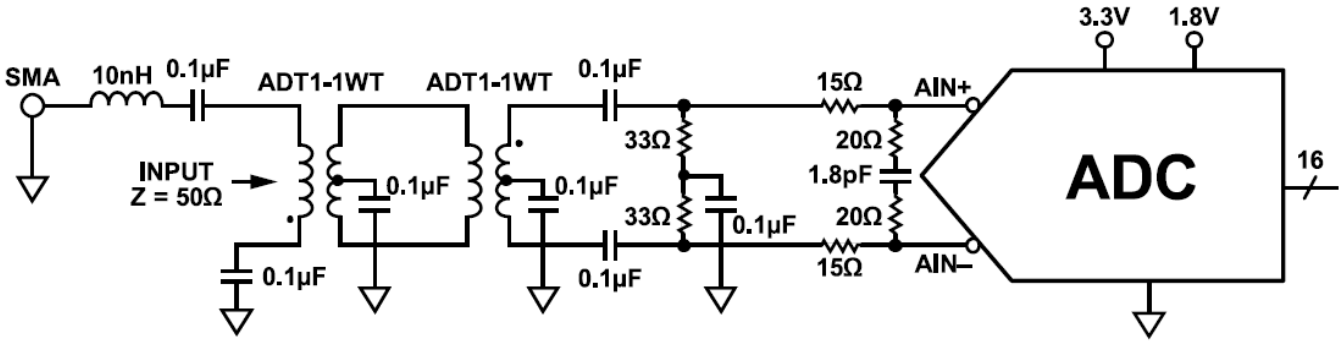


Figure 5. High -frequency input front-end network (intermediate frequency input 150MHz～300MHz)

11. Clock Input Requirements

- **Clock input structure and recommended termination method**

The ADC clock input structure, as shown in the figure, is a differential input structure with an internal 0.8V common-mode voltage. The external clock should be AC-coupled. The recommended input structure using a balun is shown in the figure. The recommended input structure using an LVPECL driver is shown in the figure. If using an LVDS driver, the recommended input structure is shown in the figure.

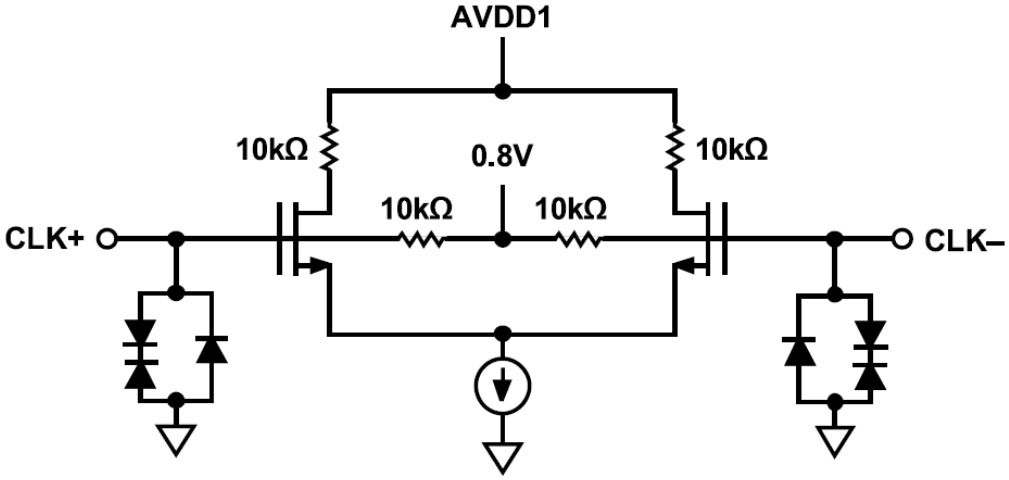


Figure 6. ADC clock input structure

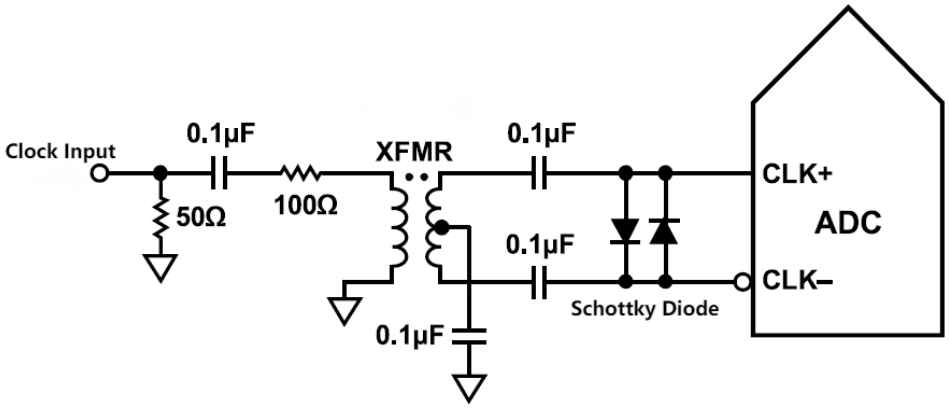


Figure 7. Transformer - coupled differential clock

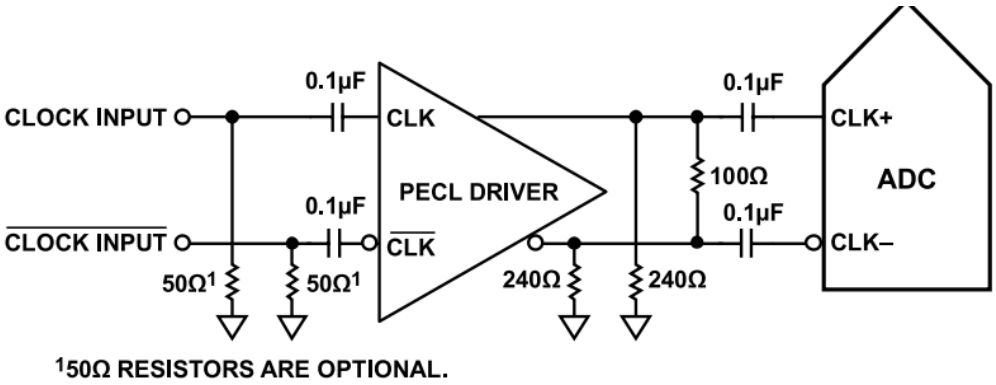


Figure 8. Differential PECL sampling clock

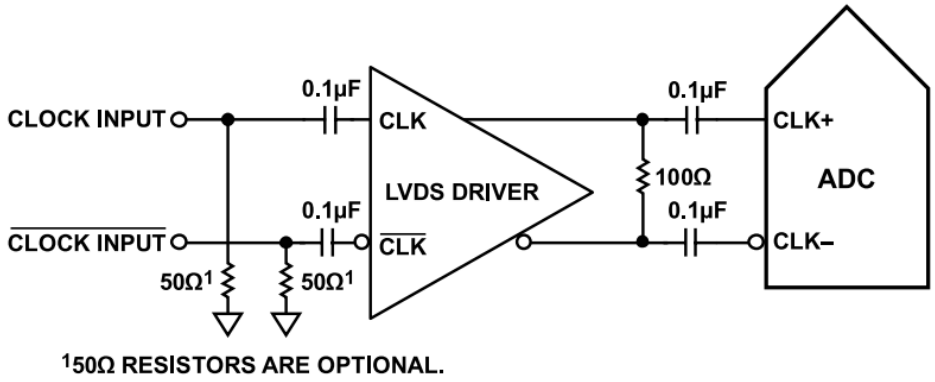


Figure 9. Differential LVDS sampling clock

- **Clock level amplitude**

The minimum amplitude of the differential input clock signal is 250mVpp, compatible with LVDS/LVPECL levels, and the maximum allowable single-ended clock amplitude is VCM±0.9V. To reduce clock jitter and achieve optimal performance, a clock with fast rise and fall times should be provided. Increasing the signal amplitude can achieve this effect with a sine wave input. For high-frequency inputs, it is recommended to maximize the clock input amplitude.

- **Duty cycle**

The internal circuit of the ADC uses the double edges of the input clock to generate various timing signals. To ensure that the chip performs well, the duty cycle of the input clock should be (50±5)% during application.

- **Shaking**

High-speed, high-precision ADCs are highly sensitive to clock jitter, especially when the input signal frequency is high. The signal-to-noise ratio (SNR) is related to jitter as SNR = 20 × lg(1/(2π × f _{IN} × t_{jitter})). To ensure optimal SNR under high-frequency analog input conditions, the system clock jitter must be less than 100 fs.

- **Recommended clock design scheme**

The clock scheme uses a single-ended to differential input, and the recommended transformer is ADT1-1WT. The input and output are AC-coupled using 0.1uF ceramic capacitors. To obtain a symmetrical waveform, two back-to-back Schottky diodes can be connected before the ADC. When routing the PCB, the differential clock traces should be of equal length and symmetrical, and kept away from the analog input ports. Some shielding (copper ground) should be applied between the clock and analog input ports. A recommended clock design scheme is shown in the figure.

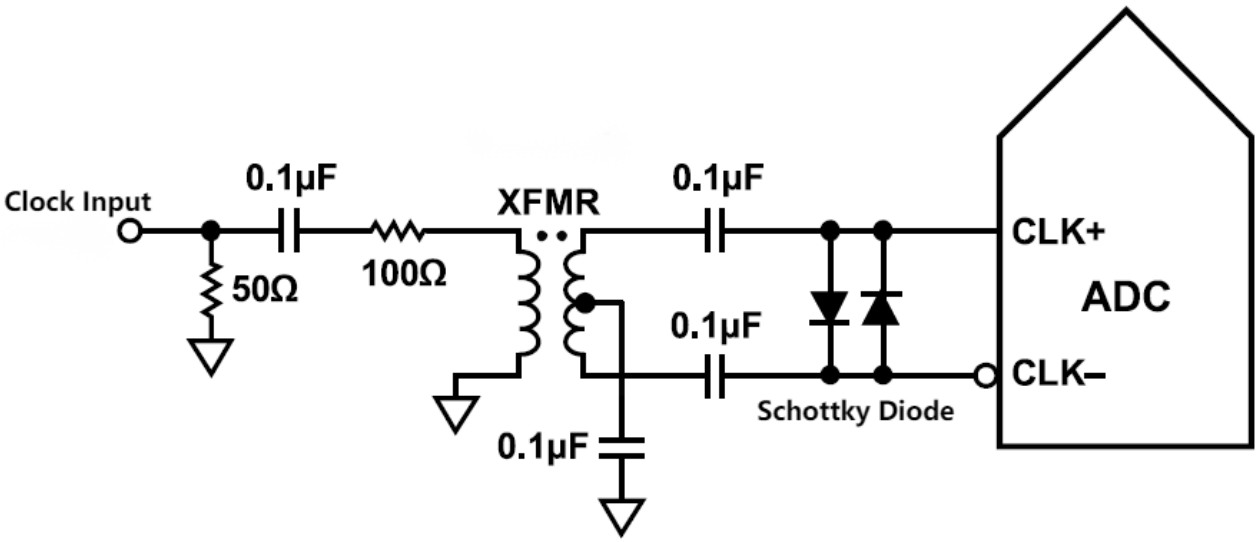


Figure 10. Recommended clock scheme

12. Precautions

- **Product installation precautions:**

1) The application circuit board must have a clean and intact ground plane.

2) The digital ground and analog ground of the circuit board to be applied should be separated as much as possible, and digital lines should not be laid next to analog lines.

3) Electrical installation instructions:

a) This product has a moisture sensitivity rating of MSL3. The permissible time for the product to be exposed to the external environment after being removed from the moisture-proof bag, stored in a dry place or dried, and before reflow soldering is: ≤30℃/60RH%, 168h.

b) If the storage conditions of the device cannot be controlled or traced, please strictly follow the baking process of 125℃ for 24 hours before electrical assembly;

c) If the ambient temperature and humidity of the electrical installation environment cannot be guaranteed to be ≤30℃/60RH%, please complete the soldering within 12 hours after baking;

d) After the product is baked, it is very easy to generate static electricity, and ESD protection should be taken into account during all operations.

e) When using leaded reflow soldering (Sn63Pb37) for board-level assembly, the recommended peak temperature range is 210℃~220℃, and the maximum peak temperature should not exceed 235℃. The dwell time within ±5℃ of the peak temperature should be ≤20s, and the dwell time above the liquidus line should be 60~90s. The heating rate is 2~4℃/s, and the cooling rate is ≤2℃~6℃.

f) When using lead-free reflow soldering (SAC305) for board-level assembly, the recommended peak temperature range is 230℃~245℃, and the maximum peak temperature is not recommended to exceed 260℃. The dwell time within ±5℃ of the peak temperature should be ≤20s, and the dwell time above the liquidus line should be 60~90s. The heating rate is 2~4℃/s, and the cooling rate is ≤2℃~6℃.

g) If the hybrid assembly process requires increased temperature, the device body temperature should be ensured not to exceed 260°C; (the device body temperature measurement point is located on the upper surface of the device during reflow soldering).

h) The solder joints of this product are plated with tin.

- **Product application precautions:**

Each time the product is powered on: First, the device needs to be reset by writing 38h' to the 0x00 register and 01h' to the 0xFF register in sequence; then, the relevant registers (as required by the user) are configured.

- **Product protection precautions:**

1) All leads of the product are designed with electrostatic discharge (ESD) protection. However, high-energy electrical pulses may still damage the circuit. Therefore, ESD protection should be taken into account during testing, handling, and storage.

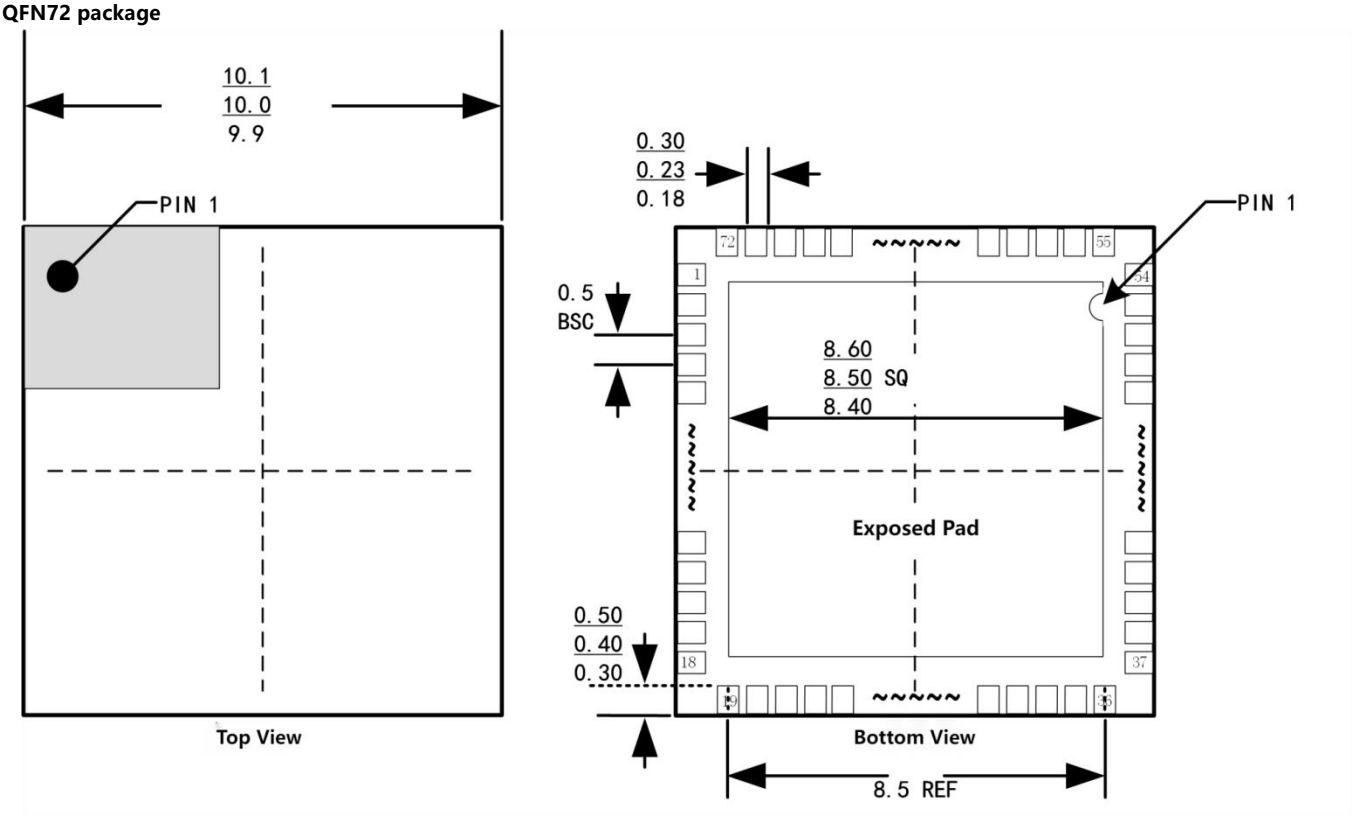
2) Exceeding the absolute maximum rating may cause permanent damage to the device.

13. Common Faults and Troubleshooting Methods

- No signal output: Check if the power supply voltage, input signal, and clock are correctly applied.
- Overflow signal occurs: Check if the common-mode voltage configuration of the positive and negative terminals of the analog input is correct, and if the input signal amplitude is correct.
- Device malfunction: Check the power supply and ensure the power supply voltage is stable.

14. Package size and structure

QFN72 package



15. Device Ordering Information

Model	Temperature Range	Packaging Type	Package Quantity
AD9467-250	-40 ℃ ~ 85 ℃	QFN72	168/reel