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DAC8808/10808/12808 Low Power, High-Performance, Buffered 8-Channel 8-/10-/12-Bit DAC

1. Features

- TSSOP16 , QFN16 Packaging
- I/O voltage: 1.8V to 5.5V
- Core voltage: 1.8V to 3.6V
- Maximum continuous data output rate of 1MHz
- Temperature range: -40 ℃ to 125 ℃
- Four-wire SPI interface
- Pulse generator
- Clock calibration unit
- Precise stop pulse enable window
- Rising edge / falling edge triggered individually or both rising and falling edges triggered simultaneously.

2. Applications

- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuator
- Analog-to-digital converter reference voltage source
- Sensor reference voltage source
- Range detector

3. Overview

The DAC8808/10808/12808 is a full-featured 8-channel, 8/10/12-bit voltage-output digital-to-analog converter (DAC) that operates from a single 2.7V to 5.5V supply, consuming 1.95mW at 3V and 4.85mW at 5V. The DAC8808/10808/12808 is available in a 16-pin WQFN package and a 16-pin TSSOP package. The WQFN package makes the DAC8808/10808/12808 one of the smallest 8-channel DACs in its class. On-chip output amplifiers allow rail-to-rail output swing, and a 3-wire serial interface operates at clock rates up to 40MHz across the entire supply voltage range. The clock frequency of competing devices is limited to 25MHz across a supply voltage range of 2.7-V to 3.6-V. The serial interface is compatible with standard SPI™, QSPI, MICROWIRE, and DSP interfaces. The DAC8808/10808/12808 also offers daisy-chain operation, allowing an unlimited number of DAC8808/10808/12808 units to be updated simultaneously using a single serial interface.

The DAC8808/10808/12808 has two external reference voltage inputs. One reference input serves channels A through D, while the other serves channels E through H. Each reference can be independently set between 0.5V and VA, providing the widest possible output dynamic range. The chip's serial interface controls 16 shift registers on its digital input terminals, facilitating control of the chip's operating modes, including sleep output state and output update state; all channels can be updated individually or uniformly.

4. Equipment Information

Device Model	Packaging	Package Size (nominal value)
DAC8808 DAC10808 DAC12808	TSSOP (16)	5.0 mm × 4.4 mm
	WQFN (16)	3.0 mm × 3.0 mm

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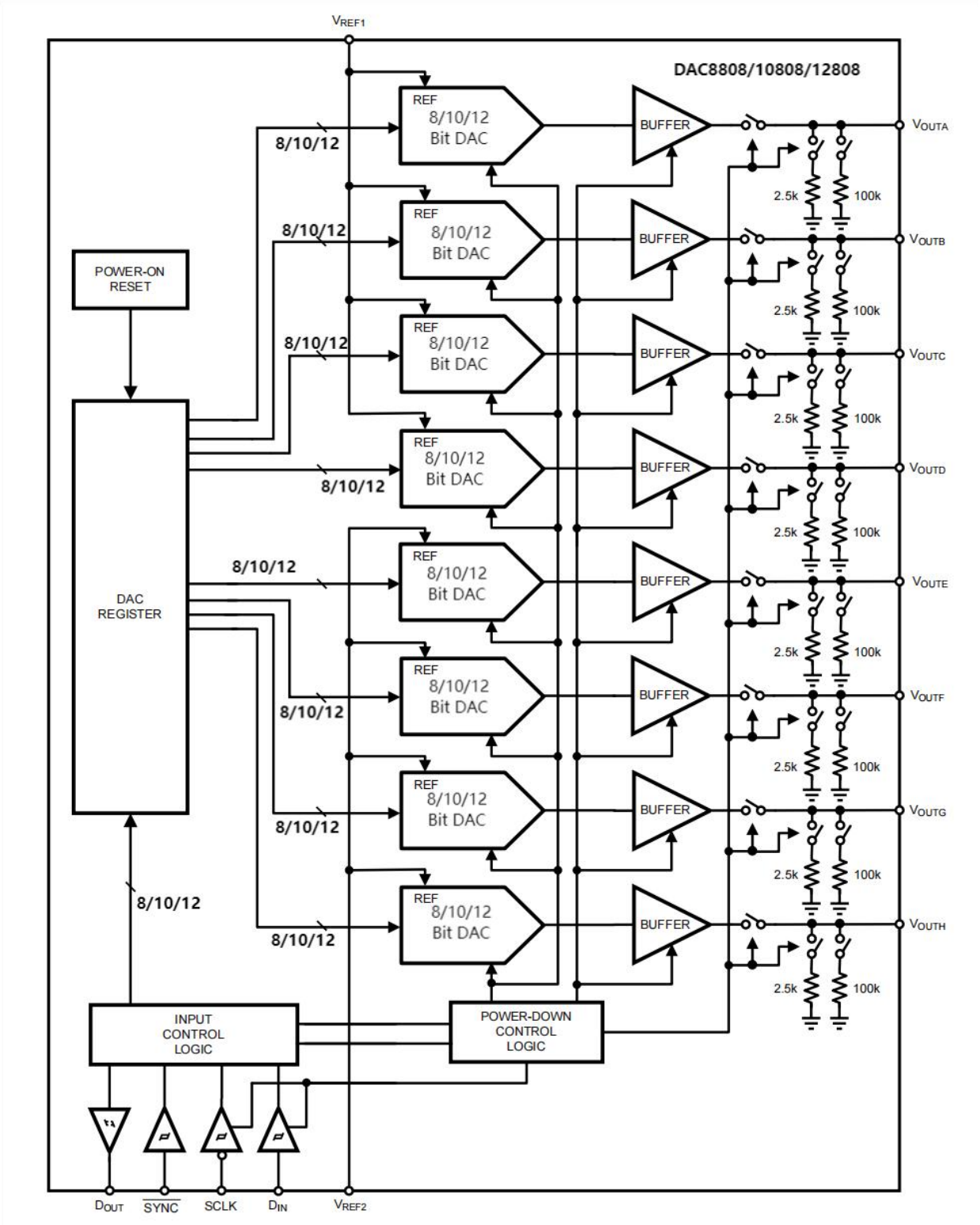
5. Functional Block Diagram



6. Pin Configuration and Functions

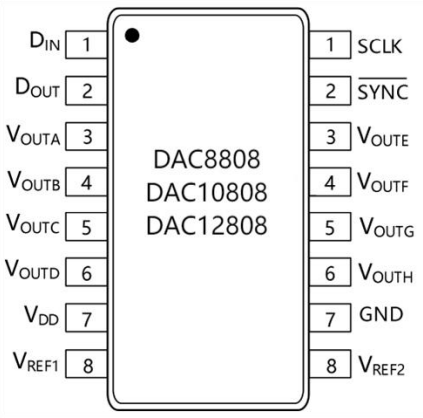


Figure 1. Pin diagram of T SSOP16

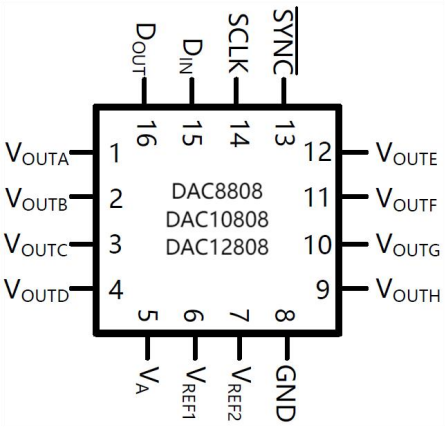


Figure 2. Pin diagram of Q FN16

Pin Functions

Pin			Type	Description
Pin Name	TSSOP No.	WQFN No.		
D_{IN}	1	15	Digital input	Serial data input . Before the frame synchronization signal goes high, 16 falling edges of the clock signal input data to a 16- bit shift register .
D_{OUT}	2	16	Digital output	Serial data output. This digital output is used in daisy-chain mode to connect to the input of another CBM128S085 chip. The digital output becomes invalid when the frame sync signal goes high 16 clock cycles prior.
GND	10	8	Ground	The reference voltage for the ground potential of the entire chip .
SCLK	16	14	Digital input	Serial clock input. Data is clocked into the input shift register on the falling edge of this pin.
$\overline{SYNC}$	15	13	Digital input	Frame synchronization input. When this pin goes low, data is written to the DAC input shift register on the falling edge of SCLK. A rising edge of SYNC after the 16th falling edge of SCLK causes the DAC to update. If SYNC goes high before the 15th falling edge of SCLK, the rising edge of SYNC will act as an interrupt, and the DAC will ignore the write sequence.
V_A	7	5	Power supply	Power input. Must be disconnected from GND.
V_{OUTA}	3	1	Analog output	Channel A simulates the output voltage.
V_{OUTB}	4	2	Analog output	Channel B simulates the output voltage.
V_{OUTC}	5	3	Analog output	Channel C simulates the output voltage.
V_{OUTD}	6	4	Analog output	Channel D simulates the output voltage.
V_{OUTE}	14	12	Analog output	Channel E simulates the output voltage.
V_{OUTF}	13	11	Analog output	Channel F simulates the output voltage.
V_{OUTG}	12	10	Analog output	Channel G simulates the output voltage.
V_{OUTH}	11	9	Analog output	Channel H simulates the output voltage.
V_{REF1}	8	6	Analog Input	The unbuffered reference voltage shared by channels A, B, C, and D must be decoupled from GND.
V_{REF2}	9	7	Analog Input	The unbuffered reference voltage shared by channels E, F, G, and H must be decoupled from GND.
PAD (QFN package only)	—	17	Ground	Exposed die connection pads can be grounded or left floating. Soldering the pads to the PCB provides optimal thermal performance and enhances package self-alignment during reflow.

7. Specifications

7.1 Absolute Maximum Ratings

(TA = 25℃, unless otherwise specified.)

Table 1

Parameter (1)	Symbol	Values	Unit
Power supply voltage relative to ground	V_{Aabs}	-0.3 to +7	V
Digital input voltage relative to ground	V_{Digabs}	-0.3 to +0.3	V
Reference input voltage relative to ground	V_{refabs}	-0.3 to +0.3	V
Channels A to H relative to each other	V_{outabs}	-0.3 to +0.3	V
Temperature range			
Storage temperature range	T_S	-65℃ to +150℃	℃
Junction temperature	T_{Jmax}	150℃	℃
ESD characteristics			
Human model		5000V	V
Machine Model		300V	V
Charging equipment model		1000V	V

1. Operations exceeding the maximum absolute rating can cause irreversible damage to the chip, and prolonged exposure to the maximum absolute rating can affect the chip's reliability.

7.2 Recommended Operating Conditions

(TA = 25℃, unless otherwise specified.)

Table 2

Parameter	Symbol	Range		Unit
		Min	Max	
power supply voltage	V_A	2.7	5.5	V
Operating current (1)	I_A	300	7 00	uA
Ambient temperature	T_A	-40	1 25	℃
Reference voltage	V_{REF1} , V_{REF2}	0.5	V_A	V
Output load	CLoad	0	1,500	pF
SCLK clock frequency	F_{SCLK}	\	4 0	MHz

1. DAC output under no-load condition

7.3 Package Thermal Resistance

Table 3

Heat metering		DAC8808/10808/12808		Unit
		Package (TSSOP16)	Package (QFN16)	
$R_{\theta JA}$	Connection with ambient thermal resistance	98	34	°C/W
$R_{\theta JA}$	Connection with ambient thermal resistance	31	25	
$R_{\theta JA}$	Connection with ambient thermal resistance	43	11	
φ_{JT}	Top characteristic parameters	2	0.2	
φ_{JB}	Connector plate characteristic parameters	43	11	

7.4 Electrical Characteristics

The following specifications apply to V_A = 2.7V to 5.5V, V_{REF1} = V_{REF2} = V_A, C_L = 200pF to GND, f_{SCLK} = 30MHz, and input code range 12 to 1011 , 48 to 4047 (12808 ONLY) . Unless otherwise specified, all limits are T_A = 25°C .

Table 4

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
DAC8808						
Resolution		$T_{MIN} \le TA \le T_{MAX}$	8			Bits
Unity		$T_{MIN} \le TA \le T_{MAX}$	8			Bits
INL	Integral nonlinearity	$T_{MIN} \le TA \le T_{MAX}$		±0.12	±0.5	LSB
DNL	Differential nonlinearity	$T_{MIN} \le TA \le T_{MAX}$		0.03	0.15	LSB
		$T_{MIN} \le TA \le T_{MAX}$	-0.1	-0.02		LSB
DAC10808						
Resolution		$T_{MIN} \le TA \le T_{MAX}$	10			Bits
Unity		$T_{MIN} \le TA \le T_{MAX}$	10			Bits
INL	Integral nonlinearity	$T_{MIN} \le TA \le T_{MAX}$		±0.5	±2	LSB
DNL	Differential nonlinearity	$T_{MIN} \le TA \le T_{MAX}$		0.08	0.35	LSB
		$T_{MIN} \le TA \le T_{MAX}$	-0.04	-0.2		LSB
DAC12808						
Resolution		$T_{MIN} \le TA \le T_{MAX}$	12			Bits
Unity		$T_{MIN} \le TA \le T_{MAX}$	12			Bits
INL	Integral nonlinearity	$T_{MIN} \le TA \le T_{MAX}$		±2	±8	LSB
DNL	Differential nonlinearity	$T_{MIN} \le TA \le T_{MAX}$		0.15	0.75	LSB
		$T_{MIN} \le TA \le T_{MAX}$	-0.4	-0.09		LSB
Static performance						
ZE	Zero code error	I_{OUT} = 0		5	15	mV
FSE	Full scale error	I_{OUT} = 0		-0.1	-0.75	%FSR
GE	Gain error			-0.2	-1	%FSR
ZCED	Zero-code error drift			-20		μV/°C
TC GE	Gain error Tempco			-1		ppm/°C
Output characteristics						
Output voltage range		$T_{MIN} \le TA \le T_{MAX}$	0		VREF1,2	V
I_{OZ}	High impedance output leakage current	$T_{MIN} \le TA \le T_{MAX}$			±1	μA
ZCO	Zero code output	V_A = 3V, I_{OUT} = 200μA		10		mV
		V_A = 3V, I_{OUT} = 1mA		45		mV
		V_A = 5V, I_{OUT} = 200μA		8		mV
		V_A = 5V, I_{OUT} = 1mA		34		mV
FSO	Full-scale output	V_A = 3V, I_{OUT} = 200μA		2.984		V
		V_A = 3V, I_{OUT} = 1mA		2.933		V
		V_A = 5V, I_{OUT} = 200μA		4.987		V
		V_A = 5V, I_{OUT} = 1mA		4.955		V

7.5 Electrical Characteristics (continued)

The following specifications apply to V_A = 2.7V to 5.5V , V_{REF1} = V_{REF2} = V_A , C_L = 200pF to GND , f_{SCLK} = 30 MHz , and input code range 12 to 1011 , 48 to 4047 (12808 ONLY) . Unless otherwise specified, all limits are for T_A = 25°C.

Table 5

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
I_{OS}	Output short-circuit current (Source)	V_A =3V, V_{OUT} = 0 V, Input Code = FFFh			-50		mA
		V_A =5V, V_{OUT} = 0 V, Input Code = FFFh			-60		mA
I_{OS}	Output short-circuit current (Sink)	V_A =3V, V_{OUT} = 3 V, Input Code = 000h			50		mA
		V_A = 5V, V_{OUT} = 5 V, Input Code = 000h			70		mA
I_O	Continuous output current of each channel	T_A = 105°C				10	mA
		T_A = 125°C				6.5	mA
C_L	Maximum load capacitance	R_L = ∞			1500		pF
		R_L = 2 kΩ			1500		pF
Z_{OUT}	DC output impedance				8		Ω
Reference input characteristics							
$V_{REF1,2}$	Minimum input range				0.5		V
		$T_{MIN} \le T_A \le T_{MAX}$		2.7			
	Maximum input range	$T_{MIN} \le T_A \le T_{MAX}$				V_A	
	Input impedance				30		kΩ
Logical input characteristics							
I_{IN}	Input current	$T_{MIN} \le T_A \le T_{MAX}$				±1	μA
V_{IL}	Input low voltage	V_A = 2.7 V to 3.6 V			1	0.6	V
		V_A = 4.5 V to 5.5 V			1.1	0.8	V
V_{IH}	Input high voltage	V_A = 2.7 V to 3.6 V		2.1	1.4		V
		V_A = 4.5 V to 5.5 V		2.4	2		V
C_{IN}	Input capacitor	$T_{MIN} \le T_A \le T_{MAX}$				3	pF
Power consumption characteristics							
V_A	Minimum power supply voltage	$T_{MIN} \le T_A \le T_{MAX}$		2.7		5.5	V
I_N	Normal supply current of power supply pin V_A	f_{SCLK} = 30 MHz, No load on output	V_A = 2.7 V to 3.6 V		460	560	μA
			V_A = 4.5 V to 5.5 V		650	830	μA
	Normal power supply current of V_{REF1} or V_{REF2}	f_{SCLK} = 30 MHz, No load on output	V_A = 2.7 V to 3.6 V		95	130	μA
			V_A = 4.5 V to 5.5 V		160	220	μA
I_{ST}	The quiescent current of the power supply pin V_A	fSCLK = 0, no output load	V_A = 2.7 V to 3.6 V		370		μA
			V_A = 4.5 V to 5.5 V		440		μA
	The quiescent current of V_{REF1} or V_{REF2}	fSCLK =0, no output load	V_A = 2.7 V to 3.6 V		95		μA
			V_A = 4.5 V to 5.5 V		160		μA
I_{PD}	Total power-off current in PD mode	After loading PD mode, f_{SCLK} =30MHz, SYNC=V_A, D_{IN} = 0V	V_A = 2.7 V to 3.6 V		0.2	1.5	μA
			V_A = 4.5 V to 5.5 V		0.5	3	μA
		After loading PD mode, f_{SCLK} = 0 MHz, SYNC = V_A, D_{IN} = 0V	V_A = 2.7 V to 3.6 V		0.1	1	μA
			V_A = 4.5 V to 5.5 V		0.2	2	μA
P_N	Total power consumption (output no-load)	f_{SCLK} = 30 MHz, No load on output	V_A = 2.7 V to 3.6 V		1.95	3	mW
			V_A = 4.5 V to 5.5 V		4.85	7	mW
		f_{SCLK} = 0, no output load	V_A = 2.7 V to 3.6 V		1.68		mW
			V_A = 4.5 V to 5.5 V		3.8		mW
P_{PD}	Total power consumption in PD mode	After loading PD mode, f_{SCLK} = 30 MHz, SYNC = V_A, D_{IN} = 0V	V_A = 2.7 V to 3.6 V		0.6	5.4	μW
			V_A = 4.5 V to 5.5 V		2.5	16.5	μW
		After loading PD mode, f_{SCLK} = 0, SYNC = V_A, D_{IN} = 0V	V_A = 2.7 V to 3.6 V		0.3	3.6	μW
			V_A = 4.5 V to 5.5 V		1	11	μW

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7.6 AC and timing characteristics

The following specifications apply to V_A = 2.7 V to 5.5 V, $V_{REF}1,2 = V_A$, C_L = 200 pF to GND, f_{SCK} = 30 MHz, and input code range 12 to 1011 , 48 to 4047 (12808 ONLY) . Unless otherwise specified, all limits are T_A = 25°C.

Table 6

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency			40		MHz
		$T_{MIN} \le T_A \le T_{MAX}$			30	MHz
t_s	Output voltage settling time	**DAC8808**, code changes from 40h to C0h: R_L= 2kΩ, C_L = 200pF		3	4.5	µs
		DAC10808, code changes from 100h to 300h: R_L= 2kΩ, C_L= 200pF		4.5	6	µs
		DAC12808, code changes from 400h to C00h: R_L= 2kΩ, C_L= 200pF		6	8.5	µs
SR	Output conversion rate			1		V/µs
GI	Burr pulse	**DAC8808**, code changes from 80h to 7Fh. **DAC10808**, code changes from 200h to 1FFh. **DAC12808**, code changes from 800h to 7FFh.		40		nV-sec
DF	Digital feedthrough			0.5		nV-sec
DC	Digital crosstalk			0.5		nV-sec
CROSS	Multichannel crosstalk			1		nV-sec
MBW	Output bandwidth	$V_{REF1,2}$ = 2.5V ± 2Vpp		360		kHz
THD+N	Total Harmonic Distortion and Noise	$V_{REF1,2}$ =2.5V ± 0.5Vpp 100Hz < f_{IN} < 20kHz		-80		dB
ONSD	Output noise spectral density	**DAC8808** code = 80h, 10kHz **DAC10808** code = 200h, 10kHz **DAC12808** code = 800h, 10kHz		40		nV/√(Hz)
ON	Output noise	BW=30kHz		14		µV
t_{WU}	Wake-up time	V_A = 3V		3		µs
		V_A = 5V		20		µs
$1/f_{SCLK}$	SCLK Minimum Period			25		ns
		$T_{MIN} \le T_A \le T_{MAX}$	33			ns
t_{CH}	SCLK Minimum High Level Time		7	7		ns
		$T_{MIN} \le T_A \le T_{MAX}$	10			ns
t_{CL}	SCLK Minimum Low Level Time		7	7		ns
		$T_{MIN} \le T_A \le T_{MAX}$	10			ns
t_{SS}	SYNC minimum setup time			3	$1/f_{SCLK}$ -3	ns
		$T_{MIN} \le T_A \le T_{MAX}$	10			ns
t_{DS}	Minimum DATA setup time			1		ns
		$T_{MIN} \le T_A \le T_{MAX}$	2.5			ns
t_{DH}	DATA Minimum Hold Time			1		ns
		$T_{MIN} \le T_A \le T_{MAX}$	2.5			ns
t_{SH}	SYNC hold time after the 16th falling edge of SCLK.			0	$1/f_{SCLK}$ -3	ns
		$T_{MIN} \le T_A \le T_{MAX}$	3			ns
t_{SYNC}	SYNC minimum high-level time			5		ns
		$T_{MIN} \le T_A \le T_{MAX}$	15			ns

8. Typical characteristics

V_A = +2.7V to +5.5V , $V_{REF1,2}$ = V_A , f_{SCLK} = 30MHz , T_A = 25°C , unless otherwise specified.

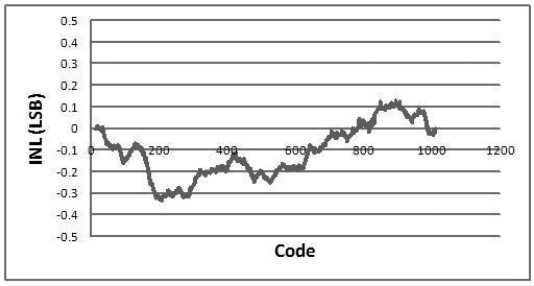


Figure 3. Typical I_{NL} of DAC10808

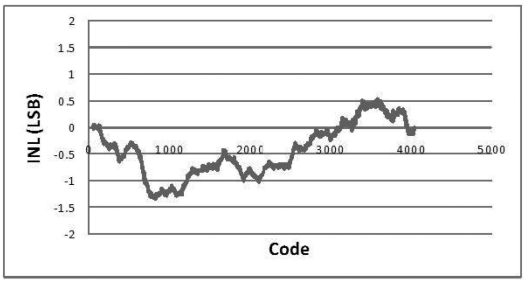


Figure 4. Typical I_{NL} of DAC12808

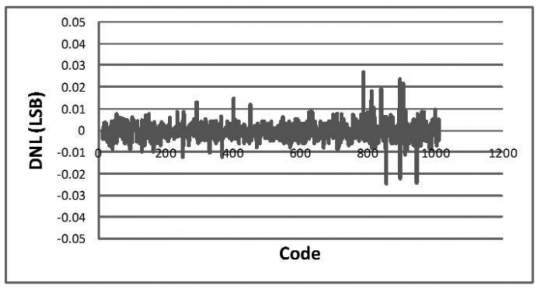


Figure 5. Typical D_{NL} of DAC10808

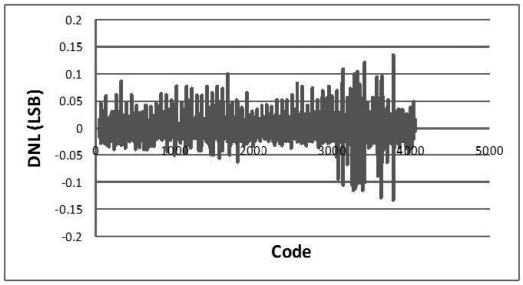


Figure 6. Typical D_{NL} of DAC12808

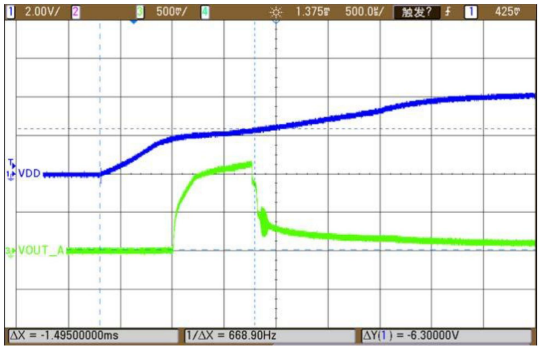


Figure 7. DAC wake-up (exit from sleep state) process

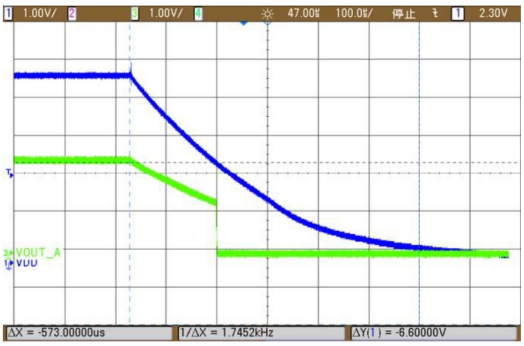


Figure 8. Output setup process (change from 0.25 full amplitude to 0.75 full amplitude).

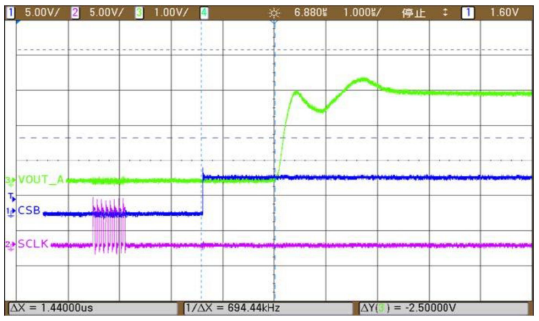


Figure 9. Power- on reset

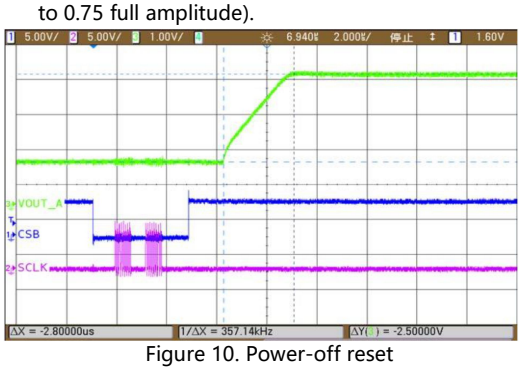


Figure 10. Power-off reset

9. DAC Structure

The DAC8808/10808/12808 is an 8-channel DAC , with each channel containing a DAC register, a resistor string DAC, and an output driver circuit. The resistor string DAC generates corresponding voltage levels through resistor string voltage division, and then switches select the appropriate output. To drive external loads, a buffer driver circuit is added to the output of each channel. A schematic diagram of the resistor string DAC structure is shown in Figure 11. The resistor string consists of N equal-value resistors. A reference voltage is applied directly to the resistor string, and resistor voltage division generates N output voltages, each controlled by N switches. Adjacent voltages are VLSB. Each resistor voltage can be output by closing the corresponding switch. Digital input signals control the opening and closing of the switches. Each input code corresponds to one switch; therefore, for 8-bit precision, N=256 ; for 10-bit precision, N=1024; and for 12-bit precision, N=4096.

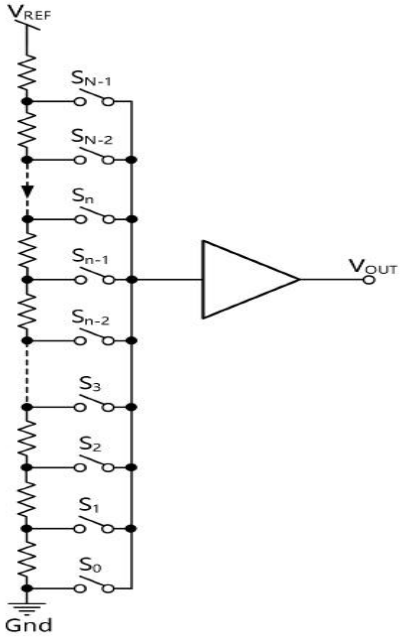


Figure 1.1 DAC resistor string

When the input digital signal is D: $V_{OUT} = V_{REF} \times (D/N)$

When DAC808 is x12, N=4096 ; when DAC808 is x10, N=1024 ; when DAC808 is x08, N=256. The 8-channel DAC in DAC808 x 08/10/12 uses V_{REF1} reference voltage for channels ABCD and V_{REF2} reference voltage for channels EFGH. The reference voltages are directly input externally and can be flexibly set. The digital signal D is written to the internal DAC register via a serial interface, thereby controlling the final output voltage of the DAC. The 8-channel DAC in DAC in DAC808 x 08/10/12 can be individually enabled or put into sleep mode. In sleep mode, the DAC output has three modes: high impedance, 2.5K ohms to ground, and 100K ohms to ground, which can be selected according to actual needs. The DAC output buffer drive circuit adopts a rail-to-rail structure, with an output voltage range of [0, VA] (the actual output voltage range is limited by the reference voltage). When the output voltage approaches 0 or VA , the linearity of the buffer drive circuit deteriorates rapidly. Therefore, the definition of the linearity index INL omits some maximum and minimum codes, which should be noted in practical applications. The output buffer drive circuit can drive a 2K ohm resistive load and a 1500pF capacitor connected to ground or power supply. When the load resistance decreases, the drive current increases accordingly, causing a change in the output voltage. Please refer to the previous characteristic description for specific results. The buffer drive circuit has a built-in output short-circuit protection device with a typical protection current of 20mA.

10. Serial Interface Description

The three-wire serial interface at the input is compatible with SPI™, QSPI, and MICROWIRE, as well as most DSP interfaces, and its clock frequency can reach up to 40MHz. Write operations are performed on the falling edge of the clock, and data is processed in 16-cycle frames, meaning there are 16 falling edges within a single data frame synchronization sequence. Detailed interface timings are shown in Figure 12, and specific values are shown in Table 5.

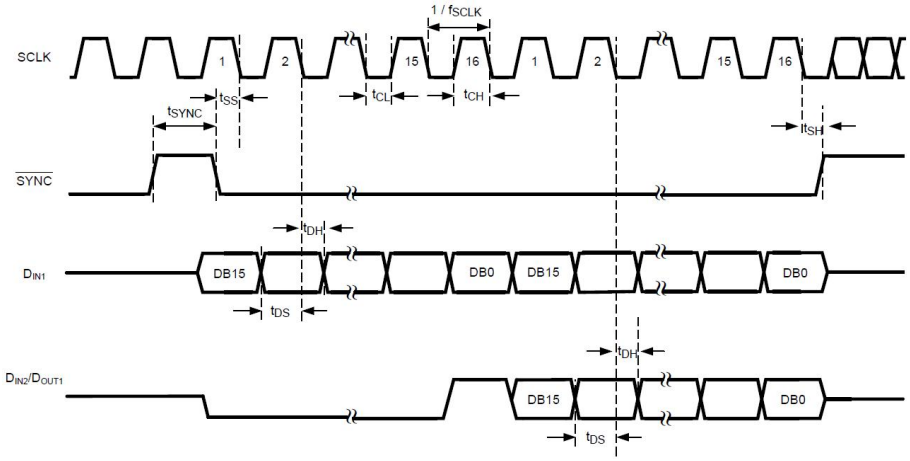


Figure 12 Serial Timing Diagram

Taking writing a single frame of data as an example, when the SYNC signal goes low, the chip's write operation begins. Data input at DIN is synchronized to the shift register via the falling edge of SCLK. To avoid clock errors, the setup time between the falling edge of SYNC and the falling edge of the clock (the timing relationship between SYNC and SCLK) needs to be ensured . When the 16th falling edge of SCLK arrives, the last bit of data is written to the shift register. If the SYNC signal goes high at this time, the chip begins programming operations (channel selection, mode selection, and register content modification, etc.). The falling edge of the clock after the SYNC signal goes high will not affect the chip. If SYNC goes high before the 15th falling edge of the clock, the write sequence data in the shift register will be considered invalid. When more than 17 falling edges of the clock have passed, the data from DIN will be output sequentially on the DOUT port. More information on this operating mode can be found in the daisy-chain operating mode. When DIN is high, the input driver consumes more current; DIN should be idle when the write sequence is active to reduce power consumption. On the other hand, when the DOUT is validly output in daisy-chain mode, the synchronization frame signal should be in an idle state.

11. Daisy Chain Working Mode

Daisy-chain operation allows a single serial controller to operate multiple chips simultaneously, reducing the number of signal lines and simplifying connections. In daisy-chain mode, all chips share the SYNC and SCLK signals, with the DOUT signal of the preceding chip connected to the DIN signal of the following chip. The serial interface still receives data in frames. When the data length exceeds one frame, the chip, while receiving the current frame, sequentially outputs the data from the previous frame from the DOUT port to the subsequent chips, thus serving as the data input for those chips. When the rising edge of the SYNC signal arrives, all chips simultaneously update their serial input registers with the currently received frame data.

Taking a three-chip daisy-chain configuration as an example, the connection is shown in Figure 13. DAC1's DOUT output is sent to DAC2's DIN, and DAC2's DOUT output is sent to DAC3's DIN. The timing sequence for the serial controller sending data is shown in Figure 14. When the SYNC signal is low, three frames of data are sent and output to DAC3, DAC2, and DAC1 respectively. Note the data transmission order. It is particularly important to note that DOUT is updated on the falling edge of the SCLK signal and will be sampled by subsequent chips on the next falling edge of the SCLK signal. To ensure correct sampling, the DIN signal hold time requirement must be met. Therefore, special attention needs to be paid to the delays of the SYNC, SCLK, DIN, and DOUT signals on the board. If necessary, a delay needs to be added between DIN and DOUT.

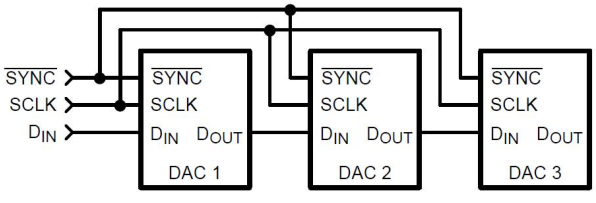


Figure 1.3 Daisy chain connection

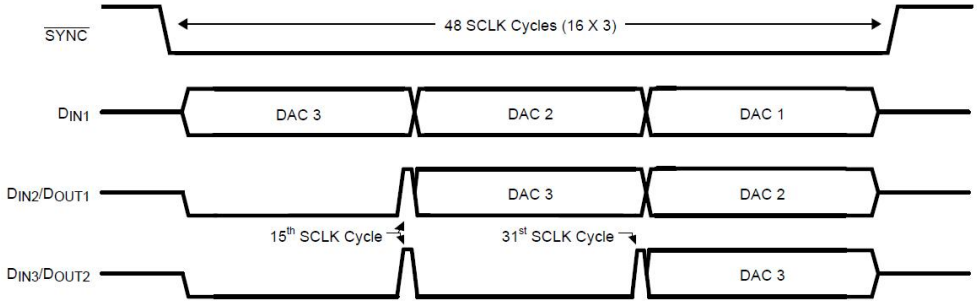


Figure 15 Daisy chain timing

12. Serial Input Register

The serial input register is framed in 16-bit blocks, denoted as DB[15:0]. The first 4 bits, DB[15:12], are mode control bits, and the last 12 bits, DB[11:0], are data bits. A summary of the serial input register is shown in Table 6. The DAC10808 is a 10-bit DAC; therefore, when D[15]=0, only D[11:2] of the data bits D[11:0] is valid, and the remaining D[1:0] are invalid. D[11] is the MSB, and D[0] is the LSB. DB[15:12]

Serial input data is divided into four types: write data/DAC register, mode control, special commands, and sleep mode, each corresponding to a different function.

Serial input register description: Table 7

Type	DB[15:12]	DB[11:0]	Description
Hibernation mode	1111	xxxx_HGFEDCBA	The corresponding bit in DB[7:0] is "1" , the corresponding channel enters sleep mode and outputs a 2.5K ohm impedance.
	1110	xxxx_HGFEDCBA	The corresponding bits of DB[7:0] are "1" , the corresponding channel enters sleep mode and outputs a 100K ohm impedance.
	1101	xxxx_HGFEDCBA	The corresponding bit in DB[7:0] is "1" , the corresponding channel enters sleep mode and outputs high impedance.
Special commands	1100	D11 D10 ... D1 D0	Broadcast mode : The data registers and DAC registers of all channels are updated simultaneously to the values of DB[11:0].
	1011	D11 D10 ... D1 D0	Channel A Update: The data register and DAC register of Channel A are updated to DB[11:0] simultaneously, and the DAC registers of the other 7 channels are also updated to the values of the corresponding data registers simultaneously.
	1010	xxxx_HGFEDCBA	Update selection: When a bit in DB[7:0] is "1" , the corresponding channel DAC register is updated to the value of the data register, and the DAC output is also updated accordingly.
Mode control	1001	xxxx_xxxx_xxxx	WTM: Writing data to the channel's register will cause a change in the DAC output.
	1000	xxxx_xxxx_xxxx	WRM: The registers of each DAC channel can be written to without changing its output.
Data Register (DAC Register)	0111	D11 D10 ... D1 D0	WRM : D[11:0] Writes only to the H channel data register ; WTM : D[11:0] Directly updates the H channel DAC register.
	0110	D11 D10 ... D1 D0	WRM : D[11:0] Writes only to the G channel data register ; WTM : D[11:0] Directly updates the G channel DAC register.
	0101	D11 D10 ... D1 D0	WRM: D[11:0] Writes only to the F channel data register ; WTM: D[11:0] Directly updates the F channel DAC register.
	0100	D11 D10 ... D1 D0	WRM: D[11:0] Writes only to the E channel data register ; WTM: D[11:0] Directly updates the E channel DAC register.
	0011	D11 D10 ... D1 D0	WRM: D[11:0] Writes only to the D channel data register ; WTM: D[11:0] Directly updates the D channel DAC register.
	0010	D11 D10 ... D1 D0	WRM: D[11:0] Writes only to the C channel data register ; WTM: D[11:0] Directly updates the C channel DAC register.
	0001	D11 D10 ... D1 D0	WRM: D[11:0] Writes only to the B channel data register ; WTM: D[11:0] Directly updates the B channel DAC register.
	0000	D11 D10 ... D1 D0	WRM: D[11:0] Writes only to the A channel data register ; WTM: D[11:0] Directly updates the A channel DAC register.

Each DAC channel contains two registers: a data register and a DAC register. Updating the DAC register directly updates the DAC's output analog signal. The data register temporarily stores data input from the serial interface. Users can send commands to update the DAC register to the value in the data register. After all data registers are written, users can send commands to control the simultaneous update of the outputs of all DAC channels. There are two modes for updating the serial interface control registers: WRM (Write Register Mode) and WTM (Write Through Mode). When writing data/DAC registers, only the data register is updated in WRM mode, while in WTM mode, both the data register and DAC register are updated simultaneously. The chip defaults to WRM mode upon power-up. There are three special serial input commands: Update Select, Channel A Update, and Broadcast Mode. The Update Select command selectively updates the DAC register of a specific channel, thereby updating the DAC output; the Channel A Update command updates the DAC output of all channels simultaneously while writing data to Channel A; the Broadcast command updates the data register and DAC register of all channels to the same value simultaneously.

13. Hibernation Mode

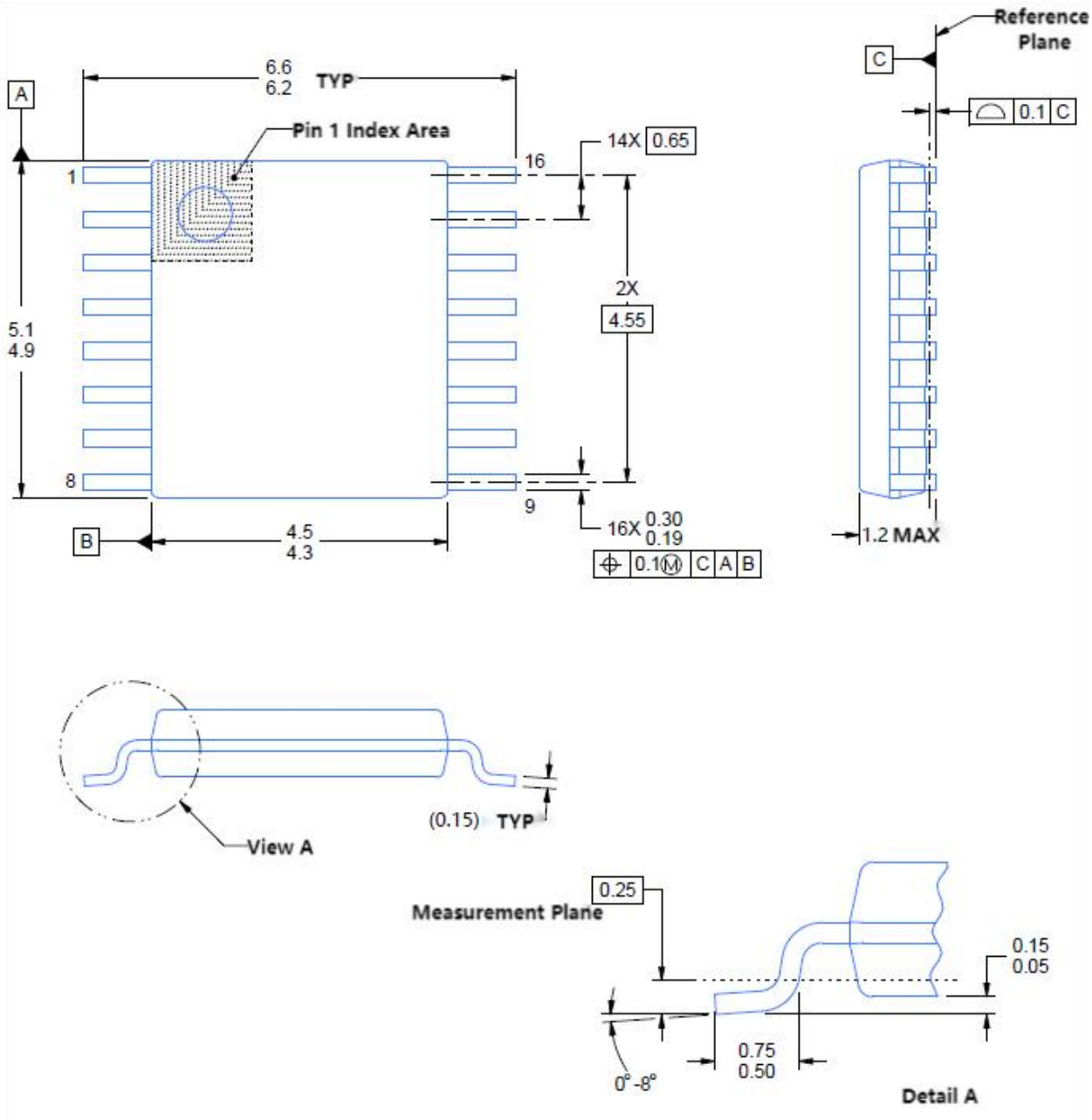
the DAC8808/10808/12808 can be individually configured into sleep mode. Sleep mode is configured by setting the serial input register. Set DB[15:12] to the desired sleep mode and set the corresponding bit of the channel requiring sleep to "1" . When all 8 channels of the DAC are in sleep mode, the internal bias circuitry also goes into sleep mode. However, the internal power-off reset circuitry continues to operate normally, typically consuming approximately 10uA of current.

14. Power-on/Power-off Reset

The DAC8808/10808/12808 internally contains both power-on reset and power-off reset circuits. This reset circuit simultaneously controls the output of all channels. After reset, the data/DAC registers of all channels are set to all zeros, and the final output of the DAC is also at a zero level. A reset operation is generated when the power supply voltage rises to the chip's minimum operating voltage, as shown in Figure 9. A power-off reset occurs during the chip's power-off process; when the power supply voltage drops below approximately 2.7V, a reset operation is generated, as shown in Figure 10.

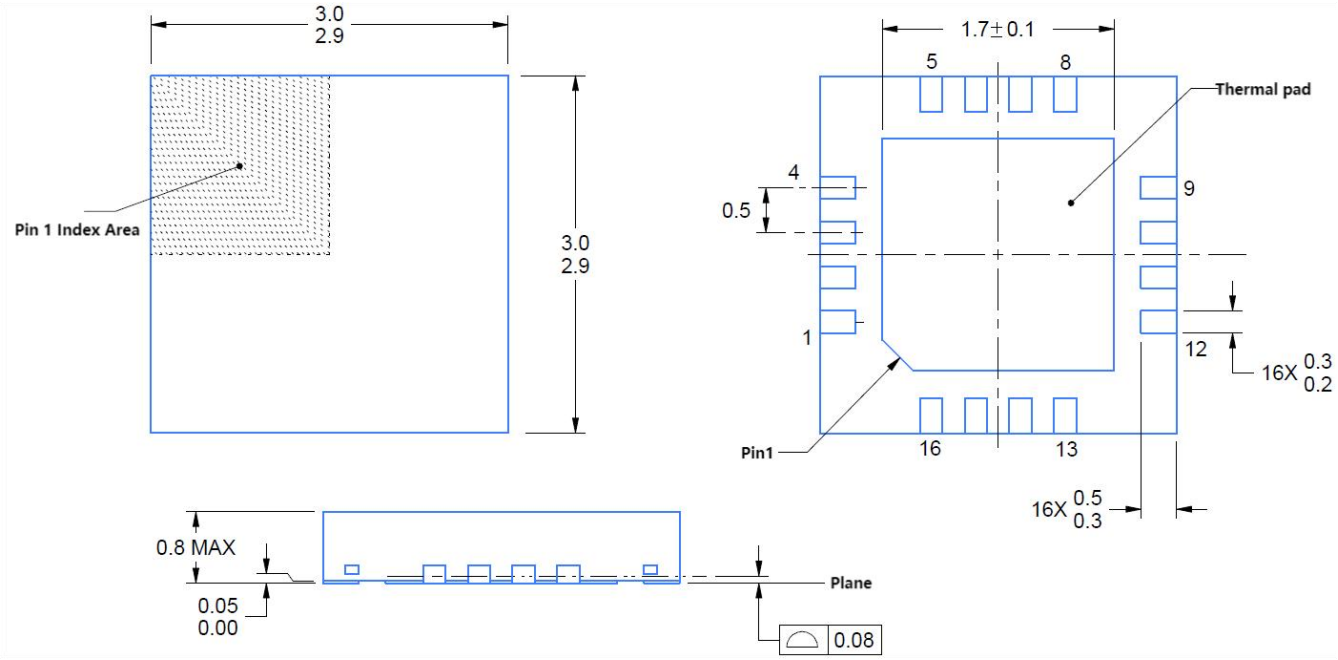
15 . Package Dimensions and Structure

TSSOP16 Package



Note: Unit is mm

QFN 16 Package



Note: Unit is mm

16 . Package Information

Model		Temperature range	Packaging	Package
DAC8808	DAC8808QF	-40 ℃ ~125 ℃	QFN16	4,000/reel
	DAC8808TS	-40 ℃ ~125 ℃	TSSOP16	4,000/reel
DAC10808	DAC10808QF	-40 ℃ ~125 ℃	QFN16	4,000/reel
	DAC10808TS	-40 ℃ ~125 ℃	TSSOP16	4,000/reel
DAC12808	DAC12808QF	-40 ℃ ~125 ℃	QFN16	4,000/reel
	DAC12808TS	-40 ℃ ~125 ℃	TSSOP16	4,000/reel